15.6 A 12b 250MS/s Pipelined ADC with Virtual Ground Reference Buffers

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High-performance op-amps in a switched-capacitor pipelined ADC consume high power to meet accuracy and speed requirements. This is aggravated by the decrease in intrinsic transistor gain and voltage headroom in nanoscale CMOS. Developments in pipelined ADCs have taken many unique directions to address these issues. Digital calibration of nonlinearity has enabled the use of low-performance op-amps [1]. Non-op-amp-based approaches, such as zero-crossing-based circuits (ZCBC) [2], the pulsed bucket brigade (PBB) [3], and the ring amplifier (RA) [4], have also been explored. This work presents a virtual ground reference buffer approach to significantly relax key op-amp specifications including unity-gain bandwidth, noise, and open-loop gain. Since the op-amp is allowed to settle fully, calibration to remove charge-transfer error in PBB and low gain or non-settling op-amp-based circuits is unnecessary. Also the transient current and corresponding voltage drop across switches and reference buffers in the ZCBCs and in non-settling op-amp-based circuits are avoided. The circuit is also shown to achieve higher maximum operating speed than alternative methods.

The concept is illustrated in Fig. 15.6.1, where the charge-transfer phase is shown in a 1b/stage ADC for both the conventional and the proposed scheme. In both cases, parasitic capacitance is ignored, and the op-amp is assumed to have infinite open-loop gain. The input voltage V_{IN} is sampled on C_1 and C_2 during the preceding input sampling phase. In the conventional circuit, C_1 is tied to either V_{REFP} or V_{REFM} depending on the bit decision. Both V_{REFP} and V_{REFM} are referenced to the system ground as shown in Fig. 15.6.1. The corresponding feedback factor is $\beta=C_2/(C_1+C_2)$, and the signal gain is $G_S=1/\beta$. The closed-loop bandwidth is f_u/G_S where f_u is the unity-gain bandwidth of the op-amp. Since G_S is typically significantly larger than 1, f_u must be much higher than the closed-loop bandwidth required for settling. The signal gain is also equal to the op-amp noise gain. Therefore, op-amp noise referred to the signal input is the same as that referred to the op-amp input. Also, high open-loop gain is required for small charge-transfer error.

In the virtual ground reference buffers, V_{REFP} and V_{REFM} are referenced to the virtual ground instead of the system ground as shown in Fig. 15.6.1. The reference buffers level-shift the virtual ground potential to V_{REFP} and V_{REFM}. Therefore, the output voltage of the ADC stage is identical to that of the conventional ADC stage once the op-amp settles. The main difference is the feedback factor. If the level-shifting buffer has an incremental gain of 1, the capacitor C_1 is bootstrapped away, providing a feedback factor of unity. Therefore, its closed-loop bandwidth f_u, is higher by a factor of G_S compared with the conventional circuit. This allows lower op-amp power or faster operation. Moreover, the op-amp noise gain is 1, reducing the total integrated op-amp noise referred to the signal input by a factor of G_S. Finally, it can be shown that the open-loop gain and offset requirement of the op-amp are reduced by the same factor. It is important to note that the benefits are obtained without affecting the signal gain. For a fair comparison, however, bandwidth, noise, and power consumption of the buffers must be considered. In the presented ADC, the buffers replace existing reference buffers, thus incurring insignificant penalty; while off-chip bypass capacitors can be used in conventional circuits to ease the reference buffer requirements, on-chip high-speed buffers are typically strongly desired in high-speed, high-SNR ADCs to avoid reference voltage ringing.

In practice, the buffer's incremental gain is typically less than unity so that C_1 is not completely bootstrapped away; a portion of C_1 loads the virtual ground node. In addition, the parasitic capacitance at the virtual ground node can further degrade the feedback factor. However, much of it can be bootstrapped away by the buffer itself. A significant improvement in feedback factor is retained compared with a conventional circuit. A typical feedback factor β in a conventional pipelined stage with a signal gain G_S of 8, is 1/10 considering the parasitic capacitance. In simulation, the prototype improves β to approximately 0.3, by a factor of 3. With further optimization, β could be realistically improved to 1/2, reducing the op-amp requirements in closed-loop bandwidth, input-referred noise power, open-loop gain, and offset by a factor of 5. Greater improvements are obtained as more bits are resolved per stage since the improvement in the feedback factor becomes more dramatic with higher signal gain. A non-level shifting buffer was previously suggested for jitter and load-insensitive charge-transfer in continuous-time delta-sigma ADCs [5].

In actual multibit ADC stages, C_1 is replaced by a capacitor array, and the outputs of the reference buffers are applied to the capacitors in a similar fashion to a conventional ADC stage. For simplicity, a source follower is chosen for each level-shifting buffer, whose V_{GS} serves as a reference. PMOS and NMOS source followers provide positive and negative reference voltages, respectively. The schematic of the first stage is shown in Fig. 15.6.2. The ADC employs a pipelined architecture with 3.9b, in the first stage, 2.8b in the subsequent stages, and a 4.5b flash backend. Little effort was made for power optimization in this prototype. Gain-enhanced telescopic op-amps are used from stage 1 to stage 4 without scaling for simplicity, leaving ample room for reduction in power consumption in the future. The buffers are scaled down by a factor of three from stage 1 to stage 2. The bandwidth of the buffers is made larger than the closed-loop bandwidth of op-amp as in the conventional circuit. The noise in the buffer is thus filtered by the op-amp bandwidth.

The flipped voltage follower (FVF) [6] is used as the level-shifting buffer. Compared with simple source followers, they provide much higher slew rate in the direction critical to the level-shifting buffers in this application. A switched-capacitor circuit sets the body-to-source voltage, V_{BS}, of the input transistors of the buffers to adjust their V_{GS} to the desired reference levels. Approximately 350mV of forward bias is applied in both the NMOS and PMOS FVF to achieve the differential reference of approximately 800mV. Their bias currents are controlled by current DACs for fine-tuning of the reference voltages to the desired level in the foreground. Although straightforward, automatic reference tuning was not implemented for simplicity and flexibility of testing.

The ADC is implemented in 65nm LP CMOS and the core occupies 0.59mm^2 (Fig. 15.6.7). The chip operates at 1.2V, and consumes 49.7mW at 250MS/s: 2.0mA in the biasing cell, 23.3mA in the op-amps, 6.9mA in the buffers, 6.0mA in the clock, digital and flash ADC, and 3.3mA in the flash reference ladders. The full-scale input signal range is approximately 1.5Vpp. Standard capacitor mismatch calibration was applied in the foreground off-chip and the calibration coefficients are frozen throughout the measurements. During the normal conversion, the capacitor mismatch calibration is estimated to consume 100µW if implemented on chip. The DNL and INL are within -0.86/+0.52 LSB and -0.90/+1.08 LSB, respectively, as shown in Fig. 15.6.3. Figure 15.6.4 shows the SNDR and SFDR vs. input frequency at 250MS/s from three randomly selected chips. The SNDR is 67.0dB and 65.7dB at 12.1MHz and 121.8MHz input frequency, respectively. The SNDR degradation at Nyquist is mostly due to the sampling clock jitter. It achieves an FoM of 108.5fJ/conv-step and 126.8fJ/conv-step at 12.1MHz and 121.8MHz input signal, respectively. Figure 15.6.5 shows better than 10.3 ENOB at sampling rates up to 280MS/s. The performance of this work compared to other single-channel ADCs in the similar performance range is summarized in Fig. 15.6.6

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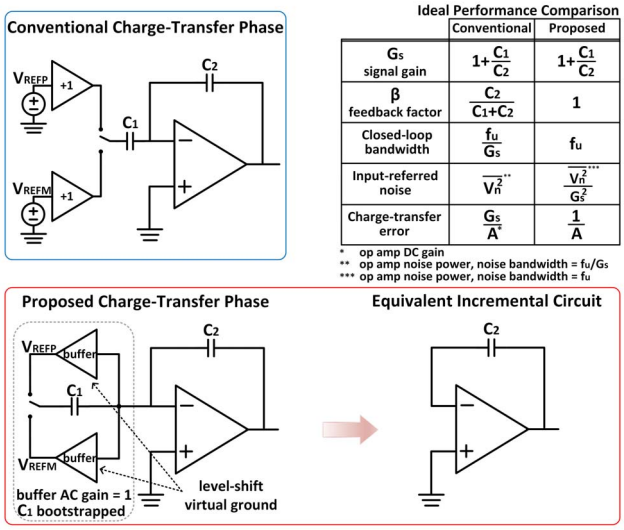

Ideal Performance Comparison

	Conventional	Proposed
G_s signal gain	$1+\frac{C_1}{C_2}$	$1+\frac{C_1}{C_2}$
β feedback factor	$\frac{C_2}{C_1+C_2}$	1
Closed-loop bandwidth	$\frac{f_u}{G_s}$	f_u
Input-referred noise	$\overline{V_n^2}^{**}$	$\frac{\overline{V_n^2}^{***}}{G_s^2}$
Charge-transfer error	$\frac{G_s}{A^*}$	$\frac{1}{A}$

* op amp DC gain
** op amp noise power, noise bandwidth = f_u/G_s
*** op amp noise power, noise bandwidth = f_u

Figure 15.6.1: Performance comparison between the conventional switched-capacitor circuit and the virtual ground buffer technique.

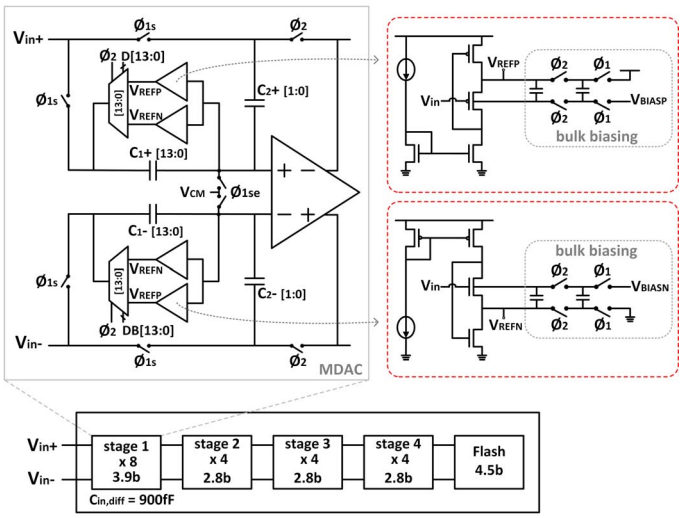

Figure 15.6.2: Circuit implementation of the first pipelined stage and the level-shifting buffers with bulk biasing.

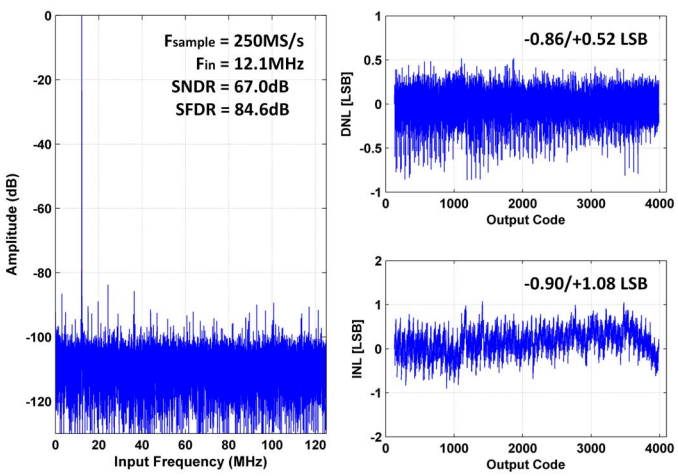

Figure 15.6.3: Measured FFT and DNL/INL.

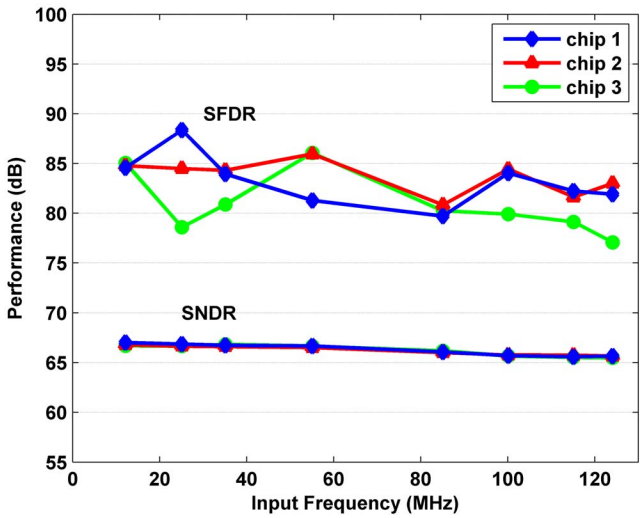

Figure 15.6.4: Measured dynamic performance vs. input frequency for three chips.

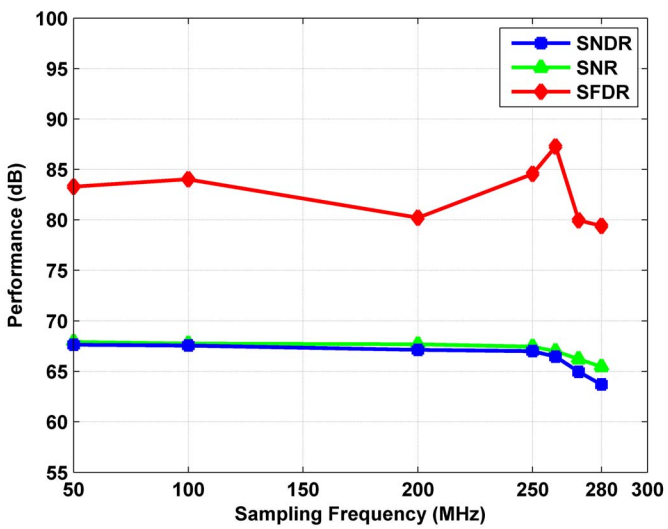

Figure 15.6.5: Measured dynamic performance vs. sampling frequency.

	This Work	Shin JSSC 2014	Dolev [3] VLSI 2013	Sahoo JSSC 2009
Technology	65nm	55nm	65nm	90nm
Type	Op-amp-based virtual ground reference buffer	Zero-crossing based	Bucket brigade digital calibration	Op-amp-based digital calibration
Sampling Rate	250MS/s	200MS/s	200MS/s	200MS/s
Resolution	12b	12b	12b	12b
Power Supply	1.2V	1.1V	1V	1.2V
Input Signal Range	1.5Vp-p	2Vp-p	-	1.2Vp-p
SNDR	67.0dB @ 12.1MHz 65.7dB @ 121.8MHz	64.6dB @ 10.1MHz 63.2dB @ 100MHz	65dB @ 1MHz 57.6dB @ 99MHz	64dB @ 3.5MHz 61.6dB @ 91MHz
SFDR	84.6dB @12.1MHz	82.9dB @ 10.1MHz	82dB @ 1MHz	70dB
Power	49.7mW	30.7mW	11.5mW*	348mW
FoM	108.5fJ/step	111.0fJ/step	39.6fJ/step*	1.34pJ/step

*Excludes power consumption in reference buffers and digital calibration circuit

Figure 15.6.6: Performance summary and comparison.

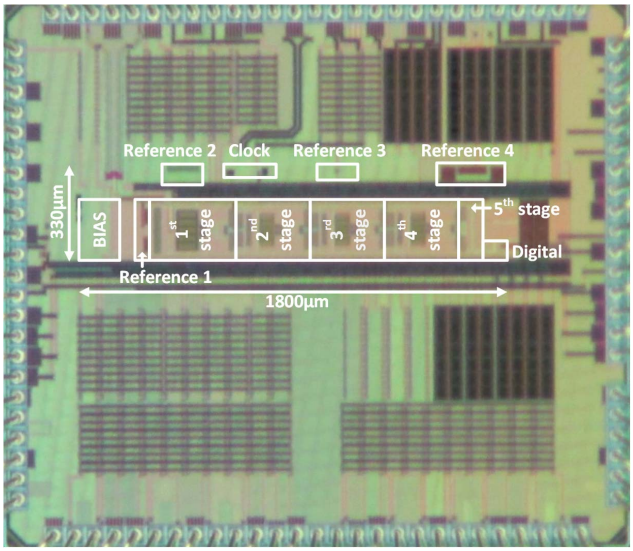

Figure 15.6.7: Die photograph.

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