22.1 An 83dB-Dynamic-Range Single-Exposure Global-Shutter CMOS Image Sensor with In-Pixel Dual Storage

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CMOS image sensors with rolling exposure have come to be widely used, but they cannot avoid the distortion inherent to rolling exposure no matter how much exposure speed improves for capturing a moving target. The need has consequently been felt for global-shutter CMOS image sensors.

An in-pixel low-leakage analog memory is required to realize a global-shutter CMOS image sensor. A floating diffusion (FD) can be used as a storage node, but the readout signal is affected by the reset kT/C noise due to delta reset sampling (DRS) used instead of correlated double sampling (CDS) [1]. This is why global-shutter CMOS image sensors incorporate an additional in-pixel storage node (MEM) especially for achieving high-SNR image quality [2-4]. However, incorporating a MEM within the pixel reduces the area occupied by the photo-diode (PD) inside the pixel, which limits the full-well capacity [2,3]. A technique with global multiple exposures helps to extend the dynamic range [4], but the composite image using different exposure periods results in some picture artifacts when capturing a moving target.

In this paper, we report a dual-storage scheme for a global-shutter function to extend the dynamic range to 83.0dB without any picture distortion or artifacts. The dual-storage scheme employs PD and MEM as charge-accumulation nodes, and then MEM and FD as charge storage nodes for low-intensity and high-intensity signals, respectively. Here, selective accumulation and retention are achieved by overflow control on a transfer gate maintaining a readout noise of $4.8e\text{-}_{rms}$.

A block diagram of the image sensor is shown in Fig. 22.1.1. The sensor consists of a pixel array, column single-slope 12b ADCs, slope generators, control circuits, SLVS-EC with 8 channels placed above and below the pixel array, and drivers. Hybrid counters [5] are laid out in blocks of 272 columns. One channel of SLVS-EC achieves an output rate of 2.376Gb/s with all 8 channels achieving 19Gb/s. The drivers consist of rolling-shutter drivers and global-shutter drivers for single-storage and dual-storage modes. In dual-storage mode, each pixel requires a MEM and FD. The operation of this chip in this mode is therefore checked by disabling one of every two pixels that share a single FD. This means that there are 10M effective pixels in single-storage readout and rolling-shutter readout against 5M effective pixels in MEM+FD dual-storage readout.

The simplified readout sequences in the dual-storage mode are shown in Fig. 22.1.2. The dual-storage scheme proceeds as follows. 1) A global RST is performed across all pixels to simultaneously dispose of charges in the PD, MEM, and FD. 2) The transistors controlled by OFG, TRX, and TRG are turned OFF and exposure is started. During the exposure process, the PD electrons that reach a threshold intensity due to the high intensity of incident light are partially transferred as overflow to the MEM by midpoint potential drives. Conversely, no electrons are transferred at a pixel where incident light is of low intensity. 3) On completion of exposure and after the FD has been reset by RST, the overflow charge accumulated in the MEM is transferred to the FD. 4) The charge accumulated in the PD is transferred to the MEM and then the charge that is now stored in the MEM and FD remains there until readout. Here, both signals stored in the MEM and FD are obtained in the same single exposure. 5) The signal stored in FD is read out by DRS. 6) The signal stored in MEM is read out by CDS. The readout to the external frame memory is completed in 30ms at 12b for CDS and DRS. If the signal obtained by the CDS readout is less than a certain number of electrons, only the kT/C-noise-free CDS-readout signal is used to reconstruct a final image. Otherwise, if the signal is greater than the number of electrons that would make the photon-shot signal the dominant noise, the sum of CDS-readout and DRS-readout signals is used.

Figure 22.1.3 shows the schematic diagram of the comparator and its control signals. Both CDS and DRS readout operations are performed by the same single-slope ADC. The CDS readout operation proceeds as follows. First, an auto-zero operation is performed as analog CDS. Next, the reset level is down-counted from the LSB until the comparator changes, and finally, the signal level is up-counted likewise until the comparator changes again thereby achieving the digital-CDS readout. Turning to the DRS readout operation, the vertical signal line (VSL) rises from a low level after reset. To adjust the comparator's operation range, V_{DRS} can be applied to the input node of the comparator by control signal Φ_{DRS}. Up-counting can now be performed from the full-scale code until the counter changes to obtain the signal level the same as in CDS. Following this, the DRS readout is completed by down-counting also until the counter changes to obtain the reset level. This implementation needs only two additional transistors per column relative to the former comparator [5].

Figure 22.1.4 shows the measured output characteristics of the dual-storage mode and single-storage global-shutter modes. The full-well capacity of 32,200e- in single-storage mode is extended to 67,700e- in dual-storage mode. In this study, we decided on 5,000e- as the switching point of electrons to calculate the composite MEM+FD signal. For this sufficient electron value, the inevitable photon shot noise of about $70e\text{-}_{rms}$ is dominant rather than the other random noise sources including kT/C, meaning no significant visible noise [6].

Sample images are shown in Fig. 22.1.5 (a), (b), and (c) for global-shutter dual-storage mode, global-shutter signal-storage mode and the rolling-shutter mode, respectively. To compare them at the same pixel resolution, these images are down-sampled to 2.5Mpixels. These images show that dynamic range in the dual-storage mode is extended beyond that in single-storage mode. In addition, no distortion, artifacts or boundaries are observed in dual-storage mode.

Chip specifications are summarized in Fig. 22.1.6. This true global shutter sensor is fabricated in a 90nm 1P4M CMOS sensor process with a light shield layer. The supply voltages are 3.3V for the pixel and analog circuits, 1.2V for the digital circuits and comparator bias voltage, and 0.4V for the SLVS-EC circuits. The sensor achieves a readout speed of 30ms in dual-storage mode (5M effective pixels) and a readout speed of 30ms in single-storage and rolling-shutter modes (10M effective pixels) at 12b resolution. A kT/C-free noise level of $4.8e\text{-}_{rms}$ is maintained under a dark level. A saturation signal of 32,200e- in the single-storage mode is extended to 67,700e- in dual-storage mode thereby extending the dynamic range from 76.5dB to 83.0dB under a single exposure. A sensitivity of 78ke-/lx·s and a parasitic light sensitivity of less than -100dB are achieved. The measured power consumption is typically 2W. The die micrograph is shown in Fig. 22.1.7 and the size is 28.9mm(H) ×23.1mm(V).

We achieve a true global shutter under a single exposure with a dynamic range of 83dB in a 5M-effective-pixel CMOS image sensor. The dual-storage scheme with the appropriate signal readout method, a full-well capacity of 67,700e- is realized while maintaining a kT/C-free noise level of $4.8e\text{-}_{rms}$ under a dark level.

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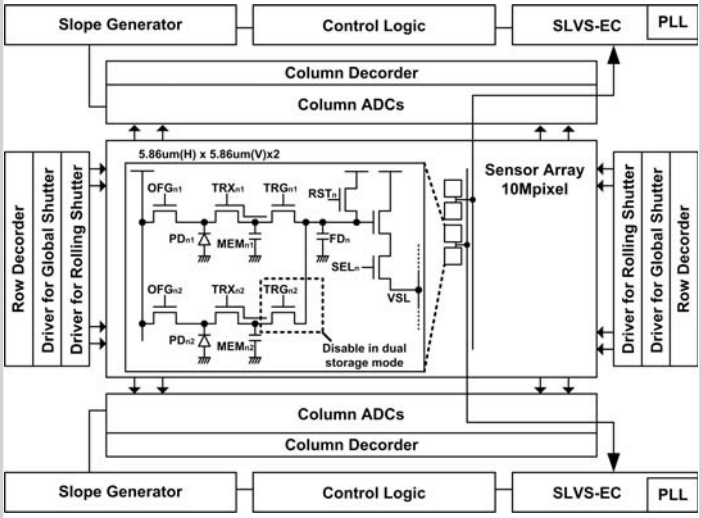

Figure 22.1.1: Block diagram.

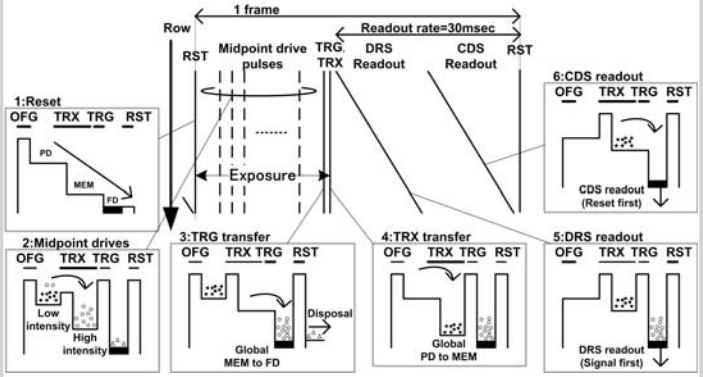

Figure 22.1.2: Readout sequences of dual-storage mode.

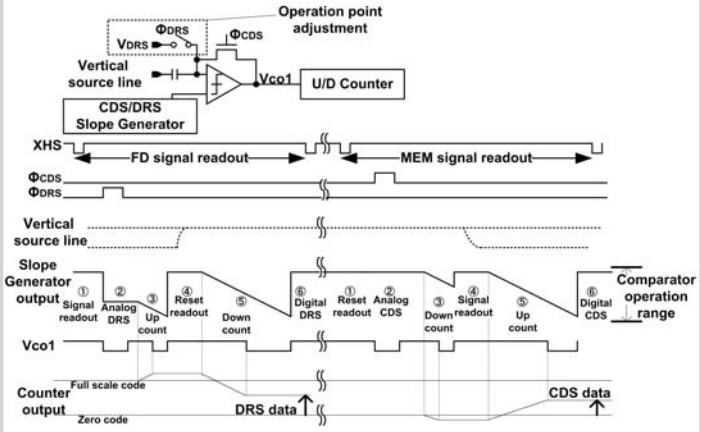

Figure 22.1.3: Comparator and timing diagram for horizontal periods of DRS and CDS.

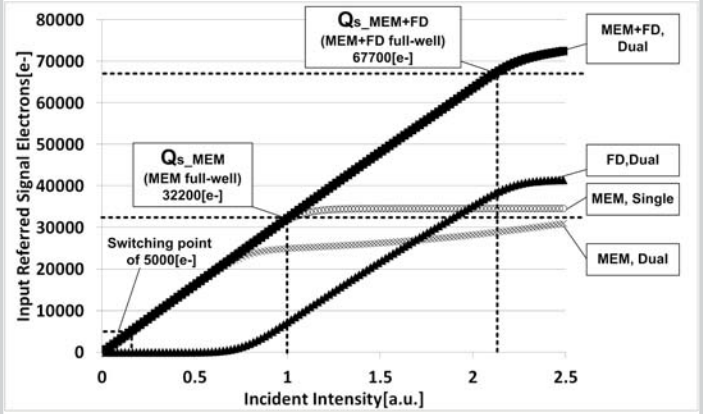

Figure 22.1.4: Measured output characteristics of dual-storage and single-storage global-shutter modes.

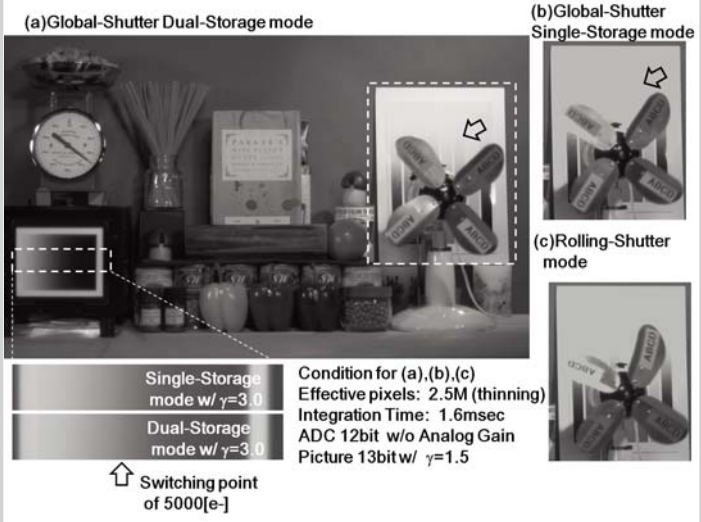

Figure 22.1.5: Sample images.

Fabrication process	90nm 1P5M + Light Shield
Supply voltage	3.3[V]/1.2[V]/0.4[V]
Effective pixels(Dual-Storage)	5Mpixel
(Single-Storage / Rolling)	10Mpixel
Pixel size	5.86[μm] x 5.86[μm]
Readout rate	30[msec] in Dual-storage mode
Power consumption	2[W]
Saturation signal (Single-Storage)	32200[e-]
(Dual-Storage)	67700[e-]
Sensitivity	78[ke-/lx·s] at 3200K light source with 650nm IR cut-off
Parasitic light sensitivity(MEM / FD)	<-100 [dB]
CDS(MEM) read noise	4.8[e^-_{rms}] (Analog gain +18dB)
Dynamic range (Single-Storage)	76.5[dB]
(Dual-Storage)	83.0[dB]

Figure 22.1.6: Chip characteristics.

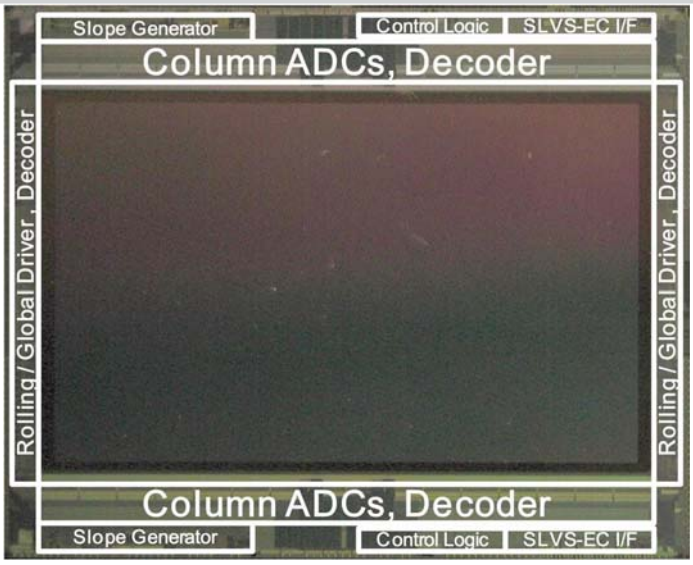

Figure 22.1.7: Chip micrograph.

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