# Design for Test of a mm-Wave ADPLL-Based Transmitter

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***Abstract* — The advantages of on-chip debugging capability and critical RF performance characterization are myriad in a system-on-chip (SoC) application. This paper focuses on design for test (DFT) and design for characterization (DFC) techniques applied to an all-digital phase-locked loop (ADPLL) transmitter targeting mm-wave frequencies. System snapshotting via on-chip SRAM to identify the root cause of the design deficiencies accurately is proposed. More importantly, offer the possibility of self-healing. Moreover, low-cost, built-in self test (BIST) and self characterization (BISC) of an ADPLL performance including critical building blocks (e.g., digitally controlled oscillator) are presented. RF characterization capability on chip enhances test coverage, and reduces test time and production cost. The DFT and DFC techniques are integrated and benchmarked using a 60-GHz ADPLL-based transmitter in 65-nm CMOS.**

***Index Terms* — Design for test (DFT), built-in self test (BIST), built-in self characterization (BISC), all-digital phase-locked loop (ADPLL), ADPLL-based transmitter, digitally controlled oscillator (DCO), phase error analyzer.**

## I. Introduction

Testing and debugging of a complex mixed-signal system-on-chip (SoC) for wireless consumer applications affects both product development time and cost. Testing costs are often high, since high-volume wireless applications are checked extensively for defects, RF performance, and wireless standard compliance by using sophisticated test equipment. Debugging also becomes more difficult because the number of I/Os available to access an SoC during testing are constrained.

Frequency synthesizers and transmitters are tested for RF performance by measuring the carrier frequency, phase noise (PN) spectral density, integrated PN, spurious content, and modulated phase error trajectory at the RF output when modulation stimuli are applied [1][2]. In a debugging scenario, it is difficult to identify the root cause and provide a fix when the phase-locked loop (PLL) fails to lock, or degraded performance is observed at the RF output (e.g., poor PN, or high spur levels). Although functional testing of individual blocks can be conducted open loop, relating closed-loop PLL performance to the performance of individual circuit blocks is non-trivial due to the tight feedback nature of a PLL [3].

Alternatively, built-in self test (BIST) requires no external test equipment. It is widely used to reduce testing time and cost of digital ICs, while increasing the test coverage. Including BIST capabilities in mixed-signal RFICs lessens the need for high-performance test equipment and provides data for debugging purposes [4]. These benefits are easier to realize on SoCs with all-digital PLLs (ADPLL), as the most of the PLL and its signal path can be accessed and evaluated by digital signal processing with little hardware overhead. By comparison, analog charge-pump PLLs are difficult to adapt for BIST because loading sensitive analog nodes for test purposes changes loop behavior and skews the measured data [1].

Aside from debugging, BIST applied to RF performance characterization of low-GHz ADPLLs has been reported in [5]-[8], where digital signal processing of a lower-frequency internal signal is used to ascertain RF performance without external test equipment. In this paper, we present a systematic approach to debugging and testing employing system snapshots, as well as BIST and built-in self characterization (BISC) in an ADPLL-based transmitter. The digitally intensive SoC integrates the ADPLL, a digital baseband processor, SRAM, and power management functions. Due to the reuse of SRAM and signal processing circuitry, very little hardware overhead is required to implement the proposed design for test (DFT) and design for characterization (DFC) techniques. The system snapshot is triggered by a sequence of major internal events in normal operation of the PLL. It captures the transient behavior of the loop at a particular moment for observation, and provides a means of analyzing loop operation analogous to simulation methodologies. Thus, snapshotting is a very powerful tool when searching for faults in a closed-loop feedback system.

Although the DFT techniques in this paper are described in the context of a 60GHz ADPLL-based FMCW radar transmitter (see Fig. 1), the same ideas apply to a general class of digitally intensive PLLs and two-point modulation transmitters - especially those using a digitally controlled oscillator (DCO), time-to-digital converter (TDC), and digitization of a conventional phase/frequency detector output [9].

The ADPLL-based transmitter is described briefly in Section II of the paper. The critical, internal digital signals and events for debugging are elaborated further in Section III. Section IV describes a systematic method of monitoring these signals using system snapshots. BIST and BISC applied to the DCO and ADPLL are then presented

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in Section V. The measurement setup and results for a 60-GHz ADPLL prototype employing these DFT techniques are described in Section VI.

## II. ADPLL-Based FMCW Transmitter

Fig. 1 depicts a generic ADPLL-based frequency modulated continuous wave (FMCW) transmitter architecture, which is digitally intensive, providing extensive re-configurability and DFT opportunities. The output frequency is controlled by a negative feedback loop comprising the DCO, a TDC and incrementer to estimate the DCO phase ($R_v$+ε), a frequency command word (FCW) accumulator to calculate the reference phase ($R_r$), an arithmetic subtractor to calculate the phase error ($\Phi_E$), and a digital loop filter (LF) to control the ADPLL bandwidth and transfer function characteristics.

The transmitter is configured to generate a ramp frequency by incorporating two-point frequency modulation directly into the ADPLL without the need for an up-conversion mixer [10]. One data path modulates the DCO directly, while the other path compensates the frequency reference and prevents the modulating data from affecting $\Phi_E$. The direct path has high-pass characteristic, while the other low-pass filters the signal. When both paths are combined with no delay mismatch, an all-pass transfer function is realized to achieve wideband FM. Therefore, the variation of $\Phi_E$ indicates the RF performance measured at the transmitter output, which makes BIST possible.

A block diagram of the 60-GHz digital transmitter implemented in this work is shown in Fig. 2, emphasizing the ADPLL [11]. The DCO oscillates in the 60-GHz band. Three tuning banks provide 7-GHz tuning range and ~1 MHz raw frequency resolution. An extra ΣΔ dithering bank operating at ~1 GHz improves the frequency resolution to 400 Hz. The DCO is transformer-coupled to a 60-GHz power amplifier (PA), and also drives a divide-by-32 prescaler to generate CKV/32 at ~2 GHz to feed the rest of the loop. The DCO, PA and prescaler operate at ~60 GHz and would require test equipment and on-die probing in order to characterize their RF performance. Section V describes how RF-BIST is used to characterize them instead.

The underlying frequency stability of the ADPLL is derived from an external reference frequency (FREF) crystal oscillator ($f_R$ = 10…100 MHz). The FCW is defined as the desired FREF to CKV frequency-multiplication ratio of and is expressed in a fixed-point format. The CKV/32 oversamples the FREF to generate a retimed clock CKR as a synchronous system clock. To avoid metastability in retiming, FREF is oversampled by rising and falling edges of CKV/32 simultaneously, and an edge-selection signal derived from the TDC delay chain chooses the path furthest away from the metastable region. The ADPLL operates in

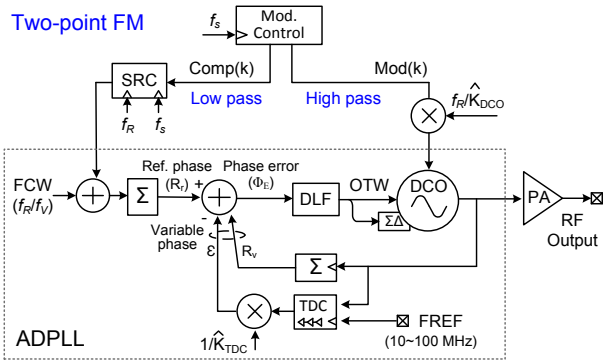


Fig. 1 ADPLL-based FM transmitter.

the synchronous phase domain [10]. The integer part of variable phase signal $R_v[k]$ is determined by counting the number of rising clock transitions of the divided DCO clock (CKV/32). The reference phase $R_r[k]$ is obtained by accumulating FCW with every rising edge of the CKR. The integer, variable-phase $R_v[k]$ together with the fractional correction ε[k], is subtracted from the reference phase $R_r[k]$ in a synchronous arithmetic-phase detector. The ε[k] corrections by means of the TDC increase the instantaneous phase resolution of the system to below the basic 2π radians of the variable phase.

The digital phase error $\Phi_E[k]$ is conditioned by a reconfigurable LF. The LF can be a proportional attenuator α, forming a type-I loop (i.e., one integration due to the DCO frequency-to-phase conversion), which is faster dynamically and is used for fast frequency/phase acquisition during locking process. The LF can also be configured as type II (i.e., one integration in LF) to suppress oscillator noise within the loop bandwidth. Adding a 4$^{th}$-order IIR filter suppresses the TDC and reference noise outside of the loop bandwidth, leading to a lower integrated PN. The LF employs the gearshift [12] technique to minimize the settling time by switching dynamically to type-I mode during frequency acquisition, and operating in type-II mode to keep the phase noise as low as possible in the steady state. Six 8-kbit SRAMs and built-in DCO ($K_{DCO}$) and TDC gain ($K_{TDC}$) calibration circuits are integrated on-chip to enable system debugging, which will be elaborated further in Section IV.

## III. CRITICAL SIGNALS FOR DFT AND DFC

The 60-GHz ADPLL shown in Fig. 2 includes several critical analog/mixed-signal building blocks (i.e., DCO, PA, high frequency divider, and TDC) and many key digital logic blocks (e.g., phase detector, LF, TDC/DCO gain calibration algorithm, two-point FM, etc.) Although the spectrum measured at the RF output (CKV and CKV/32) indicates the PLL performance, it is difficult to

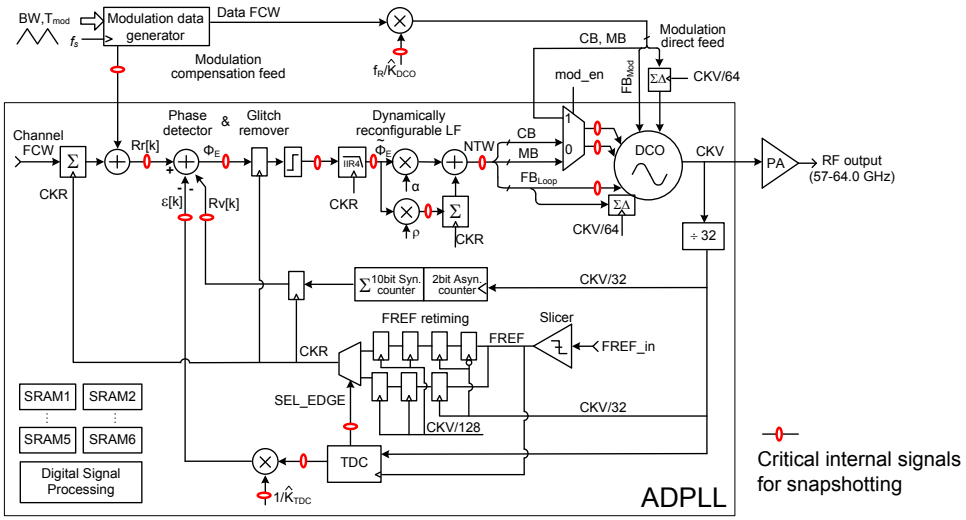


Fig. 2 Block diagram of the 60-GHz ADPLL synthesizer.

locate the source of a problem from an unlocked spectrum or when many spurious tones are observed at the RF output. In these cases, internal digital signals (e.g., raw $\Phi_E$, filtered $\Phi_E$, oscillator tuning word, etc.), clocked at FREF rate, should be monitored.

As shown in Fig. 2, the phase error signal $\Phi_E$ is the numerical difference between the reference and variable phases at the digital output of the phase detector. $\Phi_E$ has a low-pass, unity-gain transfer characteristic to the variable phase at the ADPLL RF output, that is flat up to the PLL bandwidth in type-I or type-II configurations with a large damping factor (e.g., 1) [5]. Therefore, the trajectory of $\Phi_E$ correlates closely with the RF performance measured at the PLL output.

For a type-II PLL $\Phi_E$, or its filtered version, has a zero mean once the loop is locked. Its variance represents the PN at the RF output with adequate accuracy. The trajectory of $\Phi_E$ reveals the transient behavior of the loop, loop stability and frequency response. For example, if there is an unwanted spurious tone in the RF spectrum, the tone frequency and its energy level can be sensed from spectral estimation of the $\Phi_E$ trajectory. For catastrophic errors during the ADPLL operation (e.g., the PLL loses lock), the filtered $\Phi_E$ is no longer flat and its variance exceeds the normal operating bounds.

For two-point FM, the $\Phi_E$ trajectory may be different from the continuous-wave (CW) mode because the modulation data affects the $\Phi_E$ noise characteristics, as depicted in Fig. 3 for triangular modulation. The increased range for the $\Phi_E$ variation indicates greater phase noise in the system, which could be due to the DCO gain calibration accuracy or due to the digital-to-frequency conversion nonlinearity in the DCO modulation bank.

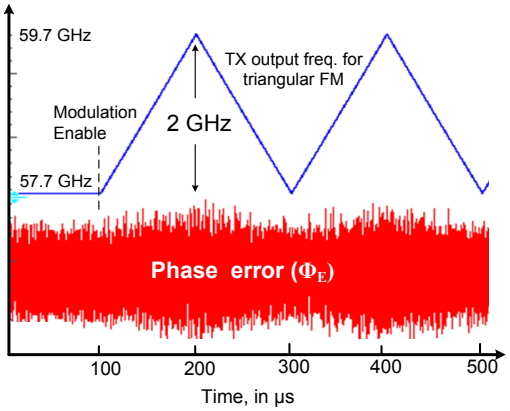


Fig. 3 Simulated $\Phi_E$ for FM applied to the ADPLL.

Besides $\Phi_E$, both integer and fractional part of the variable phase ($R_v$ and $\mathcal{E}$), and reference phase ($R_r$) are informative for debugging, as $\Phi_E[k]=R_r[k]-(R_v[k]+\mathcal{E}[k])$. When tracing fractional spurs, observing $\mathcal{E}[k]$ is more effective. It reflects the periodic behavior in variable phase due to TDC nonlinearities. In addition, other signals along the path from the phase detector to the DCO could also be used for DFT/DFC, such as internal signals in the LF, the scaled-down and filtered version of $\Phi_E$ at the LF output, and the DCO control word (OTW). A frequency deviation in the loop can be ascertained by observing an output of the integral path accumulator when in type-II operation. Alternatively, the output of the IIR filter, which is connected to the $\Phi_E$, could be observed. The OTW can be in a binary form, or an encoded number that matches the DCO interface.

The aforementioned critical internal signals are intrinsically present in any ADPLL, and are highlighted in Fig. 2. Thanks to the digitally intensive nature of the

ADPLL, these signals can be monitored as well as processed on-chip for testing and characterization. The following two Sections describe how the monitoring and on-chip signal processing are performed.

## IV. SNAPSHOTTING INTERNAL SIGNALS FOR DFT AND DFC

Parallel outputs are normally used to monitor internal digital signals in real time. An on-chip mux selects the internal signals of interest for output. The number of test outputs is limited by the available bondpads (e.g., 8 to 16). As the digital signals internal to the ADPLL are clocked at the FREF rate (e.g., 100 MHz), they should be output at the same rate or down-sampled synchronously to ensure signal integrity. Propagating the 8-bit digital signals at 100 MHz rate requires attention to the test circuit board (PCB) design and the use of properly shielded test cables to minimize crosstalk. Moreover, these parallel outputs toggle between 0 and 1, generating switching transients that can be coupled to the sensitive analog nodes on-chip via bondwires or the ESD/pad ring. Consequently, a higher noise floor and increased spurious tone levels are measured at the RF output when the digital test outputs are enabled. In addition, most of the critical internal signals discussed above have more than 8 bits to suppress quantization noise for sufficient data accuracy. Therefore, a 32-bit signal has to be output in 4 successive clock cycles and then reconstructed in a logic analyzer. Furthermore, it is impossible to monitor multiple internal signals simultaneously, which can be very powerful in some cases (e.g., monitoring $R_v$ and $\varepsilon$ to observe misalignment in the fractional and integer paths of the variable phase).

To overcome the aforementioned limitations of the parallel test outputs, we propose to use of on-chip SRAM to take a system snapshot that records one or more internal signals in the time frame of interest. Subsequently, the saved data are read out from SRAM via a serial interface (SPI) and displayed in Matlab™ using a graphical user interface (GUI), as illustrated in Fig. 4. Sharing on-chip SRAM that is used for other (non-conflicting) purposes in an SoC reduces hardware overhead. Consequently, the digital signals and the time frame recorded are selected carefully in order to utilize the limited word depth of SRAMs, and to fulfill debugging needs.

The important digital signals to monitor were discussed in Section III for various scenarios. To specify the proper time frame for recording, we have defined a series of events when the loop is prone to disruptions or even bugs (listed in Table 1) to trigger the snapshot. One (or several) trigger events are selected for monitoring by a control register.

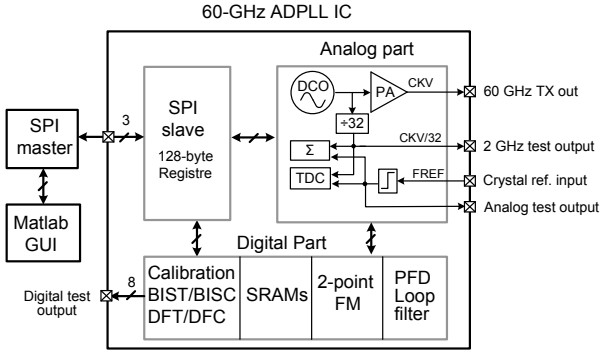


Fig. 4 Block diagram of the 60-GHz ADPLL from a DFT perspective.

Table1: Major trigger events for system snapshots.

| | |
|---|---|
| 1 | System start |
| 2 | LF integral path enable |
| 3 | Dynamically change PLL loop BW |
| 4 | IIR filter enable |
| 5 | DCO gain calibration start/finish |
| 6 | TDC gain calibration start/finish |
| 7 | Loop locks ($\Phi_E$ fall in predefined window) |
| 8 | PLL loses lock |
| 9 | Modulation start |
| 10 | DCO tuning word overflow |
| 11 | Phase error frozen enable |
| 12 | TDC fail flag on |

Some of the events in Table 1 indicate a loop status change and can be enabled intentionally during debugging, such as switching the loop from type I to type II, increasing/decreasing loop bandwidth, or selecting a higher-order IIR filter. Some indicate a different loop operation mode, e.g., enabling DCO/TDC gain calibration, enabling phase error glitch remover, freezing the DCO coarse tuning bank, starting modulation, etc. The remaining events are internal flag signals generated internally (i.e., read only). For example, when no transition edges at the outputs of the inverter chain TDC are detected, the TDC fail flag is set to 1. When the DCO tuning word exceeds its range, an overflow flag turns on. Once the phase error variation exceeds a predefined window, the poor-clock-quality flag is activated. These flag signals report an abnormal status in PLL operation. With the aid of system snapshots triggered by these flags, we are able to not only discover the loop abnormality, but also to infer the cause by examining associated digital signals.

Once the event of interest is triggered (externally/internally), the values of the associated digital signals (can be one, or several) are written into SRAM at a programmable clock rate ($f_{clk\_w}$). Rate $f_{clk\_w}$ normally equals the clock rate of these digital signals (i.e., $f_R$) in order to capture their precise trajectory. In some cases, a down-sampled digital signal stream would be sufficient,

e.g., the filtered $\Phi_E$ after the IIR filter is a slowly varying signal whose trend can be obtained by sampling it at a much lower clock rate (e.g., $f_R/16$). Consequently, a longer time window can be captured with little sacrifice in accuracy of the recorded data. This provides great flexibility to meet varied testing requirements with limited on-chip storage. In this design, sixteen critical internal signals can be monitored. Six SRAMs of $2^{13}$ bits each are used for multi-GHz FMCW generation, and are reused for ADPLL debugging. Clock $f_{clk\_w}$ is programmable from $f_R$ and $f_R/2$ down to $f_R/16$.

The proposed system snapshot can also be configured into different operation modes. *Mode1* saves one digital signal into all SRAMs in sequence to maximize the snapshot depth. *Mode2* can save up to six different signals into six small SRAMs in parallel to observe multiple signals synchronously. *Mode3* stops saving data when the SRAMs are full, to capture the short moment when the trigger is enabled. *Mode4* saves data to SRAM cyclically until triggered by the specified event to freeze the moment just before the event happens. In this work, a precise $\Phi_E$ (32 bit) trajectory up to 40 µs long can be captured (sampled at $f_R$) when all 6 SRAMs are used, which is sufficient for debugging purposes.

Fig. 5 shows a snapshot of $\Phi_E$ samples at the LF output (i.e., NTW in Fig. 2) triggered by a loop BW change during verification. It captures the transient behavior of the PLL when the loop BW is dynamically decreased from 1.2 MHz to 300 kHz. The rms of NTW is proportional to the loop BW, and is thus reduced by a factor of 4, as expected, which implies improved integrated PN at the RF output.

## V. PERFORMANCE-BASED BIST AND BISC

We use two categories of tests: structural based and functional performance based. While the former is used for block-level design verification and defect tests, the latter is used for process, voltage, and temperature (PVT) characterization.

### *A. DCO tuning step analyzer*

The digitally controlled oscillator (DCO) is tuned by a digital command word (i.e., OTW in Fig. 1). A simplified mm-wave DCO schematic is shown in Fig. 6(a), which consists of 3 capacitor tuning banks of progressively finer step-size to realize fine resolution and a wide tuning range simultaneously [13]. The switched-capacitor array represents a digital-to-analog conversion function. Mismatches cause distortions in the DCO's frequency tracking and modulation.

For the 60-GHz FMCW transmitter designed in this work, frequency modulation traverses 3 tuning banks (i.e., coarse-, mid-coarse-, and fine-bank) to obtain the desired

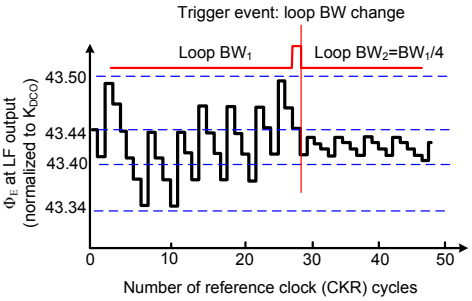


Fig. 5 Captured filtered digital phase error samples at LF output for dynamic loop bandwidth change.

GHz modulation range. The tuning step (i.e., DCO gain, $K_{DCO}$) mismatch within each unit-weighted bank, and the $K_{DCO}$ ratio between different banks affect the transmit spectrum and modulation distortion (see Fig. 6(b)). It is important to establish the tolerable extent for these mismatches in the design phase, and to verify that it is not exceeded by fabricated SoCs.

It should be emphasized that it is extremely difficult and time consuming to measure a free-running, mm-wave (e.g., 60 GHz) DCO's tuning step mismatch for the targeted accuracy, even with the aid of specialized test equipment. For a fine-tuning bank (FB) $K_{DCO}$ of ~1 MHz and 5% mismatch, the frequency difference is just 50 kHz at the 60-GHz carrier. Tremendous efforts are required to stabilize the free-running DCO and to reduce thermal noise in the test setup (e.g., noise of a harmonic mixer should be avoided).

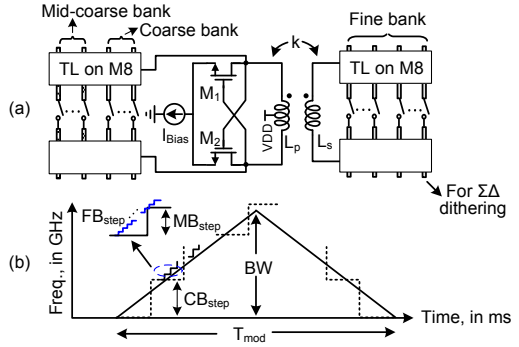


Fig. 6 (a) a simplified mm-wave DCO and (b) linear FM employing multiple DCO tuning banks.

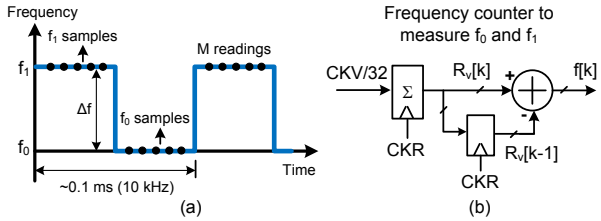


Fig. 7 DCO tuning step analyzer: (a) DCO output frequency when toggled by a single bit; (b) on-chip frequency counter.

Fortunately, the built-in self characterization (BISC) technique extracts the accurate tuning characteristic of the DCO without external resources. The $K_{DCO}$ for each tuning bit is characterized open-loop by forced ON/OFF toggling of individual digital bits [7]. Consequently, the DCO output is toggled between $f_1$ (control bit ON) and $f_0$ (control bit OFF), as shown in Fig. 7(a). The $K_{DCO}$ for this control bit is simply $\Delta f$, which is evaluated by subtracting frequency measurements performed at each of the two states. The open-loop configuration is used because each toggling procedure addresses a specific fine-tuning bit, and could not be done through the normal modulation capability of the ADPLL.

Frequency measurements are made using a counter within the ADPLL, as shown in Fig. 7(b). The frequency is measured by counting the variable phase change in one FREF cycle (i.e., f[k]=Rv[k]-Rv[k-1]). Multiple readings of the counter (e.g., M readings) are averaged to reduce the quantization error in a single measurement of the frequency deviation, especially in the presence of DCO phase noise. The tuning step ($f_i$) for particular control bit '$i$' is calculated by $\Delta f_i = \frac{1}{M}\left(\sum_{k=1}^{M} f_1[k] - \sum_{k=1}^{M} f_0[k]\right)$. The number of measurements ($N$) is typically on the order of $2^{15}$ for 1% fine-tuning step accuracy. The frequency tuning step after averaging is $\Delta f_{avg,i} = \frac{1}{N}\sum_{i=1}^{N} \Delta f_i$. Thus, the normalized tuning step mismatch of this bit is $e = (\Delta f_{avg,i} - \Delta f_{FB})/\Delta f_{FB}$, where $\Delta f_{FB}$ is the average $K_{DCO}$ of the fine-tuning bank. The parameter $\Delta f_{FB}$ is obtained by a closed-loop digital normalization algorithm that measures the phase error present in the loop [10].

The above technique can also be applied to characterize mismatch of the ΣΔ dithering bit in FB (see Fig. 6) with respect to the average $K_{DCO}$ of the integer bits in FB. BISC results are compared to the simulation data for block-level design verification. In addition, they can be compared to statistically chosen thresholds on-chip for defect detection. Furthermore, a 'self-healing' capability can be implemented based on the BISC outcomes. For example, an on-chip lookup table can be built based on the BISC results, and used to pre-distort the modulation data in order to compensate the mismatch and retrieve adequate linearity [11].

### *B. Built-in phase error ($\Phi_E$) analyzer*

As explained in Section III, the performance at the RF output can be determined with adequate accuracy by observing an internal digital signal $\Phi_E$, which is sampled at the much lower rate of $f_R$. The filtered output of the phase detector (or its raw version) is sufficient to indicate several parameters of interest in the RF output signal, such as frequency error, phase noise at lower frequency offsets, integrated phase noise, and rms phase trajectory error upon modulation. System snapshotting described in Section IV stores the $\Phi_E$ trajectory into on-chip SRAM for the time frame of interest, providing valuable data for bug identification. For performance testing of mass-produced ICs, on-chip digital signal processing $\Phi_E$ is desirable, which generates flags that characterize the performance of the RF output.

A simple phase error analyzer is implemented in the 60-GHz ADPLL IC, as shown in Fig. 8. The raw phase error $\Phi_E$ is compared with its sample at the previous clock cycle, which represents the phase error change ($\Delta\Phi_E$) in one FREF cycle, or the frequency error ($f_E$) in the loop. Once the PLL is locked, the $f_E$ is zero with small quantization noise. Thus, the quality of the synthesized clock can be monitored by constantly comparing $f_E$ with a programmable threshold. If $f_E$ exceeds a large threshold for a number of FREF cycles (controlled by the counter in Fig. 8), the loop has likely lost lock, since large frequency error due to an unwanted incidental disturbance would not have lasted that long. Thus, a simple clock quality monitor is realized.

Besides the unlock indicator, the same logic can be reused to detect potential glitches in $\Phi_E$ generation. As illustrated in Fig.2, the integer part of the variable phase ($R_v$) is determined by counting the number of rising clock transitions of CKV/32, while the fractional part is obtained by a TDC based on a pseudo-differential delay chain [14]. Sampling of the accumulator value might not coincide with those of TDC. These different sampling moments could have a timing misalignment, and cause glitches in the phase error when the counter and TDC outputs are combined. These glitches can be detected by comparing $f_E$ with a proper threshold (e.g., 0.5, much smaller than the threshold for the unlock detect). If $f_E$(k) is larger than 0.5, the input is assumed to contain a glitch. The $\Phi_E$ is then frozen for this clock cycle by simply disregarding the current phase error to obtain a glitch-free output (see Fig. 8).

The phase error analyzer can be further extended to estimate the PLL's in-band PN, the DCO's PN (at a narrow loop BW configuration, e.g., 10 kHz), and modulation noise in a transmitter with the aid of an on-chip stream processor [5][6].

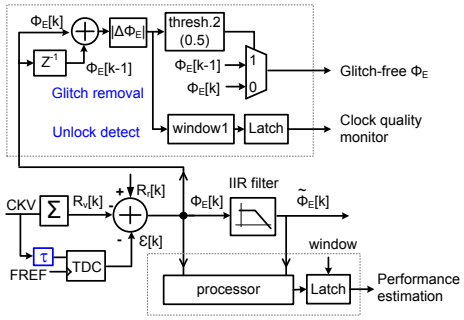


Fig. 8 Phase error analyzer logic.

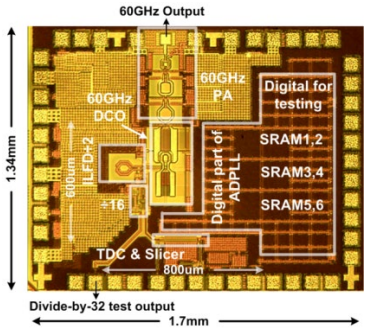


Fig. 9 Die micrograph of the 60-GHz ADPLL Tx.

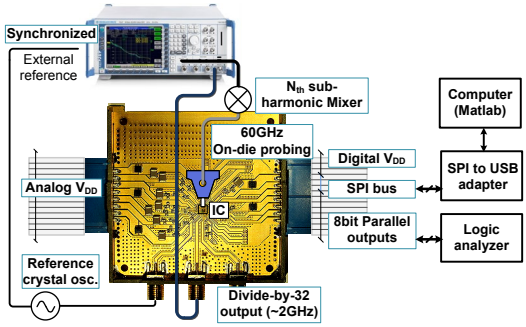


Fig. 10 Test setup for the 60-GHz ADPLL-based Tx.

## VI. Measurement Setup and Results

The DFT and DFC techniques discussed in this paper have been realized as part of the 60-GHz ADPLL-based FMCW transmitter (Tx) implemented in TSMC 65-nm bulk CMOS. The chip, described in [11], is shown in Fig. 9. The ADPLL core occupies 0.5 $mm^2$ of the 2.2-$mm^2$ total die area, including bondpads, power amplifier, SRAMs (6x8-kbit), and other digital circuitry for debugging. SRAMs store the DCO gain calibration data for the GHz range, linear FM sweeping, and are re-used to take system snapshot during debugging as described in Section IV. The measurement setup is depicted in Fig. 10. The IC is wirebonded to a PCB for DC and low-frequency connectivity, while the 60-GHz PA output is probed on die. A divide-by-32 test output provides a convenient way to monitor the 60-GHz ADPLL output without on-die probing. The 8-bit digital test outputs are captured in parallel via a logic analyzer.

The 60-GHz ADPLL IC supports 3 major test modes: open-loop test, closed-loop CW-mode test, and the frequency modulation test. In open-loop testing, the DCO, divider, reference slicer, and TDC are powered on gradually for DC and AC functionality check to ensure that the variable (CKV) and resampled reference (CKR) clocks are available to the digital part. The DCO tuning step mismatches are then characterized.

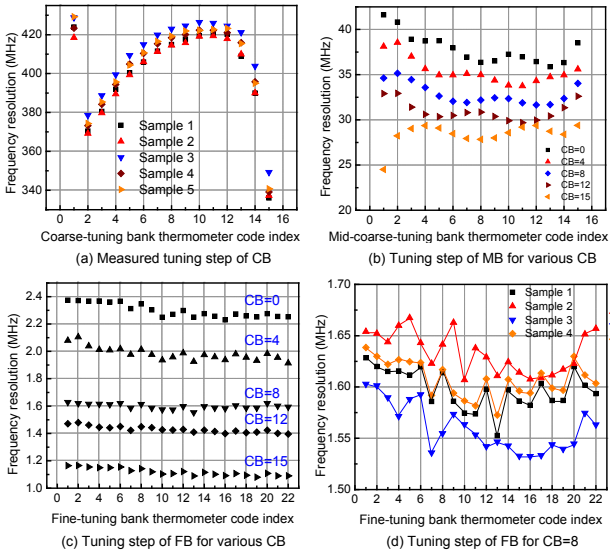


Fig. 11 Measured $K_{DCO}$ for coarse-, mid-coarse-, and fine-tuning banks (CB, MB, and FB).

To achieve 7-GHz tuning range and a raw resolution of ~1 MHz, the 60-GHz DCO employs 3 switched-metal capacitor banks distributed across a transformer coupled resonator [13]. The $K_{DCO}$ for each bank measured via the BISC technique described in Section V-A is plotted in Fig. 11. The digital-to-frequency conversion linearity of the FB measured for 4 IC samples is shown in Fig. 11(d). A measurement accuracy of 1 kHz is achieved via on-chip averaging.

In the closed-loop test, a system snapshot and the parallel digital test outputs are used to monitor important internal signals for troubleshooting. Moreover, a TDC self-test is conducted via the build-in TDC gain (i.e., TDC resolution) calibration algorithm reported in [14].

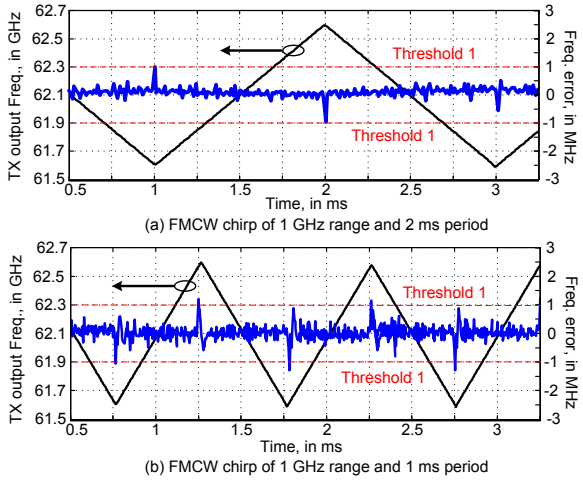


Fig. 12 Measured Tx output frequency and its error from ideal for an FMCW chirp.

The measured FMCW transmitter performance is depicted in Fig. 12 for a 1-GHz modulation range centered at 62.1 GHz with varied chirp slopes. The transmitter output frequency can be measured internally via the frequency counter at the divide-by-32 output. It is evaluated against the ideal FM trajectory to obtain the instantaneous frequency error (plotted in Fig. 12). The FMCW transmitter performance is determined using the build-in phase/frequency error analyzer, and without RF probing of the 60-GHz output. Moreover, the rms frequency error is obtained with the aid of a stream processor. Both the rms and instantaneous frequency error could be further evaluated against statistically chosen thresholds (e.g., threshold 1 in Fig. 12) in production testing.

## VII. Conclusions

Design-for-test (DFT) and design-for-characterization (DFC) techniques for a 60-GHz all-digital PLL based FMCW transmitter IC were discussed and demonstrated. The digitally intensive architecture facilitates built-in self testing (BIST) and self characterization (BISC) with little hardware overhead by monitoring and storing internal digital signals in SRAM, and with the aid of digital signal processing. Snapshotting of key internal signals captures the loop transient behavior at the time frame of interest, providing valuable data for debugging. Phase error and DCO tuning step analyzers were used to characterize RF performance without employing external resources. Measured performance metrics can be evaluated against statistically chosen thresholds in production testing. The proposed techniques could also be applied to other digitally intensive PLLs to save test time and cost.

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