Development of GaN Monolithic Integrated Circuits for Power Conversion

Yung C. Liang[1,2], Ruize Sun[1,2], Yee-Chia Yeo[1]
[1] National University of Singapore, Singapore
[2] National University of Singapore (Suzhou) Research Institute, China
E-mail: chii @ nus.edu.sg

Cezhou Zhao[3]
[3] Xi'an Jiaotong-Liverpool University, China

***Abstract*— This paper describes the development of a viable platform for the design of full GaN (Gallium Nitride) monolithic integrated circuits for power conversion applications. The Normally-on and normally-off AlGaN/GaN power HEMT devices are used for the integrated circuit design using the ADS (Advanced Design System) tool. A monolithic switched-mode DC-DC buck converter with integrated functional blocks and over-current protection is used to showcase the suitability of the development. The designed GaN power integrated circuit was fully fabricated and tested to verify its functionality in power conversion.**

Keywords—GaN Integrated Circuit, Power Integrated Circuit

I. Introduction

The development of wide bandgap devices has advanced the technology in power energy conversion. Particularly owing to the superior properties of GaN material and the polarisation effect in AlGaN/GaN heterostructure, GaN based power devices become a superior candidate used in power conversion. For an identical blocking voltage rating, GaN High Electron Mobility Transistors (HEMTs) have lower on-resistance and gate-drain capacitance for higher switching frequency operations. They have shown potential to surpass the performance of Si based power devices and are more cost-effective than the SiC counterparts [1, 2].

By the year of 2008, works had reported high efficiency power electronic converters using discrete normally-on GaN HEMTs as the main switches [3-6]. Later, the discrete normally-off power HEMTs were introduced for a better control and safety [7-9] in 2011. With the help of continuous development of discrete normally-off GaN HEMTs and commercialisation, power converters using GaN HEMT modules such as half or full bridge topology [10-15] are available for higher power rating and reduced cost. In these works, the integration is limited on the main switches. To further utilise the advances in GaN based integrated circuits among the main switches, control circuits and other passive components, a full integration is required. At the same time, the on-chip controlling, monitoring and protecting circuits can increase its functionality and reliability. Previously, the design of Monolithic Microwave Integrated Circuit (MMIC) [16] were adopted for such a development, which focus on normally-on GaN HEMT integration process. With the advent of several technologies enabling normally-off operations, GaN integration circuits with normally-off HEMTs were introduced and fabricated [17-20]. Analogue circuits such as comparators [21], voltage referencing, and temperature sensing [22] were individually realised using GaN HEMTs and NMOS logic. However, so far there is still a lack of studies on the systematic and full integration of main switches, gate drivers, protection and feedback control circuits, all based on the GaN MIS-HEMT platform for power conversion application. In this paper, we proposed the Au-free all-GaN MIS-HEMT power integrated circuit platform. Through the platform, a constant-output-ripple DC-DC buck converter with integrated gate driver, pulse width modulation (PWM) feedback control and over-current protection circuits was realised, fabricated and verified by laboratory measurements.

II. All-GaN Power Integrated Circuits Platform

The schematic cross sections of the GaN power HEMTs and Schottky diode used for the development are shown in Fig. 1. The platform is targeted at CMOS-compatible fabrication for all-GaN power electronic converters. It features Au-free metal contacts, normally-off gate partial/full recess process, MIS gate structure and the embedded current sensing structure. The AlGaN/GaN epitaxy consists of 4.2-μm GaN buffer on Si substrate, 1.6-μm undoped GaN, 20-nm $Al_{0.25}Ga_{0.75}N$ and 1-nm GaN cap. The measured electron mobility and sheet carrier concentration are 1627 cm^2/Vs and 0.93×10^{13} cm^{-2} respectively.

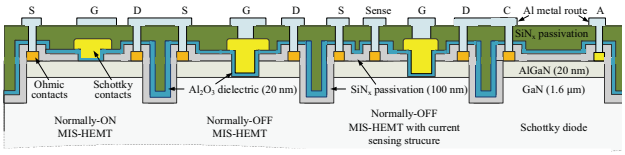

Fig. 1 Cross section of GaN power HEMT and Schottky diode

A. Au-free metal contacts

The Au-free metal schemes of Ti/Al/TiN (25/125/50 nm) and Ni/TiN (100/50 nm) are used in ohmic contact and gate electrodes respectively for a CMOS-compatible platform. Owing to the hardness of TiN cap layer, a smoother surface morphology can be realised for good metal ohmic contacts.

B. Gate recess process

Normally-off HEMTs can be made by AlGaN barrier layer recess based on multiple cycles of O_2 plasma oxidation and dilute hydrochloric acid rinse deoxidation. This can be done for partial or full AlGaN recess. If for full recess of 19 nm, a total

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of 35 cycles of treatments is needed with 2 nm barrier to preserve the AlGaN/GaN interface mobility. For partial recess, fluorine ions can be placed through RIE (Reactive Ion Etching) process during the deposition of Al_2O_3 gate dielectric to enhance the positive gate threshold voltage.

C. Embedded current sensing structure

For control function and device over-current protection, an embedded current sensor is essential. A floating ohmic contact current sensing electrode is added between source and gate electrodes. The voltage at the sensor electrode can be used for converter feedback control, which constitutes as a key element in the whole feedback control loop.

Fig.2(a) shows a schematic cross-section of the normally-off MIS-HEMT with current sensor. The MIS-HEMT utilizes partial AlGaN recess and fluorinated Al_2O_3 dielectric to achieve +5 V threshold voltage. Figure 2(b) shows both the measured and ADS simulated static I-V characteristics of MIS-HEMTs. Fig.3 illustrates the measured and simulated transient switching waveforms. They are closely matched by the ADS simulations. This confirms the MIS-HEMT models used in ADS simulation. The full-GaN DC-DC converter can then be designed based on the models identified.

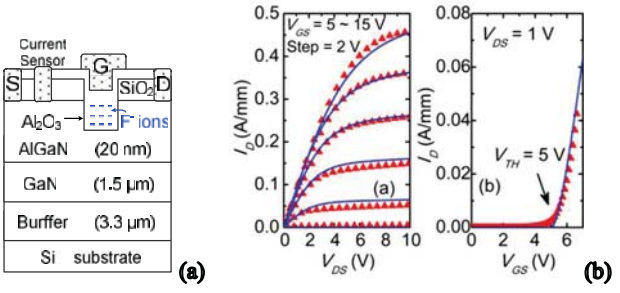

Fig. 2. (a) Schematic cross-section of the normally-off AlGaN/GaN MIS-HEMT with embedded current sensor; (b) The matching of static I-V curves between device measurement (points) and ADS simulation

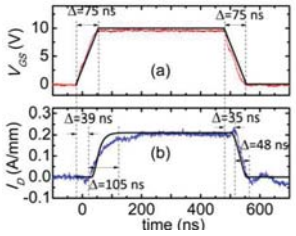

Fig. 3. Transient switching waveforms of V_{GS} and I_D of the MIS-HEMT between measurement (red/blue) and ADS simulation (black).

III. All GaN DC-DC Power Converter

In order to demonstarte the functionality and feasibility of the proposed GaN power integrated circuits platform, an all-GaN integrated DC-DC buck converter was designed on the ADS platform, later fabricated and measured as a test case. For the power conversion application, constant and low output voltage ripple is preferred. In this design, we set the output voltage between two levels, which then determine the peak-to-peak ripple voltage. The control circuit swings between two duty cycles, where a higher duty cycle will bring up the output voltage and a lower duty cycle reduces the output voltage.

The design integrates gate driver, pulse width modulation (PWM) feedback control and over-current protection functional blocks. The specific design objectives include: (a) output voltage is set at 10.0 V and input line voltage range should cover 15 to 30 V; (b) output ripple voltage is at 5%; (c) the converter should be able to maintain stable output with constant ripples against variations in input line voltage or load conditions; (d) the converter should be able to respond to over-current incident according to the pre-set threshold and shuts down within one duty cycle. The circuit diagram of the overall converter integrated circuit design is shown in Fig. 4, which includes four major parts, namely buck converter, high-side gate driver, pulse-width-modulation (PWM) feedback controller and over-current protection (OCP) blocks.

A. Buck converter

The DC-DC buck converter block includes the main MIS-HEMT switch S_0 with integrated current sensor, GaN Schottky barrier diode D_O, inductor L_O, capacitor C_O and load R_O. The converter operates in the continuous current mode (CCM) for normal operation.

B. Gate driver

In the buck converter configuration, the power switch is situated at high-side, which requires a non-ground-referenced control signal to ensure gate over-drive. Hence a high-side gate driver is required for high-side S_0 through the bootstrap scheme. As shown in Fig. 4, the gate driver design includes stages of level shifter (normally-off S_1 and normally-on S_2), two inverters (normally-off S_3/S_5 and normally-on S_4/S_6) and buffer (normally-off S_7/S_8) stages with bootstrap capacitor (C_{bt}) and diode (D_{bt}).

The level shifter is the link between the high-side driver and the ground referenced control signal V_C. The inverter stages invert the level shifter stage output V_1 to V_2 and V_3 to drive HEMTs S_7 and S_8 for charging and discharging of the main switch S_0. The bootstrap capacitor C_{bt} and diode D_{bt} are other core components in the bootstrap power supply, which has the advantage of being simple and low cost. The operation mechanism of bootstrap power supply can be explained with the help of the solid-line shades and dashed-line shades in Fig. 4. When control signal V_C is at high value, S_8 is turned on and the gate capacitor of S_0 is charged by C_{bt} through the solid line shades, thus the converter is turned on; when V_C is at low value, S7 is turned on and the gate capacitor of S_0 is discharged through the dashed-lines shade. C_{bt} is charged to V_{DC} every time when becomes non-conductive. C_{bt} holds the charge and bootstraps Vg to be $V_{DC}+V_S$ for high-side drive.

C. PWM Feedback Control

It is essential for a DC-DC converter to have a control topology to maintain output stability against input voltage and load variations. Here we design and integrate the control-signal generating unit and feedback circuit to realize a PWM feedback control. As shown in Fig. 4, the block includes two major parts: PWM signal generator and feedback controller.

The PWM signal generator can generate square wave PWM signal of varying pulse width. It includes a hysteresis comparator (S_{16}-S_{20}, R_1, R_{FB}), a sawtooth unit (S_{21}, S_{22}, C_{SAW}) and a comparator (S_{21}-S_{25}). The output of the hysteresis comparator is applied to the gate of S_{21}. When S_{21} is off, C_{SAW} is charged to V_{DC} through S_{22}. When S_{21} is on, C_{SAW} is discharged through S_{21}. The respective device layout widths of S_{21} and S_{22} determine the charging and discharging rate of C_{SAW}. When connecting the source electrode of S_{22} back to the input of the hysteresis comparator, the formed close-loop generates sawtooth oscillation signal of V_{SAW}. Then V_{SAW} is compared to a feedback reference signal V_{fb} at PWM comparator, resulting in the generation of PWM signal of V_C.

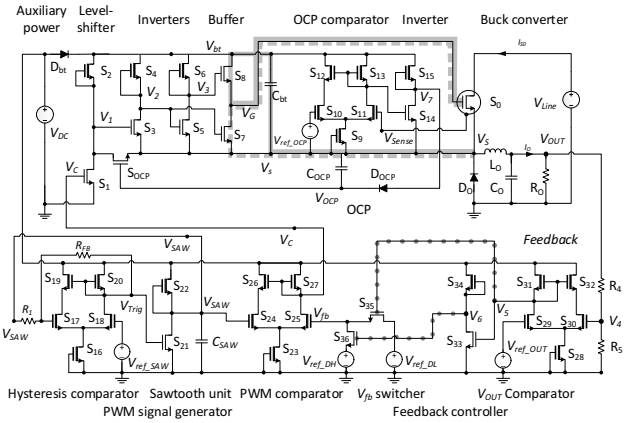

Fig. 4 Circuit diagram of the designed all-GaN integrated DC-DC buck converter with gate driver, PWM feedback controller and over-current protection.

The feedback controller uses the reference signal V_{fb} to modulate the pulse width of V_C accordingly. It includes V_{OUT} comparator (S_{28}-S_{32}, R_4, R_5) and V_{fb} switcher (S_{34}-S_{36}). V_{OUT} is fed back to the input of V_{OUT} comparator via a resistor divider (R_4 and R_5). The comparator output V_5 and inverter output V_6 have opposite polarities and are applied to S_{35} and S_{36} in V_{fb} switcher through the dotted paths in Fig. 4. When $V_4 < V_{ref\_OUT}$, V_5 is at low output and V_6 is at high output. S_{36} is turned on and $V_{fb} = V_{ref\_DH}$, which is set for the desired high duty cycle DH to bring up the output; or else when $V_4 > V_{ref\_OUT}$, S_{35} is turned on and $V_{fb} = V_{ref\_DL}$, which is set for a lower duty cycle DL to bring down the output voltage. Together with the PWM signal generator circuit, this feedback controller can manipulate the duty cycle of the main switch to maintain stable converter output voltage within a fixed band.

D. Over-current Protection

The converter is to be protected under over-current incident. The over-current protection (OCP) block includes the comparator (S_9-S_{13}), inverter (S_{14} and S_{15}), capacitor (C_{OCP}), diode (D_{OCP}) and normally-off S_{OCP}. The V_{Sense} signal is from the HEMT current sensing terminal. When $V_{sense} > V_{ref\_OCP}$ under over-current incident, V_{OCP} will rise beyond the threshold voltage of S_{OCP}. When S_{OCP} is turned on, the level-shifter is bypassed, causing the high-side driver and converter to be shut down.

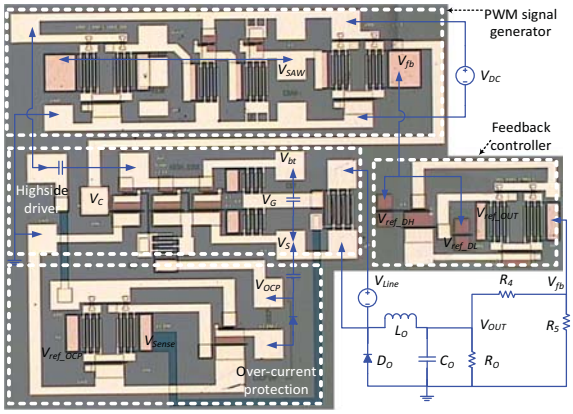

Fig. 5 Optical image of the fabricated all-GaN integrated DC-DC buck converter. The function blocks are labelled and marked by dashed line box. The off-chip passive components, external

The starting 6-inch AlGaN/GaN on silicon epitaxy wafer was obtained from a commercial vendor. The fabrication process started with the mesa isolation, then Ti/Al/TiN Au-free ohmic contacts were formed and annealed at 800°C for 45s in N_2 ambient. Then 50-nm SiN_x was deposited as passivation. After gate opening and recess, 20-nm Al2O3 gate dielectric was formed by atomic layer deposition. Ni/TiN was evaporated as gate metal then Al formed the pads and metal routes. The fabricated GaN power integrated circuit is shown in Fig. 5 where all the functional blocks and external circuits are labelled on the fabricated die.

IV. Laboratory Measurements

A. Normal operation

The fabricated prototype was measured in normal operation with different input line voltages at 10 kHz switching frequency. The inductor L_O of 193 mH and capacitor C_O of 10 µF are off-chip due to their large values. The resistive load R_{OUT} is 500 Ω. The V_{ref_DH} and V_{ref_DL} are set at 3.5 V and 6.8 V to generate corresponding duty cycles DL and DH of 30.2% and 70.1%. The V_{Line} is varied from 16 V to 29 V. Below shows the normal output waveforms with V_{Line} of 16 and 29 V to verify the operations.

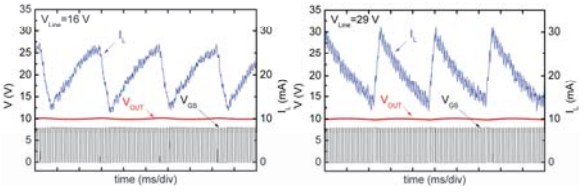

Fig. 6 Waveforms of output voltage (red), inductor current (blue) and main switch gate voltage (black) at input voltage of 16 V and 29 V.

The mismatch between the designed and measured V_{OUT} values is less than ±1.69%, indicating good accordance between the design and laboratory measurement.

B. Line voltage variations

The converter could be subjective to abrupt input line voltage variation. The designed feedback scheme should maintain a stable output under all the variations. Here the input voltage is abruptly switched from 20V to 16V (step down) and from 20V to 28V (step up). The transient responses from measurement are shown below. The converter responses well with the input voltage changes.

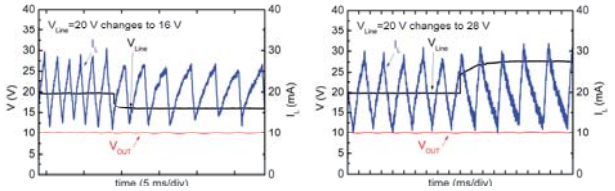

Fig.7 Transient response waveforms of input voltage (black), output voltage (red), and inductor current (blue) with abrupt variations of input voltage

C. *Load variations*

The load resistor is abruptly changed from 500Ω to 300Ω and then abruptly changed back. The transient responses of the fabricated prototype are shown below. The converter reacts well with the load changes.

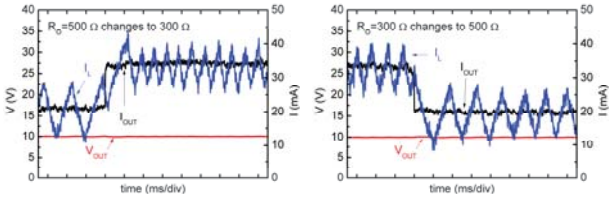

Fig.8 Transient waveforms of load current(black), output voltage (red) and inductor current (blue) under load changes.

D. *Over-current protection*

When the load is at fault, the over-current incident can happen, and the designed over-current protection circuit will be activated to shut down the main switch. Fig.9 shows the measurement of the over-current protection at 180 mA load current thresholds. The protection reacts instantly to shut down the main switch current. The load current decays for a few milli-seconds due to the output capacitor discharge.

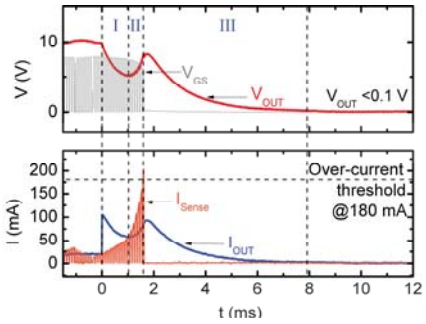

Fig. 9 Transient waveforms of converter main switch current (lower red), output voltage (upper red), gate voltage (black) and load current (blue) under over-current protection.

V. Conclusion

A full-GaN monolithic IC design platform was developed based on normally-on and normally-off AlGaN/GaN HEMT device technologies. A DC-DC integrated converter was designed, fabricated and measured in laboratory to showcase the design platform. The development enables all-GaN based power integrated circuits for energy conversion.

References

[1] R. S. Pengelly, et al., "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," IEEE Trans on Microwave Theory and Techniques, vol. 60, pp. 1764-1783, Jun 2012.

[2] D. Kinzer and S. Oliver, "Monolithic HV GaN Power ICs: Performance and application," IEEE Power Electronics Magazine, vol. 3, pp. 14-21, 2016.

[3] Y. Gao and A. Q. Huang, "Feasibility Study of AlGaN/GaN HEMT for Multi-megahertz DC/DC Converter Applications," in CES/IEEE 5th International PEMC Conference, 2006, pp. 1-3.

[4] W. Saito, et al., "A 120-W Boost Converter Operation Using a High-Voltage GaN-HEMT," IEEE Electron Device Letters, vol. 29, pp. 8-10, 2008.

[5] W. Saito, et al., "Current collapseless high-voltage GaN-HEMT and its 50-W boost converter operation," in IEEE International Electron Devices Meeting, 2007, pp. 869-872.

[6] Y. Wu, M. et al., "A 97.8% efficient GaN HEMT boost converter with 300-W output power at 1 MHz," IEEE EDL, vol. 29, pp. 824-826, 2008.

[7] K. Boutros, et al., "Normally-off 5A/1100V GaN-on-silicon device for high voltage applications," in IEEE IEDM, 2009, pp. 1-3.

[8] M. Acanski, J. Popovic-Gerber, and J. A. Ferreira, "Comparison of Si and GaN power devices used in PV module integrated converters," in IEEE Energy Conversion Congress and Exposition, 2011, pp. 1217-1223.

[9] J. Das, et al., "A 96% efficient high-frequency DC–DC converter using E-mode GaN DHFETs on Si," IEEE EDL, vol. 32, pp. 1370-1372, 2011.

[10] B. Hughes, et al., "GaN HFET switching characteristics at 350V/20A and synchronous boost converter performance at 1MHz," in Twenty-Seventh Annual IEEE APEC, 2012, pp. 2506-2508.

[11] R. Mitova, et al., "Investigations of 600-V GaN HEMT and GaN diode for power converter applications," IEEE Trans on Power Electronics, vol. 29, pp. 2441-2452, 2014.

[12] Y.-F. Wu, et al., "kV-class GaN-on-Si HEMTs enabling 99% efficiency converter at 800 V and 100 kHz," IEEE Trans on Power Electronics, vol. 29, pp. 2634-2637, 2014.

[13] D. Reusch, J. Strydom, and A. Lidow, "A new family of GaN transistors for highly efficient high frequency DC-DC converters," in IEEE APEC, 2015, pp. 1979-1985.

[14] S. Ujita, et al., "A Compact GaN-based DC-DC Converter IC with High-Speed Gate Drivers Enabling High Efficiencies," IEEE 26th ISPSD, pp. 51-54, 2014.

[15] R. Ramachandran and M. Nymand, "A 98.8% efficient bidirectional full-bridge isolated dc-dc GaN converter," in 2016 IEEE APEC, pp. 609-614.

[16] S. Singhal, et al., "GaN-On-Si Reliability: A Comparative Study Between Process Platforms," in ROCS Workshop 2006, pp. 21-24.

[17] K. J. Chen, "GaN smart power chip technology," in 2009 IEEE International Conference of Electron Devices and Solid-State Circuits, 2009, pp. 403-407.

[18] W. Saito, et al., "Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications," IEEE Trans on Electron Devices, vol. 53, pp. 356-362, 2006.

[19] D. Kinzer, "GaN power IC technology: Past, present, and future," in 2017 29th ISPSD, 2017, pp. 19-24.

[20] N. Otsuka, Y. Kawai, and S. Nagai, "Recent progress in GaN devices for power and integrated circuit," in 2017 IEEE 12th ASICON, 2017, pp. 928-931.

[21] X. Liu and K. J. Chen, "GaN Single-Polarity Power Supply Bootstrapped Comparator for High-Temperature Electronics," IEEE EDL, vol. 32, pp. 27-29, 2011.

[22] A. M. H. Kwan, G. Yue, L. Xiaosen, and K. J. Chen, "A Highly Linear Integrated Temperature Sensor on a GaN Smart Power IC Platform," IEEE Trans on Electron Devices, vol. 61, pp. 2970-2976, 2014.