Clocked Comparator for High-Speed Applications in 65nm Technology

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Abstract—**This paper presents a design for an on-chip high-speed clocked-comparator for high frequency signal digitization. The comparator consists of two stages, amplification and regenerative, comprising a total of 10 MOS transistors. The design is implemented in 65nm CMOS technology. Also, the paper presents a new cost effective technique for measuring the maximum speed of the clocked comparator. The measurement and simulation results show that the proposed design has an average of 31% higher speed and ~17% less active area than the conventional design.**

I. Introduction

Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications such as on-chip high frequency signal testing, data links, sense amplifiers and analog-to-digital converters. On-chip testing of high frequency pseudo random binary sequences (PRBS) requires a high speed comparator at the electrical interface stage [1], [2].

A clocked comparator usually consists of two stages. The first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In low power target designs, the regenerative stage starts its operation from supply level [3], [4], or ground level [5], [6]. In a CMOS-based latch, the regenerative stage and its following stages consume the lowest possible static power since the power-ground path is switched off either by a NMOS or PMOS transistor.

The comparator speed is not the highest priority however, because the latch evaluates to its stable state starting from the opposite state. If comparator speed is a priority, the regenerative stage could be designed to start its operation from midway between power supply and ground, for example, as it is implemented in [7]. However, the static power consumption is relatively high. In [5], Schinkle presented a double-tail latch-type voltage sense amplifier. The circuit is developed to work in the scaled technology by stacking a lower number of transistors compared with the conventional sense amplifier [8]. A modified version of the design in [5] is developed in [9] to calibrate the voltage offset due to process variations.

Comparator design largely depends on the target application. In this paper, we present a design for an on-chip high-speed clocked comparator for high-frequency low-swing signal test applications. The comparator is attractive for the applications where speed is of the highest priority and the common mode range is limited, for examples, testing of on-chip high frequency signals, high-speed data link and ADCs of moderate number of bits. In addition, a cost-effective technique is presented for measuring the highest possible clock frequency that can be applied to the comparator while keeping correct operation.

The rest of the paper is organized as follows. The speed limitations of the conventional design and areas for improvements are investigated in Section II. An overview of the proposed design is given in Section III. The simulation results and comparisons are given in Section IV. The prototype chip and test results are covered in Section V.

II. Delay Time in Conventional Comparators

The schematic diagram of the comparator presented in [5] is shown in Fig. 1. This comparator is selected for comparison with our design because of its speed and suitability for low supply voltage applications. In the rest of the paper it will be referred to as reference comparator. The transient behavior of this type of comparators is shown in Fig. 2 assuming that V_P is higher than V_N. While the clock is *low*, the output nodes (OUT+ and OUT-) are discharged to ground. When the clock switches to *high*, the currents flowing in M3 and M4 charge the output nodes at different rates depending on the values of input voltages V_N, V_P. When one of the output voltages reaches the threshold voltage V_{thn} of the NMOS, a feedback operations starts and the two outputs eventually evaluate to V_{DD} and ground.

The delay time can be calculated as the time difference between 50% levels of clock and output shown in Fig. 2(a). According to the analysis given in [10], the delay time t_{delay} can be divided into two parts namely t_0 and t_{latch}, where t_o and t_{latch} can be given by Equations (1) and (2) respectively.

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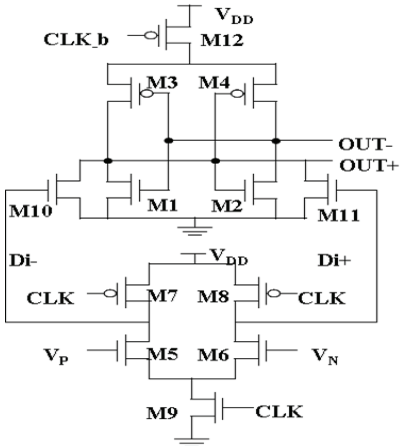

Figure 1. A conventional comparator [5].

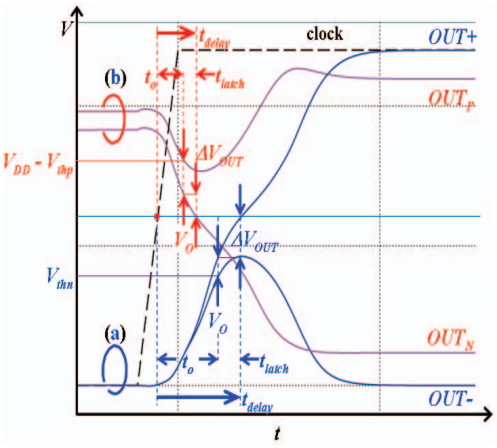

Figure 2. Transient behavior of (a) conventional design [5] (b) proposed design.

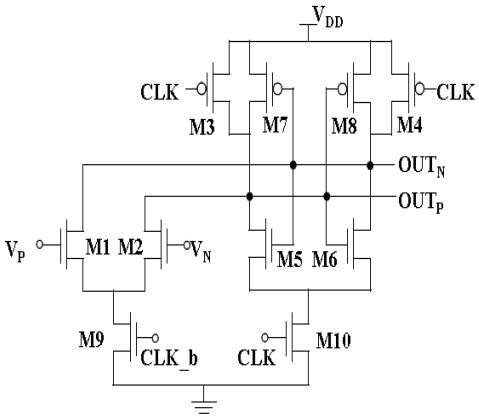

Figure 3. Proposed comparator design.

$$t_0 = \frac{C_L V_{Charge}}{I_{Eq}} \quad (1)$$

where C_L is the load capacitance at an output node and I_{Eq} is the resultant current of M3 minus the current of M10 and V_{Charge} is equal to V_{thn} in this case.

$$t_{latch} = \frac{C_L}{gm_{eff}} \ln\left(2\frac{\Delta V_{OUT}}{V_O}\right) \quad (2)$$

where ΔV_{OUT} and V_O are as indicated in Fig. 2.

In general V_O can be written as $V_O = G\Delta Vin$ where G is the gain of the interface stage (M5-M11) between the inputs signals and inputs of the cross-coupled inverters and ΔV_{in} is the difference between the input signals (V_P, V_N).

The total delay can be expressed as:

$$t_{delay} = \frac{C_L V_{Charge}}{I_{Eq}} + \frac{C_L}{gm_{eff}} \ln\left(2\frac{\Delta V_{OUT}}{G\Delta Vin}\right) \quad (3)$$

III. The Proposed Comparator

Equation (3) indicates that the gain of the interface stage and V_{Charge} can be used as control parameters to shorten the delay of the comparator. For our main target application, which is on-chip sampling of high-frequency PRBS, the speed is the first concern. Both V_{Charge} and G are utilized to design a high speed comparator.

The proposed comparator is composed of two stages as shown in Fig. 3. The first stage is the amplification stage, which is consists of the transistors M1–M4 and M9. The second stage is the regenerative stage that is comprised of the transistors M5–M8 and M10. The circuit works in two phases, namely the amplification phase and the regenerative (evaluation) phase. As shown with red color in Fig. 2, when the clock (CLK) is low (amplification phase), the tail transistor M9 is turned on and the transistors M1-M4 work together as a difference amplifier with resistive load utilizing the on resistance of M3 and M4. During this phase the difference between V_P and V_N is amplified and the differential outputs are applied to the inputs of the regenerative stage. At the same time, the second tail transistor M10 is off, which prohibits the operation of the regenerative stage.

When the clock turns to its high state, M9 turns off disabling the operation of the amplification stage. On the other hand M10 is turned on enabling the operation of the regenerative stage. The regenerative stage starts its operation with its inputs being fed by an amplified version of the differential inputs V_N and V_P. In addition, the amplification stage is designed to produce its output close to V_{DD}-$|V_{thp}|$ which can effectively reduce the charging time t_0 given by Equation (1).

Furthermore, since that the gain of the gain stage is larger than one, this tends to reduce t_{latch}. Fig. 2(b) and 2(a) show the timing diagram of the proposed circuit and the reference comparator of [5] respectively. This figure clearly indicates the reduction of the delay time in the proposed circuit over the Ref comparator. Since that the proposed circuit uses an amplification stage, it consumes static power during the amplification period and hence the energy consumption in the proposed circuit becomes higher than the reference comparator design. However, since the proposed circuit is to work at high frequency, the energy consumption of the proposed circuit becomes comparable to the reference comparator, as will be shown in the subsequent sections.

IV. Simulation Results and Comparison

Since the comparator offset can be reduced by using known techniques [5], the main focus of this paper is the comparator speed. Simulation comparing the delay versus the difference input voltage of the comparator in [5] with the one in [12] at 65nm technology and 1.2V supply has been done. The results have shown that the comparator in [5] outperforms the one in [12]. Hence the comparator in [5] and the proposed one will be compared. These two designs were implemented in 65nm technology. The circuit netlists are extracted from the layout and simulated with a HSPICE simulator. Fig. 4 shows simulation results of the delay versus input voltages difference (ΔV_{in}) at two different bias voltages for the proposed and reference designs. The results show that the proposed circuit has ~35% less delay time than the reference design. On the other hand, it shows ~10% delay dependence on the common mode level within the range of interest. The simulation results are consistent with the

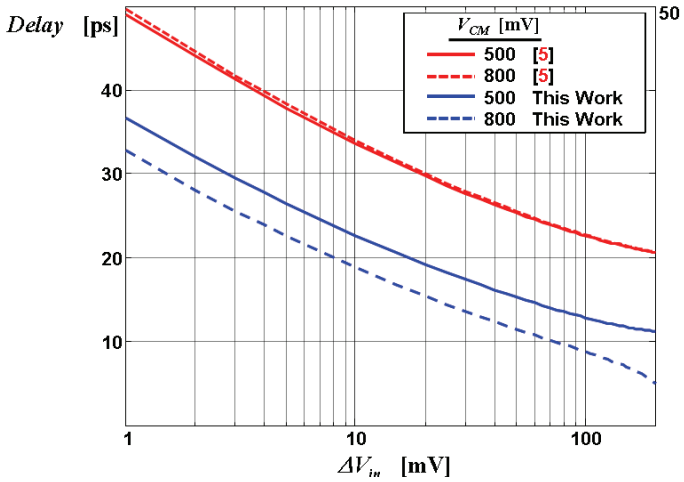

Figure 4. Simulated comparator delays versus input voltages difference. Red curves show the delay of the reference circuit [5]. Blue curves show the delay of the proposed circuit.

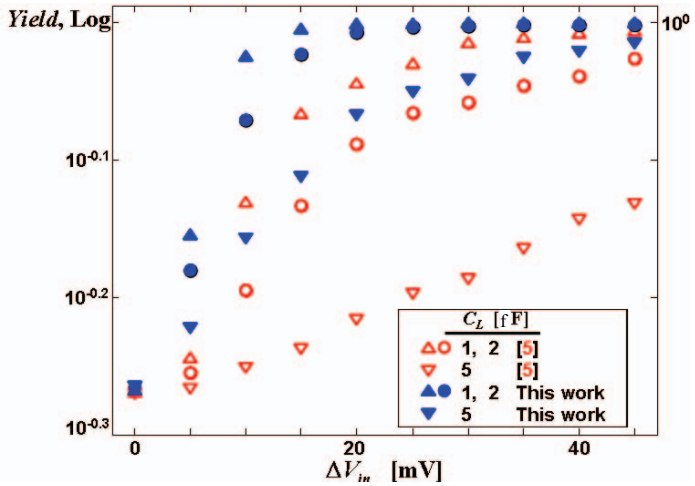

Figure5. Simulated comparator yield versus input voltages difference. Red symbols show the yields of the reference circuit [5]. Blue symbols show the yields of the proposed circuit.

theoretical explanation given in Section II. Note that performance of the proposed circuit is limited by the delay time in the evaluation phase.

While the PV variation can be translated into a referred input offset, the supply transitions contribute the input referred noise. Regarding these issues, a Monte Carlo simulation for 1000 samples of each circuit is done at different load capacitors. The threshold voltage variations given by the technology were assumed. The yield is calculated versus ΔV_{in} as shown in Fig. 5, where the yield represents the number of correct decisions per 1000 devices at each ΔV_{in}. Fig. 5 reveals the robustness of the proposed structure over the reference design.

In the proposed circuit design, the power consumption is dominated by the power consumed in the amplification phase. This makes the proposed circuit less attractive for the low power applications at low frequencies. At the highest possible frequencies that can be practically applied on the two circuits, the power consumption is estimated from simulations. The proposed circuit consumes 461µW at 7.2GHz, while the reference circuit consumes 310µW at 5.5GHz, which reveals that the power consumptions of the two circuits are comparable.

V. Test Chip and Measurement Results

One conventional method for characterizing a clocked comparator applies a step function, which has a height ΔV_{in} with respect to the common voltage V_{CM}. The step response is captured by shifting the strobe position *t*, which is applied into the CLK input of the comparator [11]. The analog step response corresponds to the decision error probability. Thus, a digital failure counter or BER analysis can be performed on the output from the comparator. Since conventional methods require both a step function and sampling strobe of very fine time resolution (= edge placement accuracy), it is difficult to apply this method to characterization of an on-chip clocked comparator integrated on a CMOS chip. Instead, we propose a different method, which uses a constant ΔV_{in} and a free-running oscillation as a CLK. By increasing the frequency of the clock, the decision error probability can be directly estimated from its output. Furthermore, a CLK can be easily provided by on-chip ring oscillators.

In order to identify the erroneous behavior of the comparator, an M-divided comparator output and the M-divided CLK were off-chip monitored as shown in Fig. 6.

The characterizing procedure of a comparator is as follows:

1- Select a constant ΔV_{in} by adjusting V_P and V_N.
2- Select a frequency of CLK by using the coarse and fine control knobs (CC and FC in Fig. 6).
3- Monitor the M-divided comparator output to detect erroneous response of the comparator.
4- Repeat the steps from 1 to 3 for different ΔV_{in}.

Note that for step 3, the comparator is considered to work correctly as long as its output frequency is identical to the ring oscillator frequency. If the comparator' output starts to fluctuate, the comparator is considered as being failed. Measuring the BER of the comparator output is an alternative way for this purpose.

The two circuits have been implemented using a 65-nm CMOS process with 1.2-V supply. Fig. 7 illustrates the die photo. The layouts are partially superimposed on the die photo to indicate the locations of the circuits inside the chip. Since the layout of the circuits was done using lower-level metal layers, higher-level dummy metal layers hide the circuits underneath. Consequently, the fabricated circuits do not appear in the die photo. The active areas of both circuits are measured form the layout. The active area of the proposed circuit is ~17% less than its counterpart of the reference circuit.

An M of 256 was adopted to divide the comparator and CLK outputs. Fig. 8(a) and Fig. 8(b) show the M-divided comparator outputs from our proposed circuit and the 65-nm version of the reference [5], respectively. Note that one CLK generator is activated at a time to get rid of potential noise coupling between the two circuit blocks. Fig. 8(c) and Fig. 8(d) show the spectrum of the M-divided comparator outputs from our circuit and the reference circuit at ΔV_{in} = 200 mV, respectively.

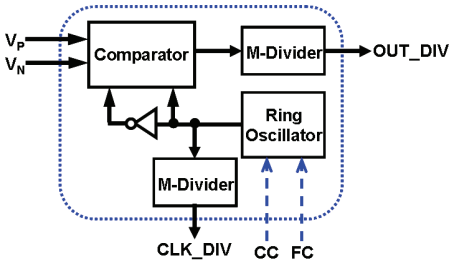

Figure 6. On-chip setup for validating the comparator design: M = 256.

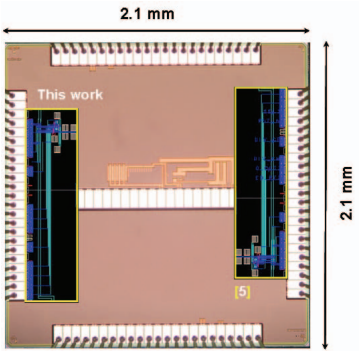

Figure 7. Two circuit layouts on the 65 nm CMOS die photo. The proposed circuit was implemented on the left. The reference circuit [5] was implemented on the right.

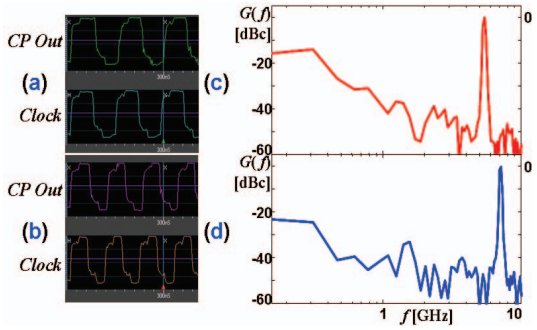

Figure 8. Measured waveforms using a SoC Tester (Advantest T2000). Applied clock and comparator outputs from the reference circuit [5] (a), and from the proposed circuit (b). Peak spectrum is observed at 5.5 GHz for the reference circuit [5] (c), and at 7.2 GHz for the proposed circuit (d).

The maximum operating frequency of our circuit was 7.2 GHz, while the reference circuit was able to operate at approximately 5.5 GHz. The measurement results at the maximum operating frequency of the four chips of the proposed and the reference circuits are shown in Fig. 9. The results clearly show that the proposed circuit can effectively operates at a higher clock frequency than the reference circuit at the same input difference ΔV_{in}. Interestingly, the ratio of the measured maximum operating frequency of the proposed circuit to that of the reference circuit is very close to the ratio of the simulated delay at the corresponding ΔV_{in}.

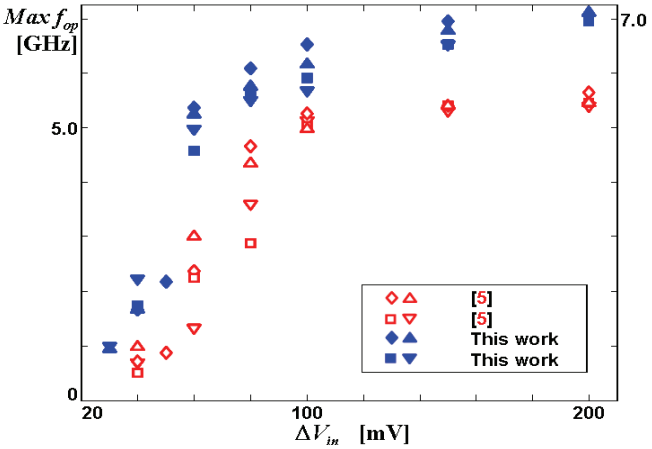

Figure 9. Measured maximum operating frequencies (f_{op}) versus input voltage differences: 4 chips.
Red symbols show the max f_{op} of the reference circuit [5].
Blue symbols show the max f_{op} of the proposed circuit.

VI. Conclusion

This paper offers two contributions. First, a design for an on-chip high-speed clocked-comparator for digitizing high-frequency low-swing signals was presented. The proposed circuit and a conventional reference comparator as presented in [5] were implemented in 65nm technology on the same chip. The measurement results show that the proposed circuit can operate at an average of 31% higher speed than the reference circuit with comparable power consumption at high frequencies. Secondly, a new cost-effective technique was introduced for measuring the highest clock frequency that can be applied to on-chip clocked-comparators. This technique relaxes the need for highly sophisticated test equipments that is usually needed for high frequency signal measurements.

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