

Reconfigurable 60-GHz Radar Transmitter SoC with Broadband Frequency Tripler in 45nm SOI CMOS

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Abstract— A reconfigurable 60-GHz radar transmitter with a broadband frequency tripler is proposed to support CW/FMCW, pulse, and PMCW radar waveforms from a single front-end. The proposed IC consists of a wide-band frequency tripler, a two-stage driver, two power mixers with baseband circuitry and serial I/O circuitry. The IC measurements in CW mode operation show an output power of 12.8 dBm (average) and 14.7 dBm (peak) from 54 GHz to 67 GHz with harmonic suppression greater than 27 dB. Pulse and PMCW mode operations are also demonstrated to generate short pulses with the minimum pulse width of 25 ps corresponding to 40 GHz signal bandwidth and 10-Gb/s PRBS modulated signals, respectively. Fabricated in a 45-nm CMOS SOI process, the IC consumes 0.51 W and occupies an active area of 1.95 mm² excluding pads.

Keywords— CMOS, multi-modal radar, FMCW radar, 60 GHz, pulse radar, PMCW radar, wideband frequency tripler.

I. INTRODUCTION

Millimeter wave (mmWave) radars realized using Si-based ICs have enabled the exploration of an increasing number of applications, such as automotive, drone navigation, gesture recognition, and remote biometrics monitoring. Different usage scenarios require different waveforms and varying performance trade-offs between detection range (available SNR) and resolution (signal bandwidth). For instance, short-pulse radar is suitable for medical applications requiring high spatial resolution within a short range[1]. By contrast, phase-modulated continuous-wave (PMCW)[2] or frequency-modulated continuous-wave (FMCW) radar[3], [4] is optimal for automotive applications requiring a long detection range and moderate resolution. Low cost and reduced form factor are key enablers for the mass adoption of mmWave sensors, so a single-chip multi-mode radar solution is desirable[5]. In this paper, we propose a reconfigurable broadband V-band radar transmitter (TX) capable of generating (1) continuous wave (CW/FMCW), (2) pulse, and (3) PMCW radar waveforms from a single CMOS front end, providing adaptability for different applications and support for a multimodal radar system.

II. RECONFIGURABLE TRANSMITTER ARCHITECTURE

Fig. 1 shows the proposed reconfigurable transmitter architecture. A broadband frequency tripler up-converts an LO input in the range of 17–22 GHz to 51 GHz–66 GHz. The tripler is followed by a two-stage amplifier and a pair of power mixers. The power mixers are configured/driven by baseband (BB) signals generated from a waveform generator and their

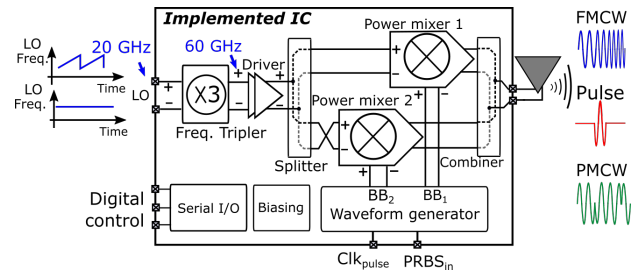


Fig. 1. Proposed reconfigurable radar transmitter architecture.

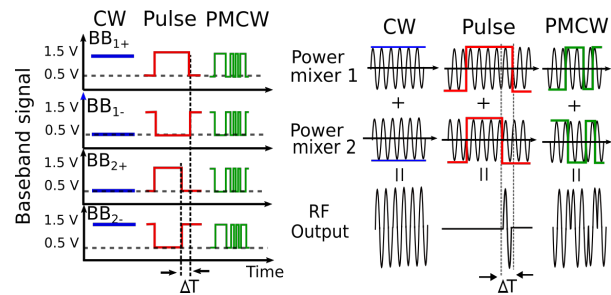


Fig. 2. Baseband signals to modulate the two power mixers for generating different radar waveforms.

combined outputs form the final output of the radar TX. The waveform generator is key to the configurability of the TX. Fig. 2 shows the BB signals and the waveform generation principle corresponding to each output radar waveform type. In CW mode, the power mixers operate as power amplifiers with DC BB signals. The BB signal polarities between the two power mixers are opposite for constructive combining as the LO input polarity is swapped for the 2nd power mixer. When coupled to a wideband PLL which generates an output frequency of 17–22 GHz with frequency chirp generation capability, e.g. [6], this mode enables the creation of FMCW radar signals from 51 GHz to 66 GHz. For pulse mode operation, two clock signals with aligned rising edges but different falling edges by ΔT are applied to the power mixers. The mixer's outputs are added constructively only when the two BB signals are not overlapped (added destructively otherwise), thus generating a sharp pulse with the programmable pulse width down to 25 ps at the output. A key advantage of this approach is that pulse generation occurs at the combiner, therefore the bandwidth of the front-end circuitry does not directly limit the minimum pulse width, enabling the maximum pulse signal bandwidth of 40 GHz. In PMCW mode, the two power mixers are fed with complementary code waveforms to support binary phase

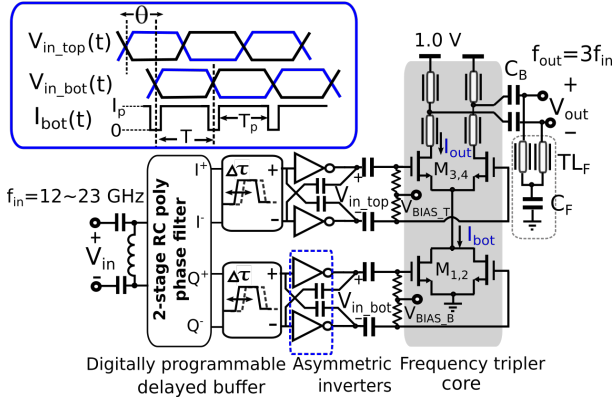


Fig. 3. Schematic of frequency tripler with >30-GHz output frequency range.

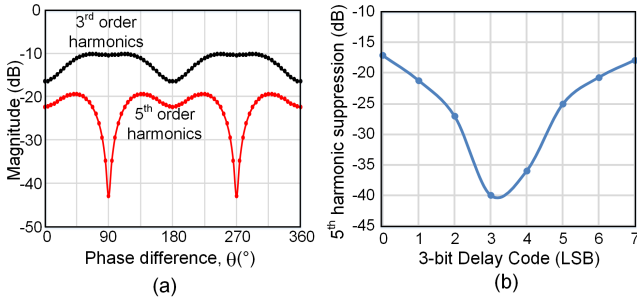


Fig. 4. (a) Calculated output current magnitude at $3\omega_{in}$ and $5\omega_{in}$ with respect to phase difference (b) measured $5\omega_{in}$ suppression across 3-bit fine delay tuning code for an input frequency of 13 GHz.

modulation. Since only the last stage of the transmitter is directly modulated with the baseband signal, the front end can support code data rates exceeding 10 Gb/s.

III. CIRCUIT-LEVEL IMPLEMENTATION IN 45-NM SOI

A. Wide-band Frequency Tripler Design

Fig. 3 shows the proposed frequency tripler with input I/Q generation and programmable delay preamplifiers. The frequency tripler core consists of a push-push frequency doubling differential pair $M_{1,2}$ and an up-conversion differential pair $M_{3,4}$ in a current-reuse topology. Assuming (1) an ideal square-wave switching of $M_{3,4}$ and (2) a rectangular waveform of the combined drain current of $M_{1,2}$, $I_{bot}(t)$, with a duty ratio of $\alpha = T_p/T$, the output current $I_{out}(t)$ for an input frequency of ω_{in} is written as

$$I_{out}(t) = \frac{4}{\pi} I_{bot}(t) \sum_{m=1} \frac{\sin((2m-1)\omega_{in}t)}{2m-1} \quad (1a)$$

$$I_{bot}(t) = \sum_{n=0} I_n \cos(2n(\omega_{in}t + \theta)), \quad (1b)$$

where $I_0 = \alpha I_p$, $I_n = I_p/(\pi n) \sin(2n\pi\alpha)$ for $n > 1$, and θ is the phase difference between driving voltages of $M_{1,2}$ and $M_{3,4}$ as shown in the inset of Fig. 3. Eq. (1) indicates that the k^{th} harmonic frequency component of the output current results from the combination of different mixing processes which meets $k = |2m \pm 2n - 1|$ as a function of θ . To find out the optimum θ for the maximum

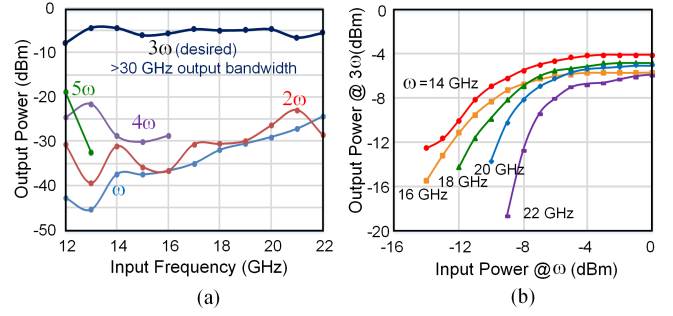


Fig. 5. Measured frequency tripler output using a separate breakout circuitry

conversion gain, Fig. 4(a) shows the calculated 3^{rd} and 5^{th} harmonic frequency components of the output current across θ for $m, n \leq 3$. $\theta = 90^\circ$ provides the maximum conversion gain at $3\omega_{in}$ and the minimum conversion gain at $5\omega_{in}$ which is the dominant unwanted harmonic for low input frequencies. To drive $M_{1,2}$ and $M_{3,4}$ with an accurate 90° difference, a two-stage RC poly phase filter generates broadband quadrature signals using staggered tuning over a bandwidth >10 GHz, and the programmable delay buffers, based on current-starved inverters, provide fine phase control of ~ 0.3 ps resolution over ~ 2 ps tuning range with 3-bit digital control. Fig. 4(b) shows the measured 5ω harmonic suppression over 3-bit delay code of the input buffer (realized in a separate breakout), demonstrating the effect of fine I/Q timing control. Asymmetric inverters following the I/Q timing circuitry drive $M_{1,2}$ with the optimum bias voltage and duty ratio α for maximum $2\omega_{in}$ generation in I_{bot} . An output filtering network consisting of C_B , TL_F , and C_F is designed to suppress ω_{in} and $4\omega_{in}$ in which C_B and TL_F form a high pass filter to suppress ω_{in} , and TL_F and C_F form a notch filter using a series resonance to suppress $4\omega_{in}$. Fig. 5 shows the measurement of the frequency tripler in a separate breakout. Output bandwidth is greater than 30 GHz with a peak output power of -4.4 dBm; harmonic rejection up to $4\omega_{in}$ is better than -20 dB over an input frequency range of 14 GHz to 20 GHz. The harmonic suppression is further improved through the front-end circuitry that follows the frequency tripler. Fig. 5(b) shows the measured output power at $3\omega_{in}$ with respect to input power for different frequencies. The maximum conversion gain is higher than 0 dB for input frequencies up to 20 GHz, and the saturation output power is around -5 ± 0.9 dBm. The measured power consumption of the frequency tripler ranges from 33 mW to 39 mW from 1 V power supply for input frequencies from 12 GHz to 22 GHz. The proposed frequency tripler presents a wider output bandwidth and higher conversion gain with a comparable power dissipation compared to a prior wide-band V-band frequency tripler with 18-GHz bandwidth and -5.2-dB conversion gain[7].

B. TX Front-end and Waveform Generator Design

Fig. 6 shows the front-end and waveform generator schematic. The two power mixers are driven by two-stage

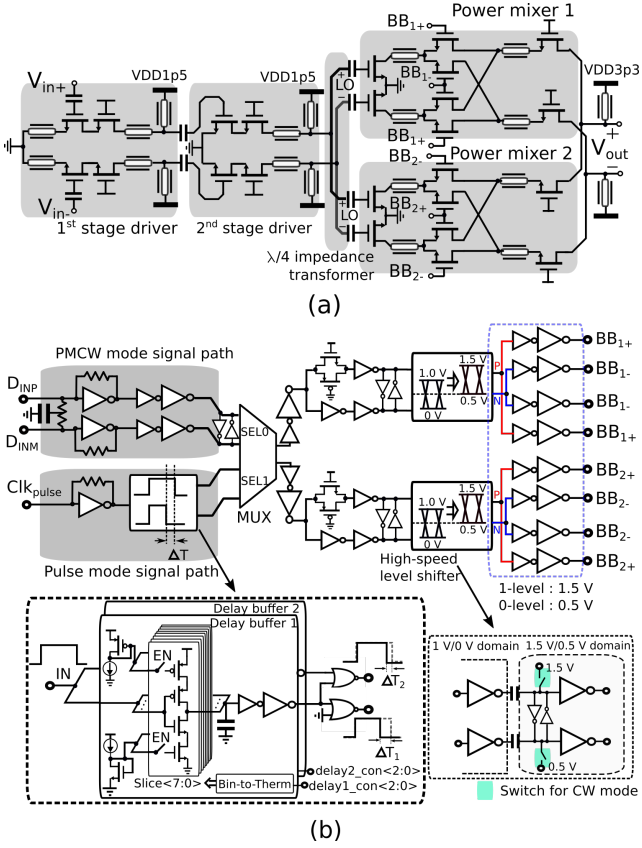


Fig. 6. Schematic of (a) front-end and (b) waveform generator.

different differential cascode amplifiers through $\lambda/4$ impedance transformers. The 1st stage driver has a degeneration inductor for a broadband input matching to provide a consistent load impedance to the frequency tripler over a wide frequency range. The power mixer is similar to a differential Gilbert mixer with cascode transistors on the top. The quad-switching devices are modulated with BB signals from the waveform generator as shown in Fig. 2. The simulated front-end gain in CW mode is 27.7 dB at 60 GHz with 3-dB bandwidth of 17 GHz. The waveform generator has separate signal paths for pulse and PMCW modes, selected by a MUX. The pulse mode input receives a clock signal CLK_{pulse} which determines the pulse repetition frequency. The clock signal is applied to a programmable pulse generation block after resistor-feedback inverters. The pulse generation circuitry consists of two programmable delay blocks followed by NOR gates to generate two outputs with aligned rising edge but time-shifted falling edges. The falling edge difference $\Delta T = \Delta T_1 - \Delta T_2$ determines the pulse width at the RF output. Each delay block is independently controlled with 3-bit slices, covering a 140-ps range with ~ 23 -ps resolution. After the MUX selects one of the two input paths, the signal is converted into a differential signal and level-shifted from the 0/1.0V to the 0.5/1.5V domain to properly drive the power mixer's quad-switching devices. For CW mode, the switches inside the level shifters are turned on to provide the proper DC level to the BB output.

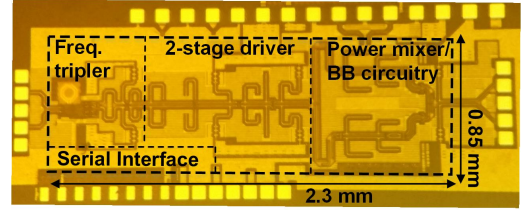


Fig. 7. Chip photograph.

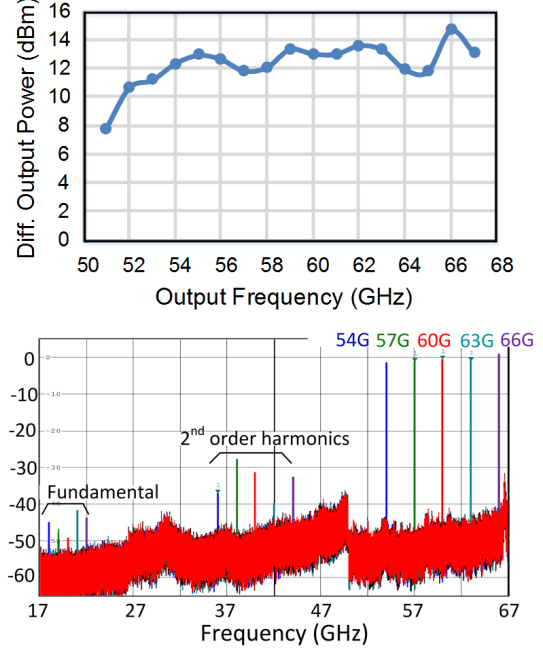


Fig. 8. Measured differential output power across frequency and frequency spectrum at the single-ended output.

IV. MEASUREMENT RESULT

The IC was fabricated in 45-nm SOI CMOS process with an active chip area of 2.3 mm \times 0.85 mm excluding pads; a die photo is shown in Fig. 7. All measurements have been performed on-wafer at 25 $^{\circ}$ C. Fig. 8 shows the CW mode operation. The measured average output power (measured using a U8488A power sensor with 0 dBm tripler input power) from 54 GHz to 67 GHz was 12.8 dBm, with peak power of 14.7 dBm at 66 GHz. The power variation from 59 GHz to 63 GHz is less than ~ 0.3 dB, which can support 4-GHz FMCW radar generation. The frequency spectrum (measured using a single-ended output) also demonstrates harmonic rejection greater than 27 dB over a wide bandwidth; this result could be further improved if measured differentially, considering that dominant harmonic component at the single-ended output is the second order harmonic frequency. The pulse and PMCW mode operations were measured at a single-ended output in the time and frequency domains using a 70-GHz BW DSA8300 Digital Serial Analyzer and FSU67 spectrum analyzer. Fig. 9 shows results from pulse mode operation with CLK_{pulse} of 400 MHz and output carrier frequency of 66 GHz for different ΔT settings of the delay blocks in the waveform generator. The measured pulse width at half maximum ranges from 25

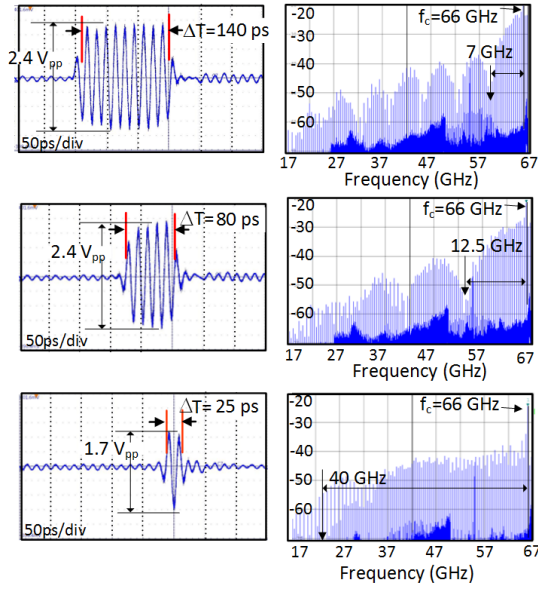


Fig. 9. Measured pulse mode output for different pulse width settings in time and frequency domains.

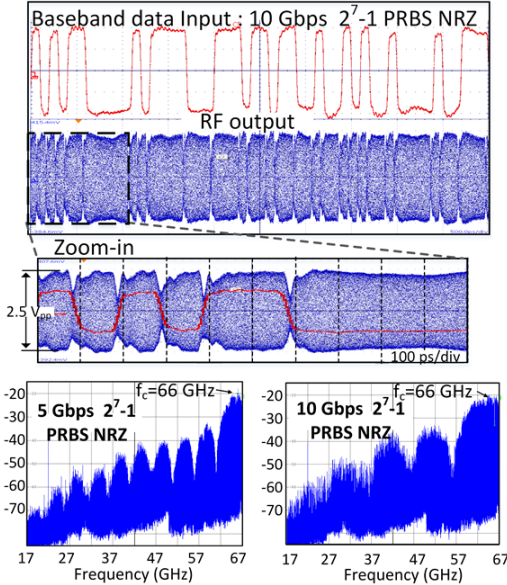


Fig. 10. Measured PMCW mode output in time and frequency domains.

ps to 140 ps, which corresponds to signal bandwidth from 7 GHz to 40 GHz. Note that 40-GHz BW can be translated into a 3.75 mm spatial resolution. The peak output power differed by less than 1 dB compared to the CW mode until the pulse width is reduced to <45 ps. The PMCW mode of operation was also measured with a 10-Gbps $2^7 - 1$ PRBS baseband signal in the time and frequency domains, demonstrating a wide signal bandwidth as shown in Fig. 10. The average power consumption of the IC is 0.51 W (0.36 W for power mixers, 0.1 W for pre-drivers, and 0.05 W for frequency tripler and BB/digital circuitry). Table 1 summarizes the performance of the proposed design compared to prior single-mode and multi-modal radar transmitter ICs.

Table 1. Performance summary and comparison

	This Work	[5]	[1]	[4]	[2]
Supported Waveforms	Pulse, FMCW/CW, Code (PMCW)	Pulse, FMCW/CW	Pulse	FMCW	Code (PMCW)
Frequency	60GHz	24/26GHz	90GHz	77GHz	79GHz
Pulse Width	25ps-140ps	500ps-1ns	25ps-220ps	N/A	N/A
FMCW BW	4GHz ^a	0.32GHz	N/A	4GHz	N/A
CW Output Power	12.8dBm(ave.) 14.7dBm(peak)	-0.56dBm	17.2dBm (PA Psat)	10.8dBm ^b	8.5dBm ^c
Code Rate	10Gb/s	N/A	N/A	N/A	2Gb/s
Integration level	Freq. tripler, waveform gen., TX front-end	VCO, freq divider, waveform gen., driver	VCO, PA, antenna, waveform gen.	PLL, 3TX, 4RX, Baseband, A2D, MCU	PLL, 2TX, 2RX, A2D, digital core
Chip Area	1.95mm ²	3.64mm ²	1.2mm ²	22mm ²	7.9mm ²
Technology	45nm SOI CMOS	130nm CMOS	130nm SiGe	45nm CMOS	28nm CMOS
Power Cons.	0.51W	0.14W	0.74W	3.5W	1W

^a A chirp bandwidth of 4 GHz for FMCW radar is supported with <0.3-dB output power variation, but an external PLL with chirp generation capability is required.

^b Across -40°C to 125°C

^c Including flip-chip assembly and module loss

V. CONCLUSION

This work has presented a wide-bandwidth reconfigurable mm-Wave radar transmitter integrated with a frequency tripler in CMOS. The proposed transmitter architecture enables a single front-end to generate FMCW/CW, pulse, and PMCW radar signals, thereby covering a wide variety of applications. The novel frequency tripler design technique has been integrated for a wide-bandwidth LO generation with high harmonic suppression.

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