5.5 A Low-Power Dual-Band Triple-Mode WLAN CMOS Transceiver

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Although dual-band CMOS transceivers used in IEEE 802.11a/b/g WLAN systems have been extensively developed [1 - 4], there is an increasing demand for lower power, multi-standard transceivers for portable applications. An example of such applications is future multi-functional cellular phones that require a long battery life. Moreover, to achieve a higher data rate by means of higher-order modulation (OFDM/256QAM, etc.), wider bandwidth technology (UWB etc.), space-time diversity (MIMO etc.) and so on, transceiver architectures with a lower noise and/or a higher signal-to-noise ratio are becoming more attractive.

In this paper, a direct-conversion dual-band triple-mode low-power CMOS transceiver with low noise figure is presented.

The highlights of the proposed transceiver (shown in Fig. 5.5.1) are: (1) a ΔΣ–based low-phase-noise fractional-N frequency synthesizer with a switched resonator VCO to cover the entire range for WLAN standards, (2) a concurrent-conjugate-matching dual-band LNA for low power consumption with low noise figure, (3) a single widely-tunable LPF based on an adaptive DC-current-control circuit, triode-biased MOSFET (ADTM) transconductor for multi-mode operation with low power consumption, and (4) a DC-offset compensation circuit using an adaptive activating feedback loop (AAFL) to achieve a fast response time with low power consumption.

One of the most crucial subsystems in a multi-standard transceiver is the frequency synthesizer. In general, a conventional multi-band synthesizer includes a number of dividers and/or mixers, resulting in high power consumption. To achieve low power consumption as well as a multi-band yet compact synthesizer, a switched resonator dual-band VCO configuration with a back-gate impedance-controlled MOS switch is introduced (Fig. 5.5.2). The resonator in this configuration consists of the tapped inductors and an MIM capacitor bank. The MOS switch operates so that the back-gate impedance is set high in the off-state and low in the on-state. Thus, this VCO configuration enables high frequency oscillation with low phase noise. Moreover, to achieve lower phase noise characteristics, a ΔΣ-based fractional-N frequency synthesizer configuration is employed. The circuit consists of a pulse-swallowed dual-modulus divider, a 3rd-order ΔΣ-modulator, a 2nd-order off-chip loop filter with a digital controller for the MIM capacitor bank, and a divide-by-two divider generating quadrature LO signals.

The measured in-band and out-of-band phase noise are as low as –95dBc/ and -110dBc/Hz, respectively, within a wide tuning range of 2.4 to 2.5GHz, and 4.9 to 5.95GHz.

In the receive path, a concurrent-conjugate-matching dual-band LNA is introduced followed by a direct-down-conversion mixer, two programmable gain amplifiers with fast DC-offset compensation circuits, LPFs based on an ADTM-transconductor. To suppress common-mode noise, all circuits use a differential architecture.

The dual-band LNA consists of a fully balanced, two-stage cascaded amplifier (LNA1, LNA2) with a concurrent-conjugate-matching circuit, a dual-band LC resonator switch, and an attenuator. In the first stage LNA (LNA1), wide-frequency band characteristics is achieved by using a low-pass type input-matching circuit, and high linearity with high common-mode noise immunity is achieved by a tail resonator. To provide high gain in dual frequency bands of interest, the concurrent-conjugate-matching circuit is employed between LNA1 and LNA2. The conjugate-matching is realized in both frequency ranges by setting the resonant frequency of LNA1 output matching circuit and LNA2 input matching circuit at the geometrical mean of 2.4GHz and 5.2GHz. To reduce the LNA power consumption without sacrificing noise figure, an RF-power bypassing scheme is employed by dual-band LC resonator passive switch, where LNA2 turns off and the signal bypasses through the attenuator at high input power level.

The schematic diagram of a widely tunable 4th-order Butterworth g_m-C LPF using an ADTM-transconductor is shown in Fig. 5.5.3. The ADTM transconductor consists of a cascode amplifier with a triode-biased input FET (Q1), a current-mirror circuit (Q3, Q4), and an adaptive DC-current-control circuit with a replica of the transconductor core and an operational amplifier. High linearity can be provided by the triode-biased configuration, since the output signal of the cascade amplifier is fed back to the Q1 drain through Q3, so that Q1 operates under constant drain-to-source bias conditions in the triode region. The low power consumption can be achieved by adaptive DC-current-control circuit scheme, where DC bias current of Q3 and Q4 can be minimized even in a high-g_m condition.

A DC-offset compensation circuit using an AAFL consists of a high-pass filter, a DC-offset voltage-detecting circuit, and a tri-state buffer. Fast responses with negligibly low power consumption can be achieved, since the feedback loop is activated only when the PGA output signal exceeds the input-referred P_{1dB} for the following circuit. The response time measured for this circuit is 0.15μs.

The total current draw of the receive path is 78mA, both for 2.4/5.2GHz from a 1.8V supply while the overall NF is 3.5/4.2dB at 2.4/5.2GHz. As shown in Fig. 5.5.4, the NF deviation is within ±0.1dB in 2.4 to 2.5GHz, and ±0.65dB in 4.9 to 5.95GHz. The sensitivity is low, –93/–94dBm for a 6Mb/s at 2.4/5GHz. The tuning range of base-band cutoff frequency is 0.5 to 12MHz.

The transmit path consists of I/Q low-pass filters, doubled balanced modulators for each band, and driver amplifiers. The filters are identical to the ones used in the receiver.

The measured constellation diagrams for transmitted 64QAM OFDM signals for both bands are shown in Fig. 5.5.5. The measured EVM is 3.2/3.4% for 2.4/5.2GHz. The current draw is 76mA for both bands from a 1.8V supply.

Overall performance is summarized in Fig. 5.5.6 and the chip micrograph is shown in Fig. 5.5.7.

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References:
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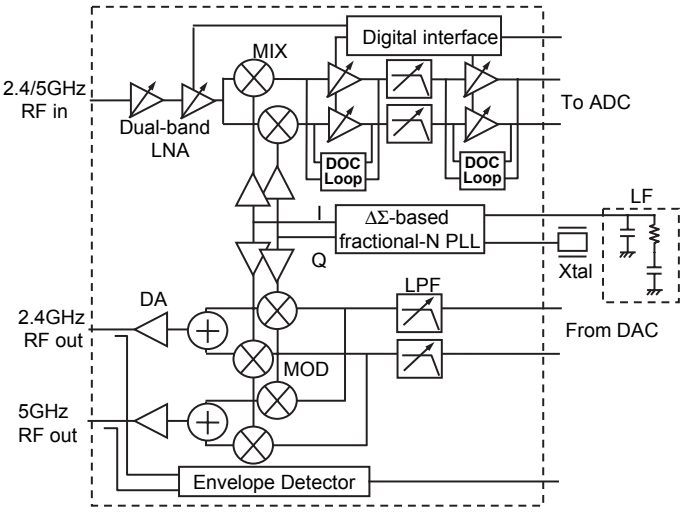

Figure 5.5.1: Block diagram of dual-band direct-conversion transceiver.

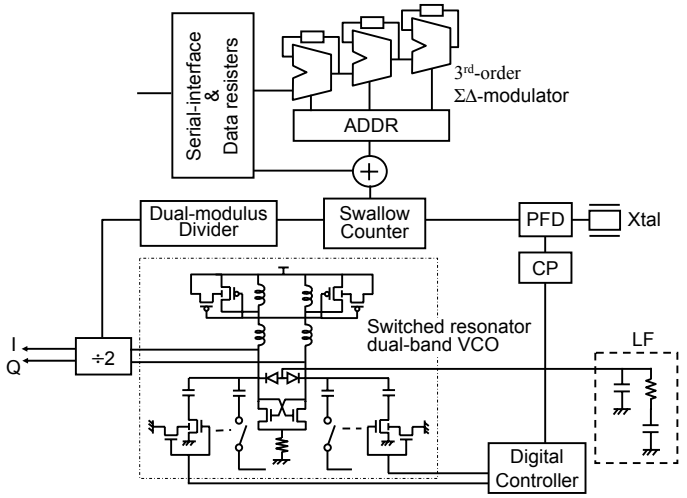

Figure 5.5.2: Circuit diagram of a dual-band low-noise synthesizer.

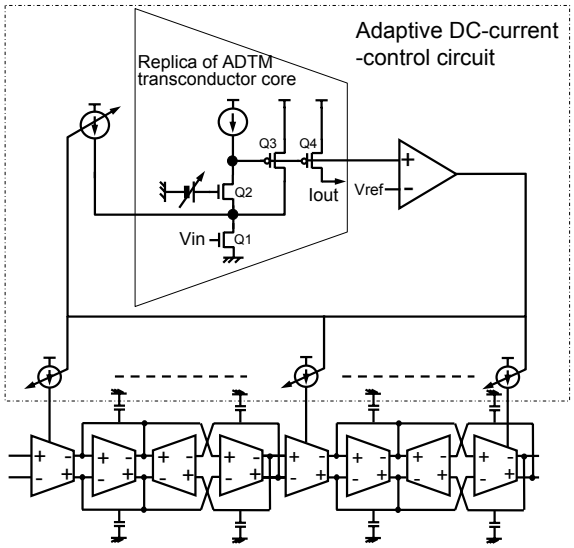

Figure 5.5.3: Circuit diagram of widely tunable ADTM transconductor LPF.

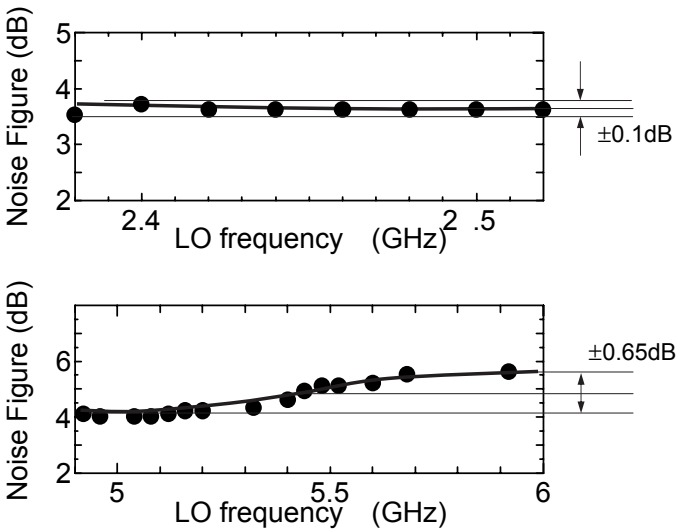

Figure 5.5.4: LO dependence of NF.

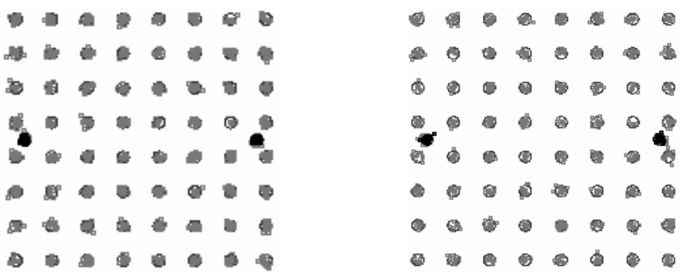

Figure 5.5.5: Measured constellation diagrams for transmitted 64-QAM OFDM signals on 2.4/5GHz bands.

		2.4GHz	5.2GHz
Supported bands (GHz)		2.4 - 2.5 / 4.9 - 5.95	
Supported channel bandwidth (MHz)		5 - 24	
Rx NF (dB)	max gain, 20MHz mode	3.5	4.2
Rx IIP3 (dBm)	min gain, 20MHz mode	+7	+5
	max gain, 20MHz mode	-5	-21
Rx max gain (dB)		75	
Rx sensitivity (dBm@6Mb/s OFDM)		-93	-94
Phase noise (dBc/Hz)	in-band	-95	-95
	out-band@1MHz offset	-110	-110
Tx P-1dB (dBm)		3	0
Tx EVM (%@Pout= -10dBm)		3.2	3.4
VDD (V)		1.8	
Rx current consumption (mA)		78	78
Tx current comsumption (mA)		76	76
Technology		0.18μm 1P6M CMOS	
Die size (Core Area) (mm2)		17.2 (11.4)	

Figure 5.5.6: Summary of transceiver performance.

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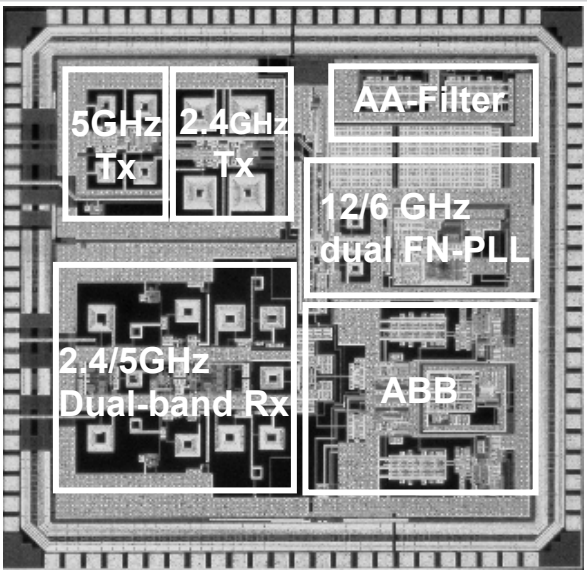

Figure 5.5.7: Micrograph of the transceiver die.

