A 600-GHz CMOS Focal-Plane Array for Terahertz Imaging Applications

Ullrich R. Pfeiffer and Erik Öjefors
High-Frequency and Communication Technology
University of Wuppertal, Rainer-Gruenter-Str. 21, D-42119 Wuppertal, Germany
Email: ullrich@ieee.org and erik.ojefors@ieee.org

***Abstract*— A 600-GHz single-chip focal-plane array (FPA) has been fully integrated in a 0.25-μm CMOS process technology. The 3×5 array achieves a room temperature responsivity of 50 kV/W and a noise equivalent power (NEP) of 400 pW/$\sqrt{\text{Hz}}$. Each pixel comprises of an on-chip antenna, an NMOS incoherent power detection circuit based on resistive self-mixing, and a 43-dB amplifier with a 1.6-MHz bandwidth. The pixel size is 150×150 μm^2 and the overall array size is 680×980 μm^2 including bondpads. The circuit topology makes it possible to fully integrate terahertz focal-plane arrays for 600-GHz video-rate imaging applications in a low-cost CMOS process technologies for the first time.**

I. Introduction

There is a vast amount of interest in millimeter-wave (mmWave) and terahertz applications today. Potential applications span across various scientific disciplines [1] and include radio astronomy, atmospheric sensing, medical diagnostics, biological research [2], label-free analysis of DNA molecules, wireless communication, radar [3], security screening, chemical and explosive detection. However, sensors and detectors that operate in the sub-millimeter wave band (300 GHz to 3 THz) have been a limiting factor for many applications in the past. Although great achievements have been made in terahertz science and technologies, detectors are often comprised of discrete components which are bulky and exhibit a low level of integration at high cost. Most terahertz images today are build up one pixel at a time, through raster scanning with single-point detectors or phased arrays. Therefore, a fully integrated CMOS focal-plane array is one of the key building blocks that will enable low-cost video-rate terahertz cameras in the future. It presents a crucial step towards the commercialization of terahertz imaging technologies.

Detection methods in this frequency range are commonly divided into two main categories: coherent detection and incoherent (direct) detection methods. Direct detectors have been around for many years and are based on the physical principle of energy/power absorption (calorimeters/bolometers [4], [5]), pneumatic detectors (Golay cell [6]), and square-law detectors (Schottky Barrier Diodes (SBDs) or transistor npn/FET non-linearities). Most of them are, however, incompatible with conventional microelectronics and require additional processing steps to be incorporated into today's semiconductor process technologies. Emerging detection principles include semiconductor nano-devices such as quantum dot arrays and plasma wave detectors [7]. Coherent detectors consist of heterodyne receivers often made of monolithic microwave integrated circuits (MMICs) [8]. The high cost of MMICs, however, limit the pixel count in a heterodyne receiver and the use of LNAs is typically limited to below 200 GHz in practical applications [3].

It is expected that future low-cost portable terahertz cameras will require sophisticated signal processing capabilities, paired with low power consumption and high sensitivity at room temperature. This fuels the growing interest in silicon integrated terahertz detectors. Promising low-cost alternatives include all electronic approaches, such as silicon SBD circuits with cut-off frequencies beyond 1 THz [9], SiGe hetero-junction bipolar transistors (HBTs) with cut-off frequencies as high as $f_{max}/f_T = 350/300$ GHz [10], and CMOS circuits reported at frequencies higher than 400 GHz [11].

In this paper the self-mixing of resistive mixers is used for incoherent (direct) power detection at 600 GHz, which is well above the used CMOS technologies cut-off frequency of $f_T = 35$ GHz. The detection principle has first been published in 1987 in discreet 10-500 MHz power detectors based on JFETs [12], and has been used later, for 0.1-3 GHz GaAs MESFET detectors in [13]. It is applied here to 600-GHz silicon integrated focal-plane arrays for the first time. The circuit architecture and the detection principle are described in Sec. II. Measured and simulation results are presented in Sec. III followed by the conclusions in Sec. IV.

II. Circuit Architecture and Detection Principle

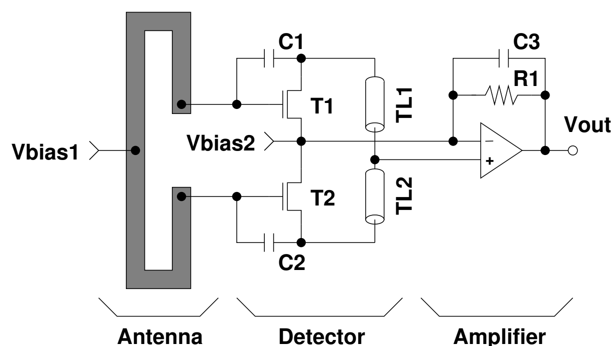

Fig. 1. Simplified single-pixel circuit schematic (R1=500 kΩ, C3=0.1 pF, C1 and C2=13 fF).

Self-mixing is usually unwanted and is caused by the parasitic FET gate-to-drain capacitance C_{gd}. It leads to dc-

offset problems in resistive mixers as described in [14]. A resistive mixer converts a radio frequency (RF) signal applied at the drain of a FET to a lower frequency IF signal that is extracted through a low-pass filter. This is done while the local oscillator (LO) signal is used to modulate the conductance of a FET channel at the gate.

Unlike this, an incoherent (direct) power detection method is used in this paper as shown in Fig. 1. The 600-GHz RF input signal is received by an on-chip folded dipole antenna. It is then coupled from the gate to the drain of a differential FET structure (T1 and T2) via coupling capacitors (C1 and C2). Shunt transmission lines (TL1 and TL2) are used to tune out the reactance at the drains for maximum voltage swing and maximum self-mixing response. The detector is followed by an on-chip 43-dB amplifier with 1.6-MHz bandwidth. The amplifier is biased at ac-grounds through the common source contact of T1 and T2 to omit additional quarter-wave RF bias chokes. Similarly, the gate bias is applied at ac-grounds of the dipole antenna. The pixel circit draws 1.1 mA from a 5-V supply.

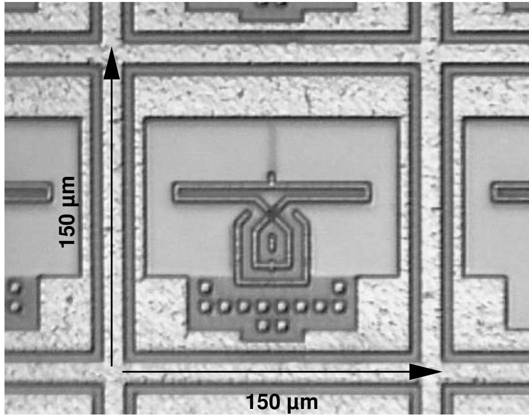

Fig. 2. Chip micrograph of one pixel showing the folded dipole antenna. The size of a pixel is 150×150 μm^2.

A chip micrograph of a single pixel including an on-chip dipole antenna is shown in Fig. 2. The chip was fabricated in IHP's 0.25-μm SG25 logic CMOS technology with an NMOS cut-off frequency of $f_T = 35$ GHz [15]. A five-layer aluminum back-end was used to implement antennas and low loss interconnects.

A. Expected Responsivity and Noise Considerations

The responsivity and NEP of a self-mixing FET detector can be analytically derived. For simplicity it is given here only for a single device in strong inversion ($V_{gs} > V_{th}$) and for a time-harmonic excitation. If an excitation voltage $v_{ds}(t)$ is applied over the drain source junction with zero V_{ds} bias (triode region), the drain current can be calculated as

$$i_{ds}(t) = v_{ds}(t)g_{ds}(t) = v_{ds}(t)\frac{W}{L}\mu Q_{ch}(t), \qquad (1)$$

where $Q_{ch}(t) = C_{ox}(v_{gs}(t) - V_{th})$ is the time varying channel charge density and where W, L, and μ have their usual meaning. Since the drain and the gate are connected through the capacitors, e.g. through C1 and C2, we obtain $v_{gs}(t) = V_g + v_{ds}(t)$ and for the drain current follows

$$i_{ds}(t) = \frac{W}{L}\mu C_{ox}(v_{ds}(t)^2 + v_{ds}(t)(V_g - V_{th})). \qquad (2)$$

The dc-component of the drain current can be calculated for a time harmonic excitation of the form $v_{ds}(t) = V_{RF}\sin(\omega t)$ as

$$I_{ds} = \frac{W}{L}\mu C_{ox}(V_{RF}^2/2)). \qquad (3)$$

This leads to the detected dc output voltage

$$V_{ds} = \frac{I_{ds}}{G_{ds}} = \frac{V_{RF}^2}{2(V_g - V_{th})} \qquad (4)$$

and the expected responsivity is

$$R_v = \frac{V_{ds}}{P_{in}} = \frac{\frac{V_{RF}^2}{2(V_g - V_{th})}}{V_{RF}^2/R_{in}} = \frac{R_{in}}{2(V_g - V_{th})}. \qquad (5)$$

For example, this yields a responsivity of 250 V/W with a detector input impedance of $R_{in} = 50\ \Omega$ and $V_g - V_{th} = 0.1$ V. With a 43-dB voltage gain the responsitivity increases to 35 kV/W. Note that the responsitivity is only limited by the modulation speed of the channel charge density, and hence, the detection principle works well in the terahertz frequency range even in 0.25-μm CMOS process technologies. To the first order, it is not transit-time limited and only limited by the FET parasitic RC time constant.

The noise equivalent power (NEP), which is defined as the minimum power for unity signal-to-noise-ratio with a detector time constant of 1 s, is only limited by the thermal noise of the channel conductance G_{ds}. Since the channel of the NMOS detector is not dc-current biased, the noise spectral power density at the drain output terminal is $N_0 = 4k_BT/G_{ds}$ and the NEP follows as

$$\text{NEP} = \frac{\sqrt{N_0}}{R_v} = \sqrt{\frac{16k_BT}{R_{in}^2\frac{W}{L}\mu C_{ox}}(V_g - V_{th})}. \qquad (6)$$

The self-mixing is predicted by the available BSIM device models and can be simulated from strong inversion to the sub-threshold region. See Sec. III for a model-to-hardware comparison.

B. On-chip Antenna Design

Previously published silicon-integrated terahertz dipoles have used high-resistivity substrates [16]. In this work, a 90-μm long dipole antenna was implemented directly in a standard low-resistivity (50-Ωcm) process technology and losses were minimized by placing the main radiator in the top-metal conductor of the back-end process. A folded dipole increases the antenna impedance at resonance by a factor of four [17] and provides a higher RF voltage for the FET power detector. It also provides a symmetry point (ac-ground) through which the FET gate bias can be applied. The antenna was designed and simulated using the 3D EM solver package HFSS, where a 200 μm thick 50-Ωcm conductor-backed silicon substrate was

assumed. At 606 GHz the impedance is $100 - j75\ \Omega$ with an approximate bandwidth of 50 GHz. The simulated directivity is 7 dBi yielding a 5-dBi gain including losses.

C. Focal-Plane Array Configuration

The pixels were arranged in a 3×5 array with 150×150 μm pitch (0.0225 mm^2 area per pixel). See Fig. 3 for a chip micrograph. With the resolution limit being $\lambda_0/2$, the aperture is oversampled unless a dielectric lens is used. The outputs of neighbour pixels can be combined by the readout electronics to improve the sensitivity if required.

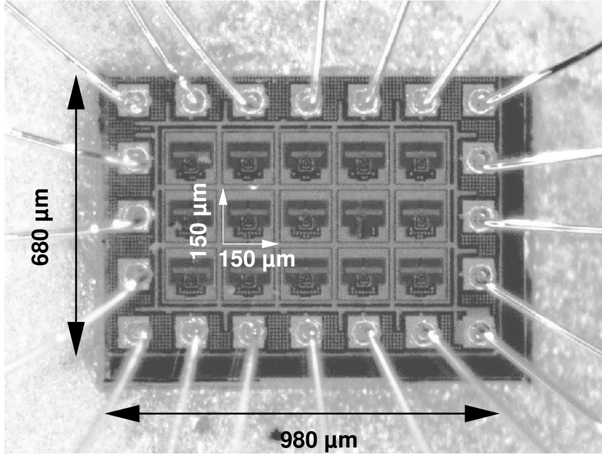

Fig. 3. Chip micrograph of the 3×5 focal-plane array. Its size is 680×980 μm^2 including bondpads.

Each antenna element has an effective area A_{eff}, which can be calculated as

$$A_{\text{eff}} = D\frac{\lambda_0^2}{4\pi}, \qquad (7)$$

where D is the directivity of the radiator. This leads to a single-pixel antenna area of 0.1 mm^2 for a simulated 7-dBi directivity in the broadside direction. Note that the physical area of a pixel is smaller than the antenna area, and hence, the effective antenna areas overlap. Because of this, the available power per pixel is calculated as the physical area times the irradiance produced by the source.

III. Measured Results

Fig. 4 shows the measurement setup for responsivity and noise characterization. A 16.83-GHz source was AM modulated with a 16-kHz square-wave and multiplied by 36 to generate a pulsed 606-GHz signal with a peak power of 1.124 mW. The purpose of the AM modulation is to facilitate detection in the prescence of a dc-offset and a $1/f$ noise floor. A 22-dBi (estimated) horn antenna was used to illuminate the FPA with an intensity of 18.3 μW/mm^2 at a distance of 3 cm. The intensity was calculated from the measured radiation pattern, where the surface integral was normalized to the total power available from the source. The intensity in the center of the beam was verified using Friis transmission equation for the 22-dBi horn antenna at a 3 cm distance. This leads to an available power per physical pixel area of 0.4 μW. A lock-in

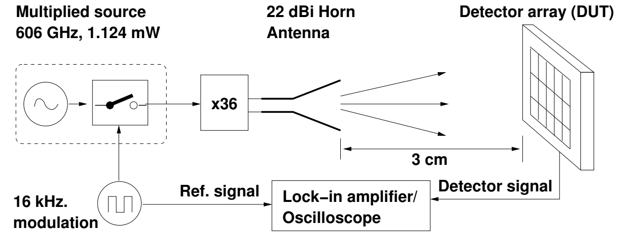

Fig. 4. Measurement setup.

amplifier (LIA), tuned to the modulation frequency of 16 kHz, was used to measure the pixel output voltage and noise level. The pixel output waveform captured with an oscilloscope is

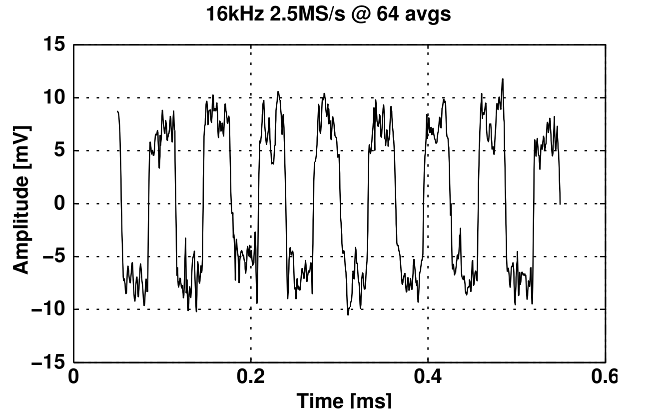

Fig. 5. Captured pixel output waveform at 2.5 MSamples/s with an average of 64 traces. The 16-kHz square-wave modulated 606-GHz signal had a power density of 18.3 μW/mm^2 (0.4 μW/pixel).

shown in Fig. 5. It is sampled with 2.5 MS/s over 16 sweeps while it was illuminated with a 16-kHz square-wave modulated 606-GHz signal. In typical video applications a band-pass filter is used around the modulation frequency to improve the signal-to-noise-ratio accordingly. The responsivity, defined as the ratio between the detected voltage and the power available per pixel, is shown in Fig. 6 as a function of the FET dc bias voltage V_{gs}. The measured peak responsivity is 50 kV/W at a 350-mV V_{gs} bias. Note that this is below the 500-mV FET threshold voltage. The simulated peak responsivity is 90 kV/W and its shape and peak position correlates well with the measurements. The minor signal reduction can partly be explained by EM-modeling inaccuracies of the antenna, and the fact, that the device and parasitic models are used outside their specified frequency range.

Measured and simulated NEPs are shown in Fig. 7 versus V_{gs}. The measured minimum NEP (400 pW/$\sqrt{\text{Hz}}$) is slightly higher than the simulated NEP (150 pW/$\sqrt{\text{Hz}}$) due to a lower measured responsivity. Simulations show that the minimum NEP without amplifier drops to about 60 pW/$\sqrt{\text{Hz}}$ (not shown). Note that the V_{gs} bias differs for minimum NEP and maximum R_v. This is caused by a higher channel conductivity which improves the resistive noise voltage but degrades the responsivity R_v.

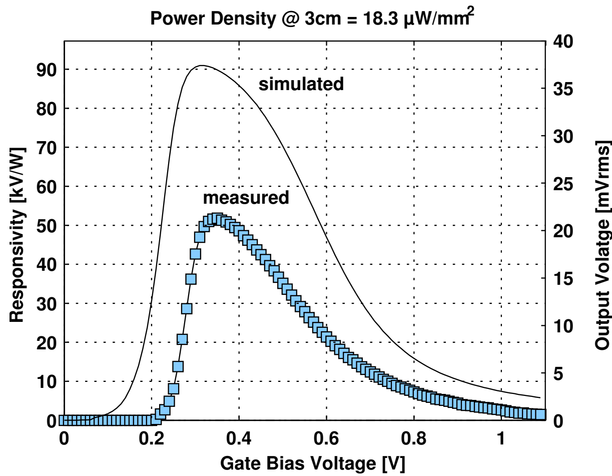

Fig. 6. Measured and simulated pixel responsivity (R_v) at 606 GHz versus the FET V_{gs} bias voltage. The power density was 18.3 μW/mm^2 (0.4 μW/pixel).

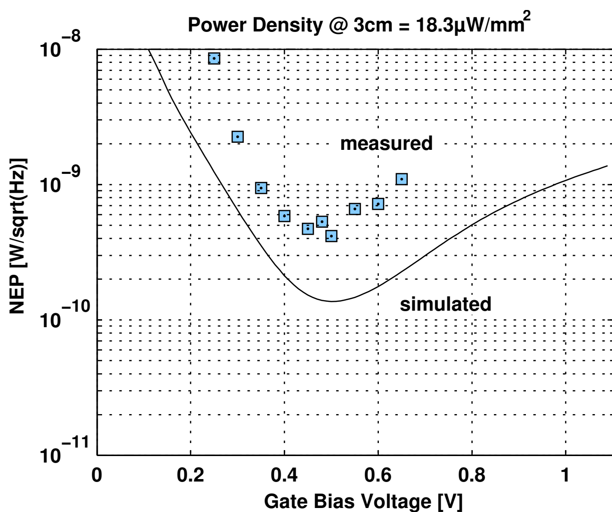

Fig. 7. Measured and simulated pixel NEP at 606 GHz versus the FET V_{gs} bias voltage. The power density was 18.3 μW/mm^2 (0.4 μW/pixel).

IV. Conclusion

A 3×5 600-GHz single-chip focal-plane array (FPA) has been presented. The FPA has been fully integrated in a 0.25-μm CMOS process technology. The array achieves a room temperature responsivity of 50 kV/W and a noise equivalent power (NEP) of 400 pW/$\sqrt{\text{Hz}}$ at 16 kHz. This performance is comparable with that of commercially available Golay cells (200-400 pW/$\sqrt{\text{Hz}}$, 45-10 kV/W @ 10-70 Hz [6]). The simulated minimum NEP of the detector without on-chip amplifier is about 60 pW/$\sqrt{\text{Hz}}$. The FPA is not thermal-time-constant limited and allows for a large modulation bandwidth of 1.6 MHz. As such, it will enable video-rate imaging applications at 600 GHz in a low-cost CMOS process technologies and leads to the construction of terahertz cameras which makes terahertz imaging practical for a wide range of high-profile applications.

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