Scaled spintronic logic device based on domain wall motion in magnetically interconnected tunnel junctions

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***Abstract*—** We present a scaled device based on magnetic domain wall (DW) transport for logic applications. The device consists of multiple magnetic tunnel junctions (MTJs) connected by the same magnetic free layer (FL). Magnetic domain walls are injected by spin-transfer torque (STT) at the input MTJs and are sensed by tunneling magnetoresistance (TMR) at the output MTJ after propagation through the FL. Logic functions can be built by merging several domain walls. By enabling real-time detection of long range DW transport, we demonstrate a spintronic component which can be used for either Boolean or non-Boolean logic.

I. INTRODUCTION

Conventional CMOS is becoming more difficult to scale and is potentially approaching fundamental scaling limits [1]. To circumvent these limitations, non-charge based logic technologies are increasingly explored. Spintronic concepts have the benefit of being intrinsically low-energy and non-volatile, therefore offering attractive properties for future logic devices [2]. One approach is to encode logic information in magnetic domain walls (DW). A DW-based three-terminal device, Fig. 1(a), was recently reported to perform buffer and inverter operations [3], and demonstrate shift register and full-adder circuits [4]. Furthermore, all basic logic functionalities were demonstrated in a magnetic network structure via gate controlled DW trajectory [5].

Here, we report on a scaled, non-volatile magnetic device where a 2nm thin CoFeB-based magnetic free layer can effectively transport information via DW motion between pillars with 150 nm pitch. Magnetic switching is initiated by STT below the first pillar to generate a DW and the motion of the DW is monitored and read in a series of adjacent pillars using the tunnel magneto-resistance (TMR). By generalizing this scheme to various numbers of pillars and geometries of the free layer, logic functions can be built. The Spin-Torque Majority Gate (STMG) in Fig. 1(b) is an example of such a logic device [6]. STMG could offer an advantage in area and energy compared to equivalent CMOS circuits.

II. DEVICE FABRICATION

Top-pinned perpendicular magnetic tunnel junctions (pMTJs) sharing a magnetic free layer (FL) were fabricated in imec's 300-mm CMOS fab with a BEOL-compatible flow (Fig. 2). Detailed information of the full integration flow is available in Ref [7]. Fig. 3(a) depicts the pMTJ stack consisting of a dual-MgO CoFeB-based FL and reference layer (RL) anti-ferromagnetically coupled to a Co/Pt-based hard layer (HL). This stack is the starting point of device fabrication. Of critical importance is the pillar patterning process, which utilizes ion-beam etching (IBE). During this step, the interpillar FL is exposed to ions which could deteriorate crystallinity of the MgO barrier and impact the interface-induced perpendicular magnetic anisotropy (PMA) in the FL. Previous results, showed strong DW pinning due to related process-induced damages [8,9].

We focus on devices consisting of three MTJs of 80 nm diameter separated by 70 nm each, arranged on a strip-shaped common FL of length 450 nm and width 150 nm. See Fig. 3b. A cross-sectional transmission electron micrograph (TEM) of the integrated device in Fig. 3(d) shows the FL spanning the entire device. Energy-dispersive X-ray spectroscopy (EDS) mapping for Mg in Fig. 3(c) confirms a continuous, damage-free dual-MgO FL in between the pillars. EDS mapping for Co indicates remaining RL materials which are necessary for preservation of PMA in the FL during pillar patterning. This is illustrated through wafer level magnetic characterization.

Fig. 4(a) shows magnetic hysteresis loops obtained by Magneto-Optical Kerr Effect (MOKE) microscopy after pillar patterning using different etch conditions (shorter vs longer). The FL is not yet patterned into the strip-shape and can be considered as continuous over the entire wafer. Over-etching (OE) results in a weak signal with high (> 60 mT) coercivity, indicating a fully etched interpillar spacing and magnetically isolated pillars. With a mild under-etch (UE1) condition, the FL is seen to be damaged with a partial in-plane signature. Only an even shorter etch (UE2) leads to an intact FL with acceptable PMA. Note that

under-etch conditions, UE1 and UE2, appear structurally similar in Fig. 4(b), but result in very different magnetic response. About 3.5 nm of material (RL + HL) needs to remain above the MgO to protect it from IBE damage. After a subsequent post etch oxidation, only a small shorting path remains due to the presence of RL between the pillars. Vibrating sample magnetometry (VSM) hysteresis loops in Fig. 5(a) show the additional magnetic moment in the UE2 condition compared to the deposited dual-MgO FL. The extra magnetic moment corresponds to approximately 1 nm of magnetic CoFeB in the RL. In Fig. 5(b), μMOKE imaging in the UE2 condition demonstrates the ability to nucleate and expand a domain in the FL by short field pulses. This confirms that we have a magnetically active FL after pillar patterning (Fig. 2(a)) and that the remaining RL does not hinder domain wall propagation in the FL.

III. RESULTS AND DISCUSSION

A. Three-pillar device magnetic properties

Here, we demonstrate electrically that the interpillar spacing is also magnetically active after FL patterning (Fig. 2(b)) and the full integration. Fig. 6(a) presents the hysteresis curves, TMR versus field, for the three pillars sharing a strip-shaped FL. The parallel (P)- and antiparallel (AP)-state are denoted by ① and ③, respectively. The exact overlap of the switching field, H_C (coercivity), in the three pillars indicates that the FL is effectively one magnetic layer. Additionally, local AP regions can be nucleated by STT. This is the state marked by ② in Fig. 6(b), where the $P \rightarrow AP$ and $AP \rightarrow P$ reversals in P1 and P3 proceed as a function of voltage pulse amplitude. The attained resistance values after AP domain nucleation at P1 and P3 are lower than state ③, due to current spreading to the RL in between the pillars. The AP regions are nucleated close to P1 and P3 as no change in resistance is observed at P2. When starting the TMR versus field loop from state ② in Fig. 6(c), instead of from the full P-state ① in Fig. 6(a), we obtain a lower switching field. This is the depinning field H_D required to move DWs. The fact that $H_D < H_C$, proves successful DW motion through the shared FL from P1 (and/or P3) towards P2.

B. Time-resolved domain wall detection

By performing time-resolved measurements, DW-based nanosecond-scale switching in the shared FL can be captured. Separated MTJs locally probe magnetization in the FL, allowing us to estimate the DW velocity. We quantify the velocity at a low external field. After setting the field, an AP region is nucleated at P1 by STT (pulse width 1 ns). The domain expands along the strip-shaped FL driven by the field. A real-time trace shown in Fig. 7(a), captures the arrival of the domain at P2.

The DW velocity between P1 and P2 was measured ~12000 times to obtain a reliable value. From the histogram in Fig. 7 (b), the DW velocity is estimated to be 9 m/s on average. This velocity is in agreement with published data on DW velocity in CoFeB-based systems [10]. It confirms that the overall integration scheme, including the critical pillar patterning step as well as remaining RL material, do not negatively impact the DW velocity of the magnetic conduit.

Additionally, in Fig. 8(a) we show real-time traces of domain expansion from P1 to both P2 and P3. An AP domain was nucleated at P1 and expands by the external field. DW propagation is sketched in Fig. 8(b). This experiment demonstrates the shift register operation '1-filled left shift' or the arithmetic function $2x + 1$, shown in Fig. 9. Note that each pillar is individually addressable for reading and writing, allowing for other shift operations (right and '0-filled'). Moreover, this device is the first demonstration of domain wall motion through an easily integrated and highly-scaled magnetic conduit shared by multiple MTJs at an aggressive pitch (150 nm). The conduit is perpendicularly magnetized, allowing further scalability and lower power consumption compared to in-plane systems. Reading and writing are performed by TMR and STT, respectively, identical to STT-MRAM technology. Other writing schemes, such as Spin-Orbit Torque (SOT) and Magneto-Electric (ME) polarization, could be implemented to improve the speed and energy efficiency of the devices. These first results show DW motion by external field. However, current-driven DW motion by STT and SOT can be applied as well. By careful stack engineering, the device can be optimized for higher DW velocities. DW velocities up to 750 m/s were reported in a synthetic antiferromagnetic structure driven by current [11] and field-driven DW motion with velocities up to 1700 m/s was achieved in ferrimagnetic materials [12]. These materials will be the excellent candidates for DW propagation based devices.

IV. CONCLUSION

We have demonstrated a fully integrated, scaled, and CMOS production compatible logic device based on magnetic domain wall transport. We present all necessary conditions for successful device fabrication and operation. Through quasi-static and time-resolved measurements, we show that domain walls can be controllably nucleated and propagated between MRAM-like pillars. The demonstration of this working magnetic device at the nanometer scale, enables a robust spintronic platform that will be used for functional silicon-integrated spintronic logic components and applications. This work paves the way towards the realization of spin-based beyond CMOS logic concepts.

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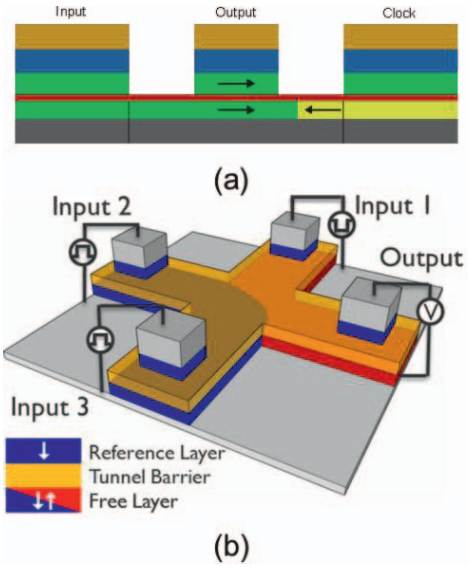


Fig. 1. Interconnected MTJ devices capable of Boolean operations.
(a) Three-terminal device
(b) Spin-Torque Majority Gate

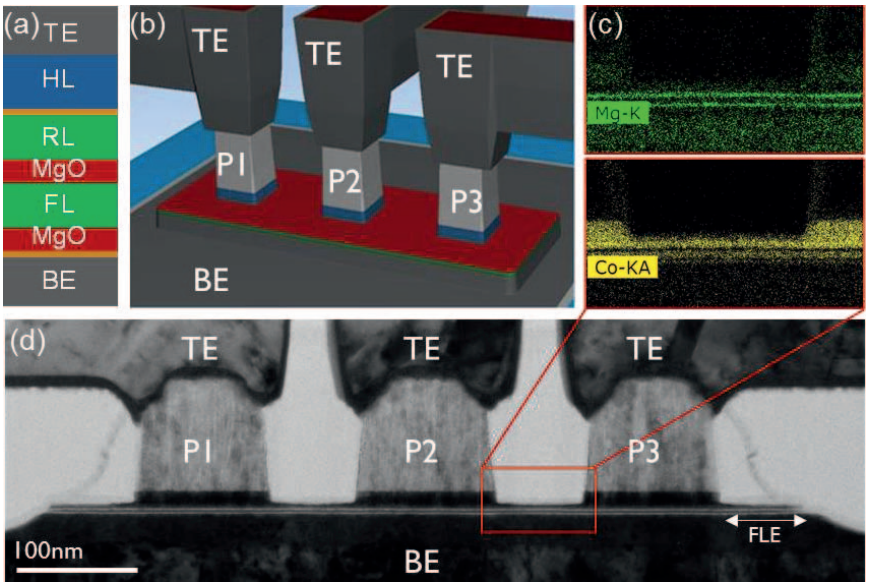


Fig. 3. (a) Top-pinned pMTJ stack – CoFeB-based FL and RL anti-ferromagnetically coupled to Co/Pt based HL (b) 3D view of 3-pillar device (c) EDS mapping showing continuous FL in between pillars (d) TEM cross-section of 3-pillar device showing undamaged dual MgO FL interconnect.

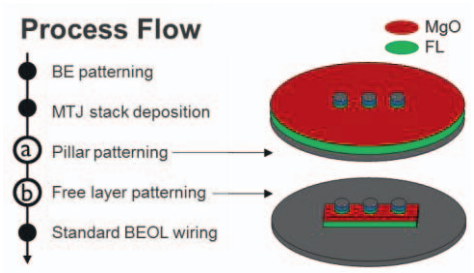


Fig. 2. Dedicated BEOL process flow for MTJs sharing the ferromagnetic FL. Critical step is pillar patterning, where the MgO layer should not be damaged to preserve PMA in the FL interconnect.

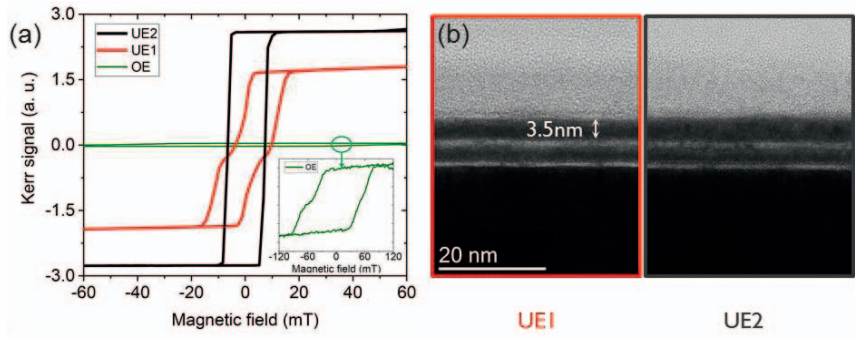
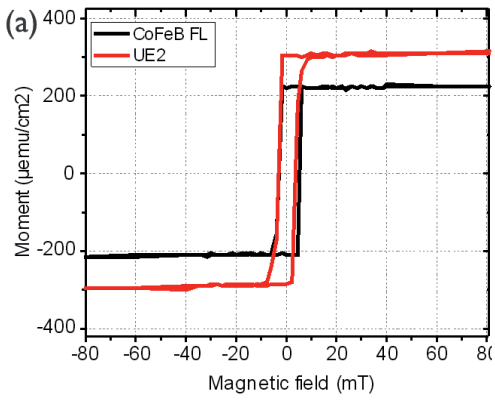


Fig. 4. (a) Magnetic hysteresis curve recorded on dense region of pillars after the critical pillar patterning step. Over-etch (OE) results in a fully patterned FL. A mild under-etch (UE1) condition damages the FL which has a partial in-plane character. A stronger under-etch (UE2) leads to an intact FL with good PMA. (b) UE1 and UE2 structurally look the same but have very different magnetic properties.



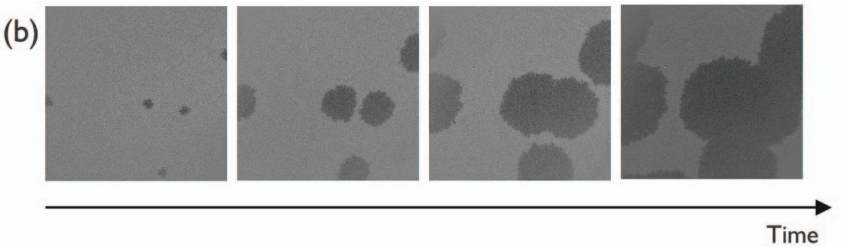


Fig. 5 (a) Hysteresis loops, moment versus field, as recorded by VSM. UE2 shows an additional moment coming for remaining RL, compared to a deposited CoFeB dual-MgO FL. (b) μMOKE image of UE2. A domain was nucleated and expanded by field in the FL. The remaining RL does not hinder the DW motion in the FL.

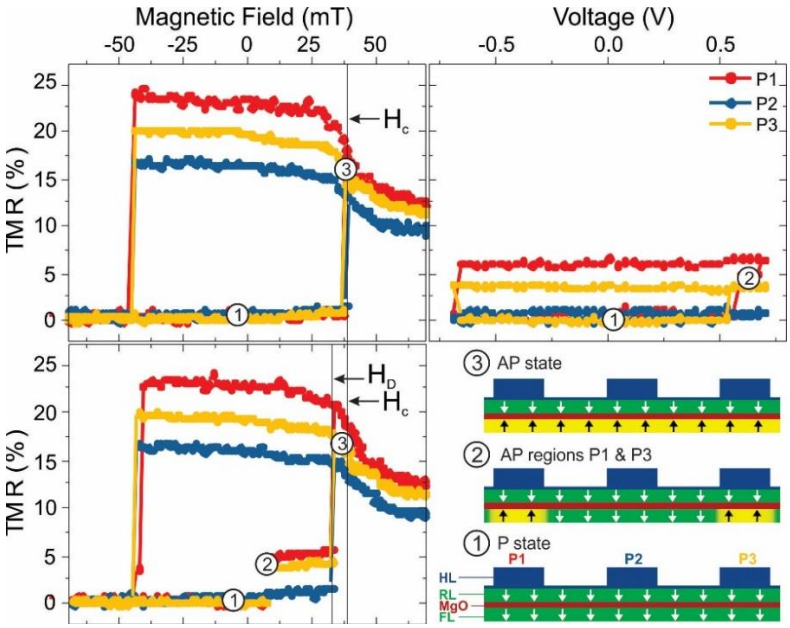


Fig. 6. (a) Hysteresis loop of FL of 3 pillars in the same device. P- and AP-state are denoted by ① and ③. All pillars have the same coercivity, meaning the FL is shared. (b) Local P-AP and AP-P switching at P1 and P3, ②. (c) Comparison of depinning field H_D and switching field H_C where $H_D < H_C$. (d) Sketch of magnetic states in FL and RL for figures (a), (b), (c).

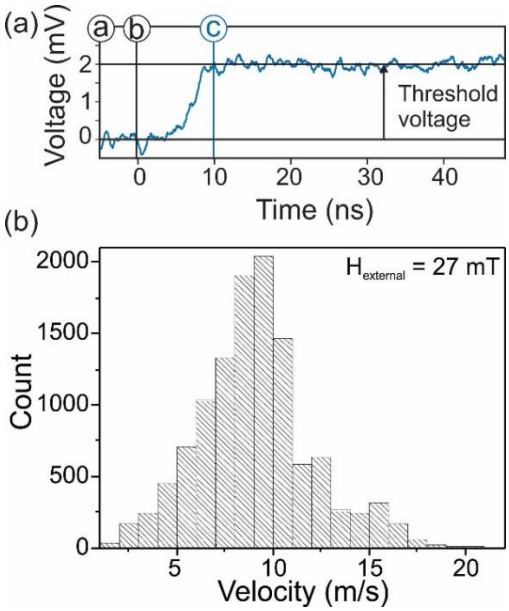


Fig. 7. (a) Smoothed time trace recorded at P2 after an AP region was nucleated at P1 with a 1 ns pulse (at time zero). ⓐ pulse at P1 ⓑ DW arrival at P2 and ⓒ DW passed under P2. (b) Histogram of DW velocity at an external field of 27 mT, below the coercive field. Average DW velocity is 9 m/s between P1 and P2.

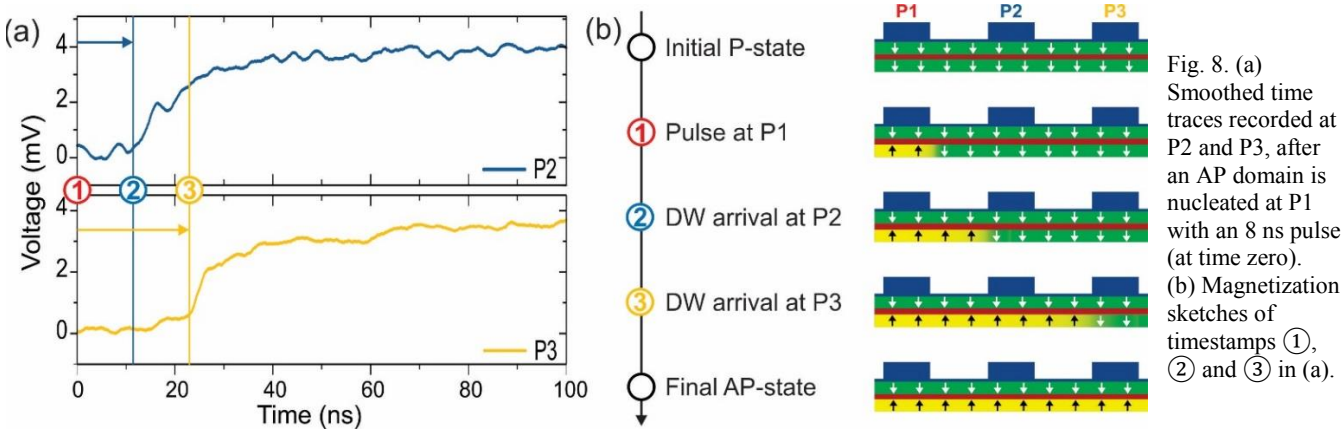


Fig. 8. (a) Smoothed time traces recorded at P2 and P3, after an AP domain is nucleated at P1 with an 8 ns pulse (at time zero). (b) Magnetization sketches of timestamps ①, ② and ③ in (a).

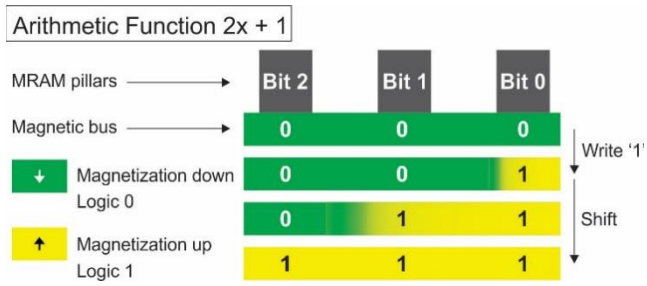


Fig. 9. Three-pillar device acting as a register. Magnetization 'down' and 'up' are logic '0' and '1' respectively. Each pillar is individually addressable for reading and writing. By writing a logic 1 to Bit 0 and domain expansion by field, we perform the arithmetic function 2x+1, as shown in the sketch.

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