UTSOI2: A Complete Physical Compact Model for UTBB and Independent Double Gate MOSFETs

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Abstract

In this paper, we present the first complete compact model dedicated to Ultra-Thin Body and Box and Independent Double Gate MOSFETs based on an explicit formulation of front and back surface potentials that is valid and extremely accurate in all operation regimes. The model provides physics-based consistent description of DC and AC device characteristics; it has been extensively validated against TCAD and hardware data, and fulfills standard requirements from quality assurance and convergence tests for circuit design.

Introduction

Ultra-thin body transistors such as FinFETs or Ultra-Thin Body and Box (UTBB) MOSFETs are required for sub-20nm nodes because of their excellent electrostatic integrity and reduced variability. Compared to FinFET, UTBB technology on thin buried oxide presents two decisive advantages: a much simpler process than FinFET and the possibility to use the backplane bias to optimize the power consumption / speed trade-off at circuit level [1,2]. To take full advantage of this latter benefit, circuit designers need compact models that describe properly the transistor behavior for a wide range of back bias. In previously reported works on complete compact models, the interface between the body and the buried oxide is assumed always depleted [3,4], which provides correct results in reverse and low forward back bias (FBB) range. However, when a strong FBB is applied, inversion occurs first at the back interface [5], which has a significant impact on device characteristics (Fig.1). In this paper, we present a complete surface potential compact model dedicated to such Independent Double Gate (IDG) device operation.

Calculation of surface potentials

Calculation of interface potentials is a key issue in the modeling of IDG MOSFET [6-10]. While an iterative resolution of Poisson's equation is used in [11], we have developed here a very accurate direct calculation of interface potentials.

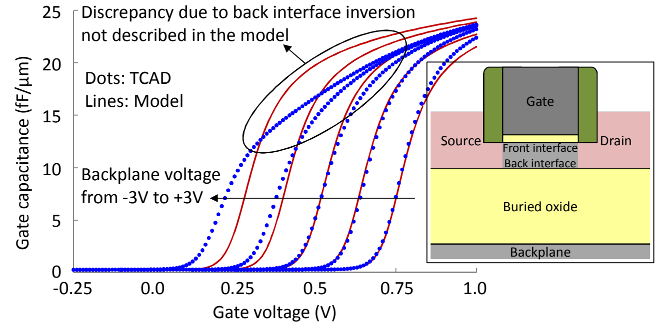

Fig.1- Impact of back interface inversion on C(V) characteristics (t_{ox}=1nm, t_{Si}=6nm, t_{box}=20nm). Dots: TCAD. Lines: Model assuming back interface always depleted [4]. Inset: Schematic description of UTBB transistor.

With notations defined in Table 1, we obtain three coupled equations (1)-(3) from the integrations of Poisson's equation and boundary conditions, as in [10], but with a different form for equation (3).

Table 1- Notations used in this work

Symbol	Definition
ϕ_T	Thermal voltage
c_{ox}	Gate oxide capacitance per area unit ($=\varepsilon_{ox}/t_{ox}$)
c_{box}	Buried oxide capacitance per area unit ($=\varepsilon_{ox}/t_{box}$)
c_{Si}	Thin body capacitance per area unit ($=\varepsilon_{Si}/t_{Si}$)
x_{g1}	Gate electrostatic potential normalized to ϕ_T
x_{g2}	Backplane electrostatic potential normalized to ϕ_T
x_n	Quasi-Fermi level normalized to ϕ_T
q_1	Gate charge density normalized to $c_{ox}\phi_T$
q_2	Backplane charge density normalized to $c_{box}\phi_T$
q_i	Inversion charge density normalized to $c_{Si}\phi_T$
k_1	Gate oxide over thin body capacitance ratio ($=c_{ox}/c_{Si}$)
k_2	Buried oxide over thin body capacitance ratio ($=c_{box}/c_{Si}$)
A_0	$2qn_it_{Si}^2/(\varepsilon_{Si}\phi_T)$, with n_i the intrinsic carrier density

$$q^2 = k_1^2 q_1^2 - A_0 e^{-x_n} e^{x_{g1} - q_1} \quad (1)$$

$$q^2 = k_2^2 q_2^2 - A_0 e^{-x_n} e^{x_{g2} - q_2} \quad (2)$$

$$q \coth(q/2)(k_1 q_1 + k_2 q_2) + k_2 q_2 k_1 q_1 + q^2 = 0 \quad (3)$$

With the latter formulation, the need to know a priori if the solution lies in the hyperbolic (q real) or trigonometric (q

imaginary) mode [12] is no more required. Indeed, the term qcoth(q/2) is a function of q^2 that ensures a natural transition from $q^2>0$ to $q^2<0$ (where it becomes Im(q)cot(Im(q)/2)). From this set of equations, we can work with real unknowns only (q_1, q_2 and q^2) and build a unique equation (4) to be solved with q_1 as a variable.

$$(k_1 q_1 + q\coth(q/2))(k_1 q_1 + k_2 q_2) - A_0 e^{-x_n} e^{x_{g1}-q_1} = 0 \qquad (4)$$

In (4), q^2 and q_2 are defined as functions of q_1 by (1) and (5), respectively, where (5) results from a combination of (1)-(3).

$$\begin{aligned} q_2 &= x_{g2} - x_{g1} + q_1 \\ &+ 2\ln(k_1 q_1 + q\coth(q/2)) - \ln\left(q^2/\sinh(q/2)^2\right) \end{aligned} \qquad (5)$$

Then, thanks to a robust analytical procedure involving three successive corrections on q_1 based on a 2nd order Taylor development of (4) (similar to PSP procedure [13]), the front interface potential x_{g1}-q_1 is obtained with accuracy better than 10 feV (Fig.2).

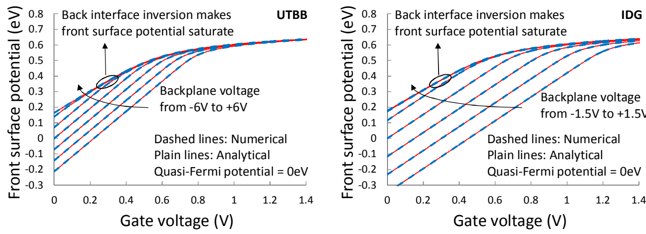

Fig.2- Surface potential as a function of gate voltage for different backplane biases. UTBB (t_{ox}=1nm, t_{Si}=7nm, t_{box}=25nm) (left) and IDG (t_{ox}=1nm, t_{Si}=7nm, t_{box}=1nm) (right) transistors. Comparison between analytical (plain lines) and numerical calculations (dashed lines). Error is less than 10 feV.

Current model

In surface potential models, the drain current computation is usually based on the linear dependence of the inversion charge density on the surface potential [4,14]. In an IDG transistor, the front interface potential is not relevant to compute the current when the charge centroid is at the back interface and vice versa. Thus, we need to define an effective electrostatic potential (called x_{drift}), whose longitudinal gradient governs the drift current whatever the position of the charge centroid. Starting from the total drain current expression and separating the diffusion and the drift components, we identify x_{drift} (to a given additive constant) as: $x_{drift}=x_n+\ln(-q_i)$. Then, we notice that the linear relationship between q_i and x_{drift} is valid in all regimes except in saturation when both front and back channels are created at source side (Fig.3). Indeed, in that case, the $q_i(x_{drift})$ curve presents two distinct slopes. The change of slope occurs at the point where the weakest channel is pinched-off.

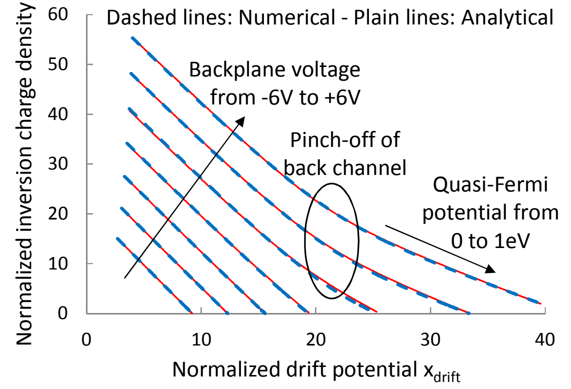

Fig.3- Inversion charge along the channel versus effective potential for different backplane biases. At forward back bias, the curve shows two slopes before and after pinch-off of the weakest channel.

Thus, we generalize the concept of inversion charge linearization by modeling q_i as a maximum function of these two linear dependences (Fig.3, analytical model). The so-defined function is analytically integrated to obtain the drain current equation. The sequence consists in computing successively 1) surface potential, inversion charge and effective electrostatic potential at source side, 2) effective drain voltage, including velocity saturation effect, 3) surface potential, inversion charge and effective potential at drain side, 4) drain current, including quantum confinement, series resistance, saturation velocity and channel length modulation effects. The physical background of the short channel effects model is described in Fig.4.

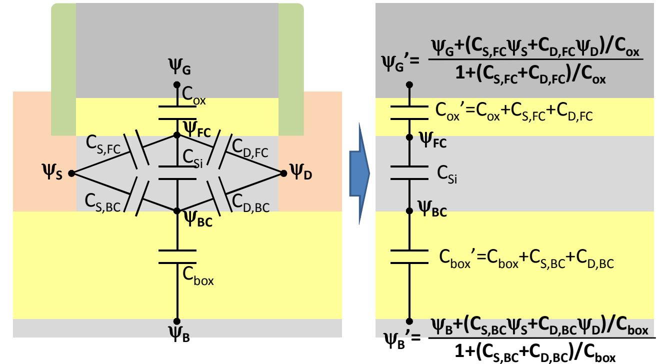

Fig.4- Modification of the effective device geometry and applied biases to account for short channel effects. $C_{S,FC}$ (resp. $C_{D,FC}$) and $C_{S,BC}$ (resp. $C_{D,BC}$) refer to the capacitive coupling between source (resp. drain) and front or back interface, respectively.

It consists in a modification of effective device geometry and applied biases, in such a way that correct short channel surface potentials are obtained with the 1D surface potential computation procedure. Similarly, quantum confinement in subthreshold regime is taken into account through a modification of device effective geometry prior to surface

potential calculation (Fig.5). In a second step, a corrective factor is applied to drain current and charges to refine the calculation in the strong inversion regime. Such implementation of short channel and quantum effects ensures a consistent description of DC and AC device characteristics.

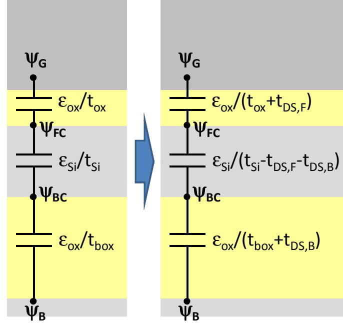

Fig.5- Modification of effective device geometry to account for quantum confinement. $t_{DS,F}$ and $t_{DS,B}$ refer to bias dependent front and back interface dark-spaces, respectively.

Furthermore, backplane depletion effect is also accounted for through an effective backplane bias. Fig.6 and 7 illustrate the excellent predictability of this DC model core, validated against TCAD simulations in which quantum effects are accounted for through an effective potential approach calibrated on Poisson-Schödinger simulations.

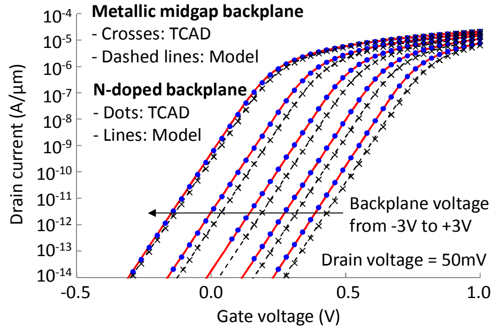

Fig.6- Predictability of the DC model. Same parameters for model and TCAD. Transfer characteristics of a UTBB MOSFET (t_{ox}=1nm, t_{Si}=6nm, t_{box}=20nm), with metallic (crosses: TCAD - dashed lines: model) and N-doped (dots: TCAD - lines: model) backplanes.

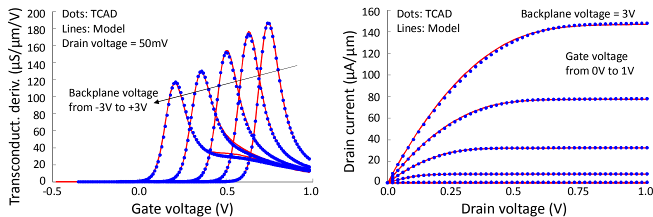

Fig.7- Predictability of the DC model. Same parameters for model (lines) and TCAD (dots), with constant mobility. Transconductance derivative with respect to gate voltage (left) and output characteristics at forward back bias of +3V (right) of a long channel UTBB MOSFET with an N-doped backplane (t_{ox}=1nm, t_{Si}=6nm, t_{box}=20nm).

Gate leakage and GIDL/GISL current models similar to those of UTSOI1 [4] are also included.

Charge and noise model

The intrinsic charge model is based on the effective gate charge concept from [15]. Noticing that the effective gate charge densities $\hat{q}_1$ and $\hat{q}_2$ are actually given by (6), the intrinsic charges computation is straightforward in our model, most of the required quantities being already computed for the drain current.

$$\hat{q}_j = \frac{q_i}{d\left(k_j q_j\right)/dx_n} \quad \text{for } j = 1 \text{ and } j = 2 \tag{6}$$

UTSOI2 includes also overlap, fringe and source/drain/gate to backplane parasitic capacitances. Predictability of this AC model is also excellent, as illustrated in Fig.8. Furthermore, a dedicated noise model is implemented. This model includes flicker, thermal, induced gate and shot noise components.

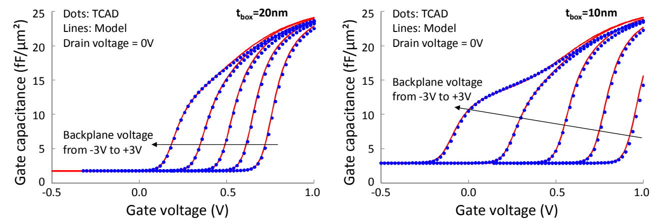

Fig.8- Predictability of the AC model. Same parameters for model (lines) and TCAD (dots). Long channel gate capacitance versus gate voltage for various backplane biases (t_{ox}=1nm, t_{Si}=6nm) for t_{box}=20nm (left) and t_{box}=10nm (right).

Model validation and readiness

Fig.9 to 11 present a comparison between the model and measurements carried out on UTBB transistors from STMicroelectronics. C(V) and I(V) characteristics, as well as their derivatives, are accurately reproduced over a wide back bias range.

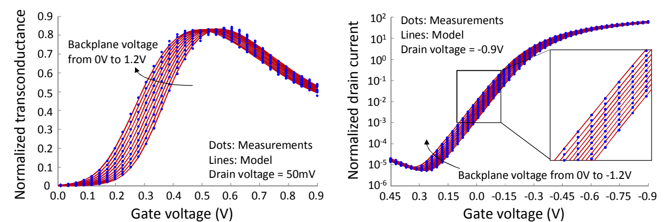

Fig.9- Comparison between model (lines) and measurements (dots). Normalized linear transconductance (left) and saturation drain current (right) versus gate voltage for various backplane biases. 20nm gate length MOSFETs (t_{Si}=6nm, t_{box}=25nm). Drain current is normalized to $2n\mu c_{ox}W/L\phi_T^2$ and transconductance to $2n\mu c_{ox}W/L\phi_T$, with n the subthreshold slope factor.

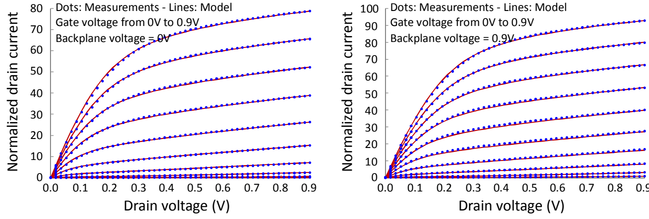

Fig.10- Comparison between model (lines) and measurements (dots) on output characteristics of a 20nm gate length nMOSFET (t_{Si}=6nm, t_{box}=25nm) at zero back bias (left) and 0.9V back bias (right).

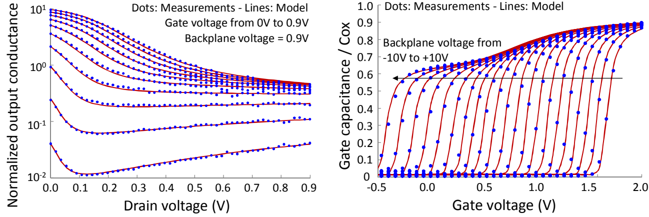

Fig.11- Comparison between model (lines) and measurements (dots) on output conductance of a 20nm gate length nMOSFET (t_{Si}=6nm, t_{box}=25nm) at 0.9V back bias (left). Measured gate capacitance is accurately modeled over a wide back bias range (-10V to +10V) (right).

In particular, the C(V) characteristic in Fig.11 illustrates the accuracy of the model for back biases as high as 10V applied on a device with a 25nm Box. Furthermore, this model is compliant with continuity, symmetry and robustness criteria of standard compact models [16], as shown in Fig.12 (left). Finally, to illustrate the suitability of UTSOI2 for circuit simulations, Fig.12 (right) shows the results of ring oscillator simulations for various back bias and supply voltages.

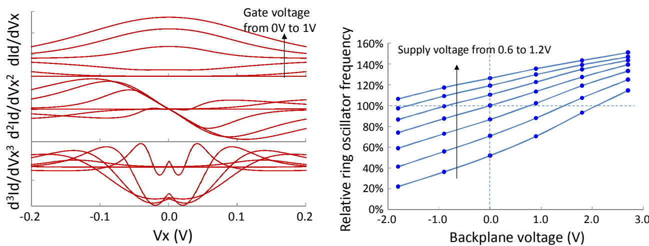

Fig.12- Left: Illustration of UTSOI2 compliance with Gummel symmetry test. First three drain current derivatives as a function of Vx for various gate voltages. Right: Relative dependence of ring oscillator frequency (fan-out=3) versus back bias for various supply voltages. Reference frequency is taken at null backplane voltage and V_{dd}=0.9V.

Conclusion

In this paper, we have presented UTSOI2, a complete physical compact model dedicated to UTBB technology and able to describe accurately independent double gate operation in all conditions including strong back bias. The physical background of this model makes it consistent over DC/AC characteristics, predictive over technological parameters, and all included effects make it suitable for sub-20nm UTBB technologies. Accuracy is validated against TCAD and hardware data, and standard Quality and Robustness tests are successfully met for circuit design applications.

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