

### 28.3 A 606 $\mu$ W mm-Scale Bluetooth Low-Energy Transmitter Using Co-Designed 3.5 $\times$ 3.5mm<sup>2</sup> Loop Antenna and Transformer-Boost Power Oscillator

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Wireless communication has been a limiting factor for achieving millimeter-sized wireless sensor nodes because of the high power consumption, large antenna size and off-chip components typically required. Several mm-scale radios have been proposed [1-3]; however, all use proprietary communication protocols, which afford their designers more flexibility to address the above challenges. For interoperability and ubiquitous adoption, it is important that mm-scale radios use standard protocols, such as Bluetooth Low Energy (BLE). However, implementing a BLE-compliant radio in a mm-scale form factor poses significant additional challenges. These include the requirements for center frequency deviation (<150kHz), FSK modulation accuracy and frequency drift during the packet (<50kHz), which drive up the power consumption of typical PLL+VCO+PA BLE transmitters to >3mW [4-5]. A 0.5mW BLE transmitter was achieved by relaxing these requirements, but suffered from high phase noise due to its low-power ring oscillator [6].

In this work, we propose several techniques to realize a mm-scale BLE transmitter and antenna consuming only 606 $\mu$ W. To achieve this, we employ a front-end based on a power oscillator with a high-Q resonator formed by a printed 3.5 $\times$ 3.5mm<sup>2</sup> inductive loop antenna (sim. Q~110) and an on-chip digitally switched capacitor array (sim. Q~283). The power oscillator (Fig. 28.3.1) replaces the traditional VCO plus PA, achieving lower power consumption while maintaining phase noise of -118.5dBc/Hz at 1MHz offset that results in low FSK modulation error (2.1%) and low frequency drift during the BLE packet (<10kHz). We propose a transformer-boost technique for the power oscillator that improves output power by 1.2 $\times$  and power efficiency by 3.16 $\times$  compared to a conventional Class-B architecture, resulting in an overall transmit efficiency of 23.6%. The center frequency is digitally controlled using an on-chip digitally switched capacitor array resonating with the inductance of the loop antenna, and achieves a 32.2kHz frequency resolution required for BLE standard compliance. The loop antenna is 3.5 $\times$ 3.5mm<sup>2</sup>, which gives an optimal trade-off between antenna gain and the required on-chip capacitance to resonate the antenna. Finally, a compact ADPLL realizes fast center frequency settling (<15 $\mu$ s), operates only during frequency settling and is powered off when transmitting the BLE packet to reduce overall energy consumption. The proposed BLE transmitter, including a CMOS chip and a 3.5 $\times$ 3.5mm<sup>2</sup> loop antenna, consumes 606 $\mu$ W when transmitting a 368 $\mu$ s advertising packet. It is incorporated in a 4.5 $\times$ 18.6mm<sup>2</sup> fully self-contained wireless circuit board powered by a mm-scale coin battery that we used to demonstrate BLE advertising to typical mobile phones with >8m distance.

The overall architecture of the proposed BLE transmitter is shown in Fig. 28.3.1. An electrically-small size (0.028 $\lambda$ ) magnetic dipole antenna is chosen because it achieves better efficiency than an electric dipole when considering the Q of on-chip passives for resonating [1]. Thus, a 3.5 $\times$ 3.5 mm<sup>2</sup> loop antenna was implemented on a Rogers 4003C PCB with -15dB omnidirectional gain. Figure 28.3.2 shows the HFSS model and simulation results of the antenna including bonding wires, chip pads and silicon substrate. The simulated capacitance to resonate this antenna at 2.4GHz is ~680fF, which is sufficiently large to implement a digitally controlled capacitor array on-chip with practical tuning range and provides margin for parasitic capacitance.

The Q-factor of the digitally controlled capacitor array is critical to transmit efficiency, and hence the equivalent series resistance (ESR) of the resonant capacitance must be kept at a minimum. At the same time, the capacitance resolution and tuning range must meet the BLE standard. To co-optimize capacitor resolution and Q-factor, we use a coarse capacitor array with 1.02fF unit cap, achieving ~110MHz range to cover the BLE bandwidth. Then, a 6b fine capacitor array with 16.8aF tuning resolution achieves 32.2kHz resolution for BLE channel selection and another 6b modulator capacitor array has 22.6kHz resolution for GFSK modulation. Each unit capacitor consists of MOM capacitors (PDK available) and NMOS switches. LVT transistors with a large W/L ratio are used to reduce unit ESR. The top two metal layers are 2.5 $\mu$ m wide to reduce ESR overhead and are alternately used for adjacent parallel wires to minimize parasitic coupling capacitance.

A traditional Class-B power oscillator uses a tail current source, similar to a differential LC oscillator [1]. Figure 28.3.3 (bottom, right) shows that peak

transmit efficiency of 28% is reached when the tail current is tuned to the cross-over between current-limited and voltage-limited regions. However, output power is low, only 22 $\mu$ W. To increase output power, tail current can be increased, but this causes efficiency to drop dramatically (13% @ 45 $\mu$ W). Entirely removing the current source results in maximum power of 75 $\mu$ W, limited only by supply voltage, but the efficiency is even lower at 8.8%. To achieve higher output power and efficiency we propose a transformer-boost technique (Fig. 28.3.3, left). A transformer replaces the tail current sources on the top and bottom of the cross-coupled pair, forming two resonant tanks with tunable capacitor arrays at 4.8GHz. The resonant tanks filter out frequency components of current other than 4.8GHz, which contribute to loss. Through the transformer's magnetic coupling, it also boosts the virtual supply (V<sub>TOP</sub> and V<sub>BOT</sub>), increasing oscillation swing by 1.3 $\times$ , resulting in 90 $\mu$ W output power with 28% transmit efficiency. The transformer was implemented on-chip using a top metal layer achieving k=0.75 and Q=12. The measured output power is -8.4dBm with 27% efficiency due to the degraded Q-factor of the loop antenna.

The proposed transmitter utilizes open-loop GFSK modulation for energy saving. When the BLE packet is ready, the ADPLL locks the frequency of the digitally controlled power oscillator (DCPO) within 15 $\mu$ s. An on-the-fly lock detector monitors the DCPO control word and, upon lock, disables the ADPLL and starts the GFSK modulator of the packet with the DCPO operating in open-loop. The open-loop nature eliminates the need to implement a high-resolution TDC; instead we implemented an injection-locked TDC based on a 12-phase pseudo-differential ring oscillator to avoid DCPO period calibration. The GFSK modulator is implemented as an oversampled (8 $\times$ ) interpolative digital filter where the output frequency during the current bit is determined considering both preceding and following bits. The look-up table of the modulator array control word is pre-calibrated for open-loop modulation.

The proposed BLE transmitter was fabricated using 65nm CMOS. Figure 28.3.7 shows the chip micrograph with 0.49mm<sup>2</sup> active area. The chip is integrated in a 4.5 $\times$ 18.6mm<sup>2</sup> prototype wireless board with custom loop antenna (Fig. 28.3.4). When operating using a 5.8mm coin battery, the self-contained transmitter generates -23.4dBm EIRP, wirelessly measured using a horn antenna (LB-530-NF). The proposed transmitter chip consumes an average power of 606 $\mu$ W dominated by the power oscillator with packet-level duty cycling. The only necessary off-chip component is a 16MHz crystal oscillator whose power can be as low as 30 $\mu$ W [8].

Figure 28.3.4 shows that measured phase noise of the power oscillator is -118.5dBc/Hz at 1MHz offset consuming 534 $\mu$ W. Measured relative 2<sup>nd</sup>- and 3<sup>rd</sup>-harmonic power is -47dBc and -52dBc, respectively (both below BLE requirement of -41.5dBc). Figure 28.3.5 shows measured results of BLE modulation. The BLE spectral mask is met and FSK error is only 2.1%. The measured transient response of the DCPO frequency shows that the frequency drift is below 10kHz during a 368 $\mu$ s BLE packet, which is within the BLE specification (<50kHz). Figure 28.3.6 shows a comparison with recent low-power transmitters.

#### References:

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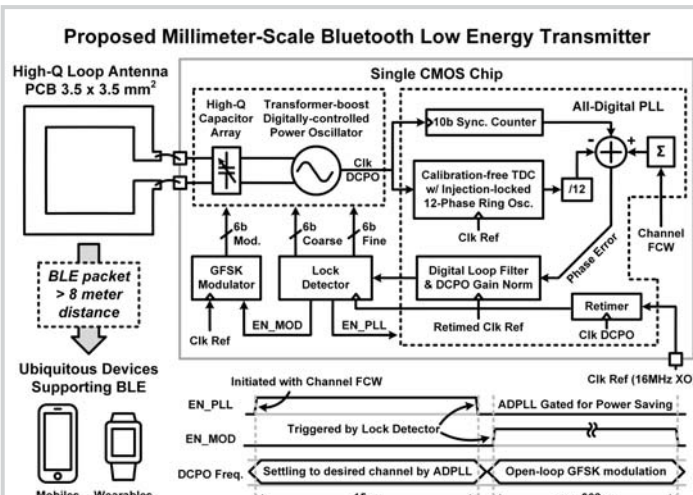


Figure 28.3.1: Architecture and timing of proposed millimeter-scale BLE transmitter consisting of 3.5x3.5mm<sup>2</sup> high-Q printed loop antenna and single CMOS chip.

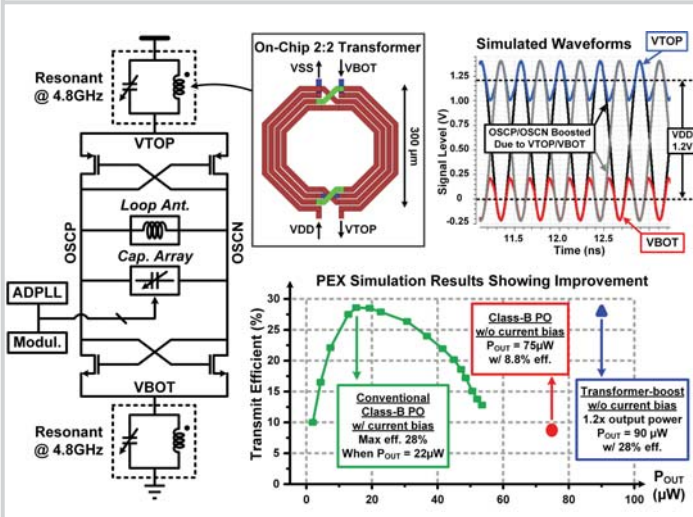


Figure 28.3.3: Proposed transformer-boost power oscillator for boosted output power with enhanced transmit efficiency.

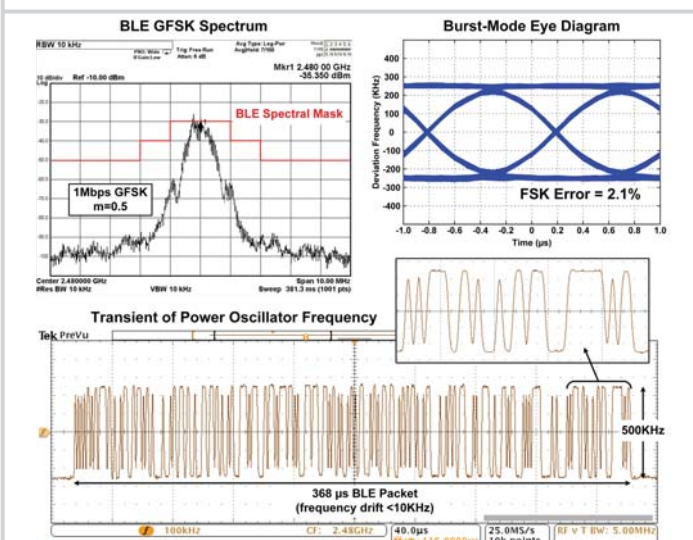


Figure 28.3.5: Measured performance of BLE GFSK modulation: continuous-mode spectrum, eye diagram, and transient.

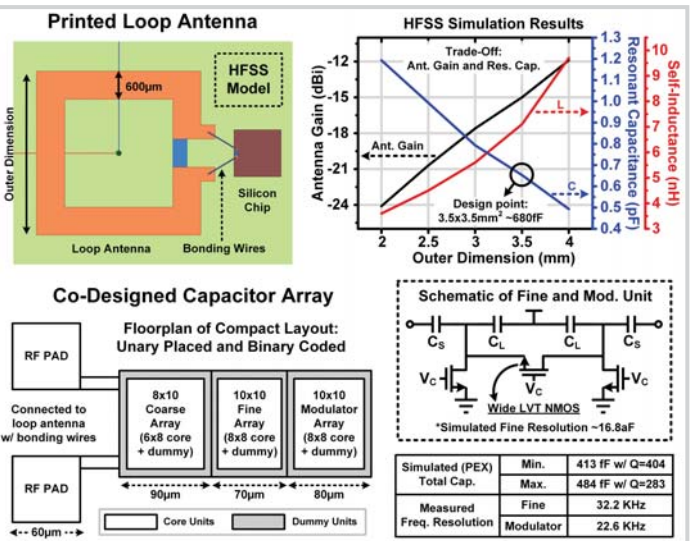


Figure 28.3.2: Co-design of loop antenna and capacitor array for high-Q resonator and BLE compliance.

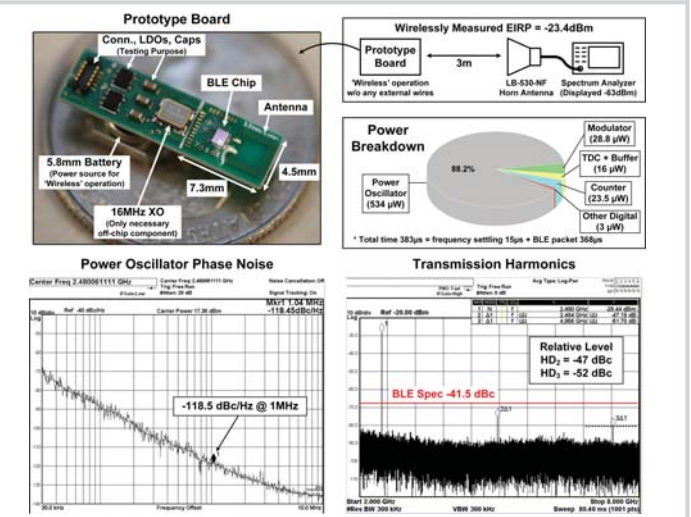


Figure 28.3.4: EIRP measured using the prototype wireless board. Transmitter power breakdown with packet-level duty cycling. Measured phase noise and transmission harmonics of the digitally controlled power oscillator.

	This Work	ISSCC 2017 [1]	JSSC 2015 [2]	JSSC 2016 [4]	ISSCC 2015 [5]	RFIC 2018 [6]	JSSC 2011 [7]
Technology	65 nm	180 nm	65 nm	28 nm	40 nm	40 nm	130 nm
Co-Designed Antenna	3.5x3.5 mm <sup>2</sup> Planar Loop	3x3x2 mm <sup>3</sup> 3D Loop	2.5 mm On-Chip Dipole	N/A	N/A	N/A	N/A
Carrier Frequency	2.4 GHz	915 MHz	60 GHz	2.4 GHz	2.4 GHz	2.4 GHz	400MHz
Modulation	GFSK	PPM	Proprietary	BLE	BLE	BLE	MCS
Date Rate	1 Mbps	30.3kbps	1.2 Mbps	1 Mbps	1 Mbps	1 Mbps	200 kbps
Supply Voltage	1.2 V	4 V	0.9 V	0.5/1 V	1 V	0.6 V	N/A
Power Consumption	0.61 mW <sup>1</sup>	2 mW	11 mW <sup>4</sup>	3.6 mW	4.2 mW	0.49 mW	0.09 mW
Energy Per Bit	0.61 nJ/b	66 nJ/b	9.1 nJ/b	3.6 nJ/b	4.2 nJ/b	0.49 nJ/b	0.45 nJ/b
TX Output Power	-8.4 dBm <sup>2</sup>	-2 dBm	-3 dBm	0 dBm	-2 dBm	-19 dBm	-17 dBm
Overall Efficiency	23.6%	32.4% <sup>3</sup>	4.5%	28%	15%	2.6%	22%
Modulation Error	2.1%	N/A	N/A	2.7%	4.8%	9%	N/A
Osc. Phase Noise @ 1MHz (dBc/Hz)	-118.5	N/A	N/A	-116	-110	-85	-104 <sup>5</sup>
Spur Level	HD2 (dBc) -47, HD3 (dBc) -52	N/A	N/A	-50	-47	-42	N/A

<sup>1</sup> Average power for transmitting one BLE packet w/ open-loop modulation. Power of external commercial XO is not included.  
<sup>2</sup> Calculated based on wireless testing results: EIRP -23.4dBm and simulated antenna gain -15dBi (omni-directional).  
<sup>3</sup> Power oscillator only and high-Q off-chip capacitor used.  
<sup>4</sup> Calculated based on simulated results: 250pC total charge for 3 pulses (width 600ps) from 0.9V supply.  
<sup>5</sup> Measured phase noise of frequency multiplier output.

Figure 28.3.6: Comparison with recent low-power transmitters.

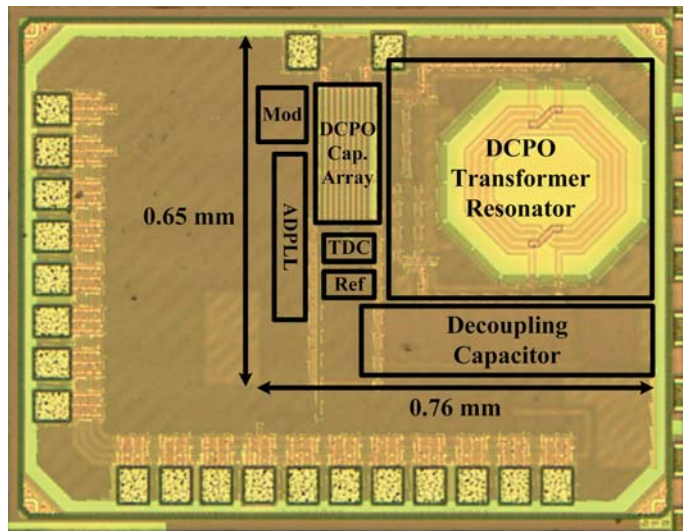


Figure 28.3.7: Die micrograph.