60 GHz Transmitter Circuits in 65nm CMOS

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***Abstract* — This work presents fundamental building blocks for a 60GHz transmitter front-end. The circuits are implemented in a 65nm bulk CMOS technology, operate from a 1.2V supply, and attain state-of-the-art performance for multi-Gb/s wireless applications. A single-stage, single-ended, power amplifier achieves peak power gain of 4.5dB, output 1dB compression point of 6dBm, saturated power of 9dBm, and peak power added efficiency of 8.5% at 62GHz. A double-balanced, Gilbert-based, up-conversion mixer achieves 6.5dB of conversion loss and output 1dB compression point of -5.0dBm with LO of 50GHz and IF of 10GHz. Millimeter-wave design considerations and measurements over frequency and temperature are discussed.**

***Index Terms* — Power amplifier, up-conversion mixer, millimeter-wave, wireless transmitter, CMOS.**

I. INTRODUCTION

The availability of silicon IC technologies capable of operating in the millimeter-wave (mmWave) range, and the commercial interest in high speed wireless applications has motivated the development of integrated 60 GHz transceivers. In SiGe BiCMOS, complex and fully integrated transmitter and receiver circuits capable of multi-Gb/s data transmission in the 60 GHz band have already been demonstrated [1]. As a natural evolution towards a 60 GHz system-on-chip (SoC), different mmWave building blocks and sub-systems have been investigated using deep sub-micron CMOS technologies. So far, most of the attention in this exploratory work has been devoted to receiver circuits [2-4], where a good level of integration and performance has been achieved. Nevertheless, the performance of large signal circuits with nanometer CMOS devices at mmWave frequencies is less understood. The power delivery capability, linearity, and efficiency of transmitter front-end building blocks are critical for the overall performance of a 60 GHz SoC. Moreover, the target transmission speeds and modulations for 60 GHz applications result in demanding speed and complexity requirements for the digital baseband processors; hence, these SoCs will benefit from the use of a CMOS node with the smallest feature size possible.

This work investigates the operation of front-end 60 GHz transmitter building blocks, namely power amplifier (PA) and up-conversion mixer, in a contemporary 65nm bulk CMOS process. Fig. 1 depicts a potential superheterodyne transmitter architecture, which is used as a reference point for this RF front-end design. The 60GHz band can be covered with an LO in the range of 50GHz and an IF in the range of 10 GHz.

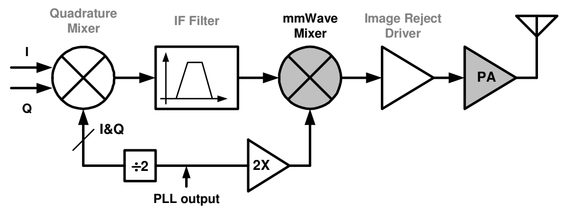


Fig. 1. Superheterodyne 60GHz transmitter architecture

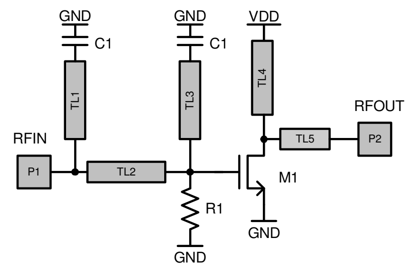


Fig. 2. Simplified circuit schematic of the 60 GHz PA

II. CIRCUIT DESIGN

A. Power Amplifier

A simplified circuit schematic for the CMOS PA is shown in Fig. 2. It is a single-stage, single-ended common source amplifier. This relatively simple configuration is chosen to investigate the large-signal compression characteristics of a 65nm nfet. A significant portion of the design effort was placed on the layout of the power device to optimize its performance while complying with electro-migration reliability requirements. The employed nfet has an equivalent width of 62um, and its DC bias current is 23mA, which results in a current density of 370uA/um. The supply voltage is 1.2V. All of the employed transmission lines (TLs) are microstrip.

The input matching network takes into account the capacitance of the input RF pad (P1), and employs TLs TL1-3. TL1 and TL3 are connected to AC ground through bypass capacitors C1. A 300Ω resistor (R1) is added next to the transistor gate to procure unconditional stability and wide-band match. In simulations, the addition of this component to the input network reduces the power gain by

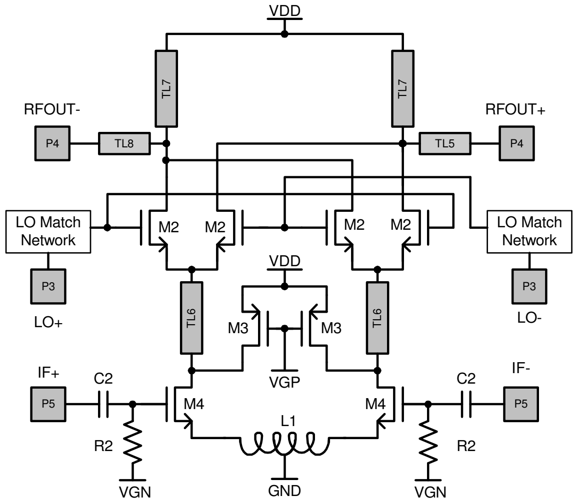
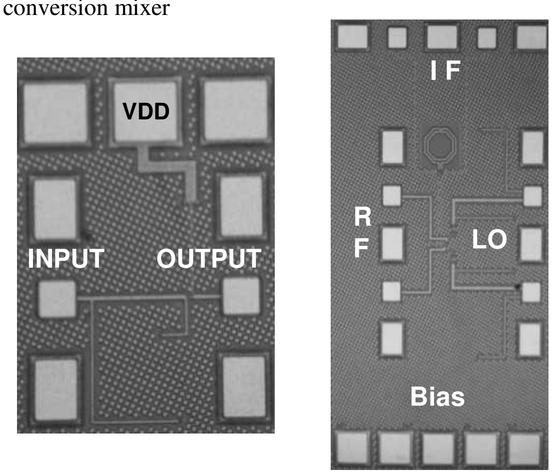


Fig. 3. Simplified circuit schematic of the 60 GHz active up-conversion mixer



(a) (b)

Fig. 4. Micrographs of the fabricated 65nm CMOS circuits. (a) Power amplifier, (b) Up-conversion mixer.

about 1dB but has no significant impact on the o1dBCP. The output network (TL4-5 and P2) is designed through schematic load-pull simulations.

B. Up-Conversion Mixer

The design of an up-conversion mixer for a superheterodyne 60 GHz transmitter faces multiple and significant challenges. Both, LO and RF ports operate in the mmWave range; as a result, the conversion gain (CG) is sensitive to the insertion loss and parasitic components of the interconnection elements. In addition, since power amplification in the transmitter front-end is expensive in terms of power consumption, the mixer's output 1dB compression point (o1dBCP) should be as high as possible.

Fig. 3 describes the up-conversion mixer. It is a fully differential, double-balanced Gilbert cell. IF, LO and RF center frequencies of 10 GHz, 50 GHz and 60 GHz, respectively, are considered for the design. The supply voltage is 1.2V and the total DC bias current is 24mA. The IF input transconductor is an inductively degenerated nmos differential pair. A differential inductor (L1) is chosen instead of two separate inductors to provide common-mode rejection. The inductance value is chosen to provide a wideband IF input match. The use of current steering is proposed for this mmWave mixer to improve its CG and linearity at the expense of additional power. The nominal current provided to the input transconductor through pmos transistors M3 is 12mA. The connection between the input stage and the switching transistors (M2) is modeled as TL6. Stubs TL7 tune the output port of the mixer for maximum gain at 60 GHz.

The LO matching network (not shown for simplicity) is composed of additional transmission lines and short stubs. At the LO port (RF pads P3), a differential impedance of a value close to 100Ω is seen in a frequency range of approximately 45-65GHz. 50Ω resistors are connected from AC ground to the gate of each pair of switching transistors M2 to provide a resistive termination. This value of resistance was chosen so that the LO voltage swing that corresponds to a given conversion gain could be known through measurements. Note that a higher resistance value can be employed to increase the effective LO voltage swing (and hence the CG) for a given input power into the LO port.

III. MEASUREMENT RESULTS

The described circuits were fabricated in a 65nm bulk CMOS process. Fig. 4 shows the chip micrographs. The size of both designs is limited by the pad frame and the necessary space between them to accommodate the RF probes. The PA and mixer use an area of 450umX600um and 0.7mmX1.4mm, respectively. All of the measurements are performed on-wafer.

The nfet employed for the PA is characterized as a stand-alone device including the parasitics introduced by all of the metal layers required for its connection to the top-metal TLs. From s-parameter measurements, the calculated cut-off frequency (f_T) is 230 GHz.

A. Power Amplifier

Fig. 5 shows the measured s-parameters of the PA. In a bandwidth of more than 10 GHz (55-65 GHz) the PA attains a power gain higher than 4dB and input match better than -10dB. Good output match and reverse isolation are also obtained.

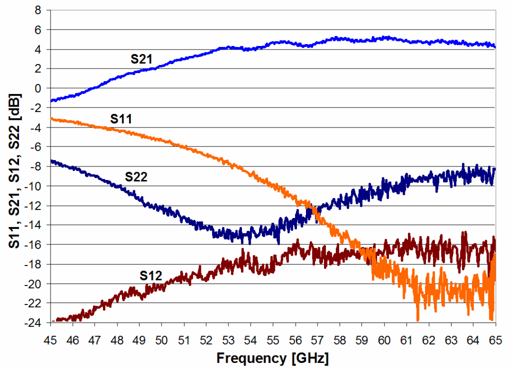


Fig. 5. Measured s-parameters of the PA

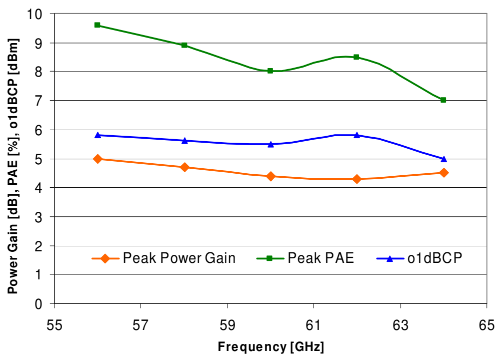


Fig. 6. Measured large-signal frequency response of the PA

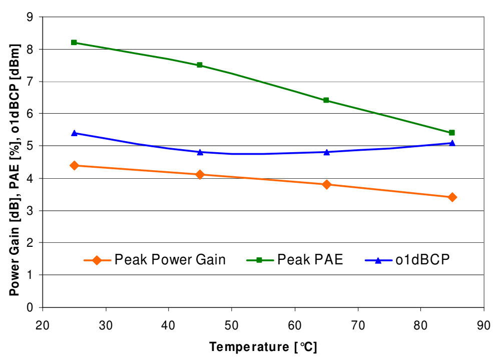


Fig. 7. Measured temperature response of the PA at 60 GHz

Swept power gain, compression and efficiency measurements are also performed. The available input power from the source is calibrated with a through measurement on a low-loss GSG substrate, and the frequency dependent loss from the probe tip to the spectrum analyzer is calibrated using a second-tier short-open-load (SOL) adapter technique. The overall calibration procedure has an estimated accuracy of 0.5dB for both input and output power levels, and is performed at each power level and frequency to remove any non-linear and/or frequency dependent effect of the test equipment. Fig. 6 shows the large signal behavior of the PA from 56 to 64 GHz. In this frequency range, the measured o1dBCP changes by less than 1dB, and the saturated output power

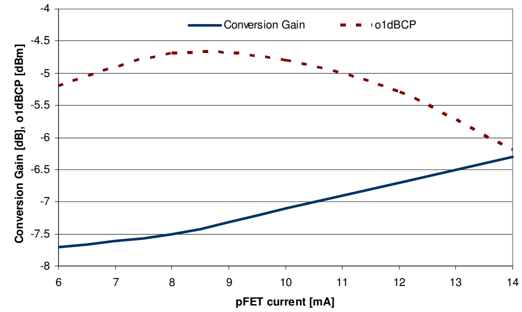


Fig. 8. Measured 60GHz conversion gain and o1dBCP as a function of current through pmos transistors M3

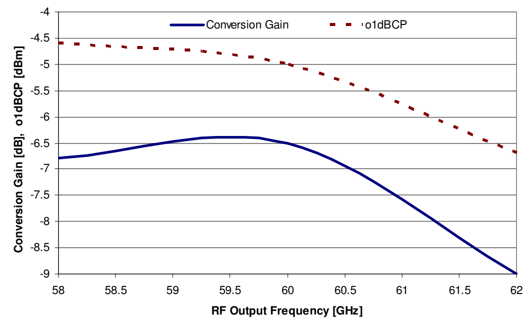


Fig. 9. Measured conversion gain and o1dBCP as a function of RF output frequency for IF=10GHz, LO=48-52GHz

changes from 10.5 to 9 dBm, showing that the PA has a large-signal wideband behavior. Fig. 7 shows the result of large signal measurements over temperature. A constant current density was kept for all temperatures.

B. Up-Conversion Mixer

For the mixer characterization, the differential LO signal is applied trough an external waveguide balun and the output is observed with a spectrum analyzer that uses an external harmonic mixer for measurements. The measured LO input return loss is better than -11dB from 45 GHz to 65 GHz and the LO-RF isolation at 50 GHz is 30 dB. Measurements at an RF output of 60GHz are performed with LO and IF frequencies of 10 GHz and 50 GHz respectively. Fig. 8 shows the performance of the mixer as a function of the bias current applied through the pmos transistors M3, while keeping the total bias current constant at 24mA. Under nominal bias conditions (pmos current=12mA), the mixer's performance is relatively constant over temperature up to 65°C. At 85°C, the measured 60GHz CG and o1dBCP are -7.5dB and -6.5dBm respectively. Figure 9 presents the frequency response of the mixer. All of the previously mentioned measurements are performed at an LO power of 5dBm. With LO power of 3dBm, the measured 60GHz CG and o1dBCP are -7.5dB and -6.5dBm respectively.

TABLE I
STATE OF THE ART IN CMOS MILLIMETER-WAVE POWER AMPLIFIERS

Ref.	Topology	DC Biasing	Frequency [GHz]	Power Gain [dB]	o1dBCP [dBm]	Sat. Power [dBm]	PAE [%]	CMOS Node
This work	1-stage, CS, SE	23mA, 1.2V	62	4.5	6	9	8.5	65nm
[5]	3-stage, CS, SE	26.5mA, 1.5V	60	4.7	6.4	9.3	7.4	90nm
[6]	2-stage, CS, SE	23mW	57	9.8	6.7	-	20	90nm
[7]	2-stage CC, 1-stage CS, SE	45mW, 1.5V	60	14	1.6	6	5.2	90nm

TABLE II
STATE OF THE ART IN CMOS MILLIMETER-WAVE UP-CONVERSION MIXERS

Ref.	Topology	Power [mW]	Frequency [GHz] RF	Frequency [GHz] IF	LO Power [dBm]	Conversion Gain [dB]	o1dBCP [dBm]	LO-RF Isolation [dB]	CMOS Node
This work	DF, DB, Gilbert w/ current steering	29	60	10	5	-6.5	-5.0	30	65nm
[8]	DF, DB Gilbert w/ LO buffer	70	60	1-5	-	-4 to -7	-	-	90nm
[9]	SB, Resistive, w/ Balun	0	60	2	9	-13.5	-19	34	65nm
[10]	DF, DB, Gilbert w/ LO & RF baluns	13.2	51	11	0	-11	-12	26.5	90nm

CS = common source, CC = cascode, DF = differential, SE = single-ended, DB = double-balanced, SB = single balanced

VII. SUMMARY AND CONCLUSIONS

To the best of the author's knowledge, this work has reported 60 GHz PA and active up-conversion mixer for the first time in 65nm CMOS. Table I summarizes the results of the reported 60 GHz CMOS PAs. The gain of this 65nm single-stage PA is comparable to the gain-per-stage of the PAs in [6, 7], and the o1dBCP is comparable to the one reported in [5] with 1.5V supply and the one reported in [6] at 57GHz. This PA has probably the widest operating bandwidth (S21 and o1dBCP vary within 1dB over 10GHz); previous works [6-8] have not reported o1dBCP and PAE over frequency. Table II summarizes the results from the published CMOS up-conversion mixers operating beyond 30GHz. This design achieves the highest o1dBCP. Its overall performance is also very competitive with respect to mmWave mixers reported in SiGe and III-V technologies [11], and to CMOS mixers operating at 20-30 GHz [12-13]. Both, PA and up-mixer, maintain a good performance over temperature. These results and those from others in 65nm [4, 8, 14], suggest the feasibility of 60 GHz wireless SoCs integrating mmWave and complex, high-speed digital components.

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