A 1.7-dB Minimum NF, 22-32 GHz Low-Noise Feedback Amplifier with Multistage Noise Matching in 22-nm SOI-CMOS

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***Abstract* — A transformer-feedback low-noise amplifier (LNA) implemented in 22-nm SOI-CMOS with interstage noise matching is described. The LNA peak gain is 21.5dB at 22GHz, with a -3dB bandwidth (BW) of 19-36GHz. Minimum noise figure (NF) is 1.7dB centered at 28GHz, and remains below 2.2dB across 10GHz. Third-order input intercept (IIP_3) is -13.4dBm at peak gain when dissipating 17.3mW. Input and output return losses are >10dB across 22-32GHz (effective BW). Modulation of the FET backgate voltage increases NF by <0.5dB, while reducing power consumption to just 5.6mW.**

***Keywords* — Low-noise amplifier (LNA), lossless RF feedback, mm-wave transformer, broadband, FD-SOI CMOS.**

I. Introduction

Improvements in the bandwidth, noise figure, and power consumption of silicon integrated mm-wave receiver front-ends enables the development of advanced wireless communication systems. Low-noise amplifiers (LNAs) implemented in production bulk-CMOS technologies typically offer 3GHz bandwidth, 3dB minimum noise figure (NF), and an input intercept (IIP_3) between -15 and -20dBm in the 28GHz band [1]. The feedback LNA developed in this work benchmarks the performance of a 22-nm FD-SOI CMOS technology (GF-22FDX [2]) in the same band. We target sub-2dB NF, better than 10-dB input return loss across >10-GHz bandwidth, 20-dB peak gain, and power consumption well below 20mW, while maintaining linearity comparable to circuits implemented in bulk-CMOS.

The paper is organized as follows. Design of the input and output stages, and interstage interfacing of the proposed LNA are described in Section II. Modeling, implementation, and tuning of the interstage transformer for minimum noise figure are also detailed. Measurement results are presented in Section III, and concluding comments are drawn in Section IV.

II. LNA Design

A schematic of the proposed 2-stage LNA is shown in Fig. 1. The first stage consists of a common-source amplifier with source-gate feedback via transformer T_1. Both the input and optimum source impedances for minimum noise figure seen at the gate of M_1 are modified by negative feedback to realize impedance and noise matching simultaneously. Transformer T_2 interfaces the two stages, and it is designed to minimize the noise added by M_2. It also improves the gain by stepping-up the voltage between the first and second stages. The frequency response of the cascode second-stage is extended using inductive peaking ($L_{1\text{-}4}$). Resistor R_F biases

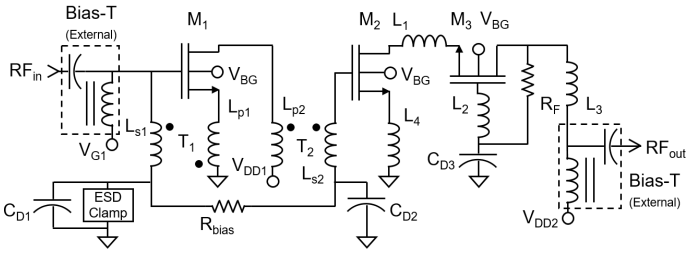


Fig. 1. Schematic of the 2-stage, wideband LNA prototype

M_3 and trims the LNA output impedance to match a 50-Ω load. The backgate voltage of the fully-depleted (FD-SOI) transistors (V_{BG} in Fig. 1) is used to adjust the LNA power consumption between low-power (LP) and low-noise (LN) modes of operation. On-chip metal-metal capacitors ($C_{D1\text{-}3}$) decouple key bias points, and a bidirectional ESD clamp at the cold side of T_1 protects the LNA input from electrostatic discharge. Bias-Ts facilitate characterization with a 2-port vector network analyzer (VNA).

A. Input Stage

Common-source transistor M_1 is biased at the optimum bias current for minimum noise figure (i.e., NF_{min1}). A unit-transistor size of 1μm×20nm is selected to reduce noise contributed by its extrinsic gate resistance. M_1 is comprised of 80 gate fingers in total, and the real part of its optimum source resistance for minimum noise figure ($R_{n,opt}$) is 50Ω. With V_{G1} and V_{BG} set to 0.25V and 2V, respectively, M_1 operates at 0.15μA/μm of gate width, and I_{DS1} is 12mA. V_{G1} is fed to the gate via an external bias-T for testing due to the limited number of testpads available.

Negative feedback makes the LNA input impedance dependent on transconductance gm_1 of M_1 and the transformer turns ratio n/k [3]. The first-stage bandwidth (BW) is determined by the coupling factor k_1 of T_1 [4]. Planar windings, consisting of a 1-turn primary and a 2-turn secondary coil, are implemented in second-metal copper (3-μm wide, 3.3-μm thick). The gap between turns is uniform at 2μm. The resulting transformer k_1 is 0.55 and it occupies 66×66μm^2 of chip area. Primary (L_{p1}) and secondary (L_{s1}) self-inductances are 90pH and 250pH, respectively, giving an electrical turns ratio n/k = 3. Reduced metal fill minimizes parasitic capacitance and extends the transformer's high-frequency response. The shunt parasitic capacitance of the RF input pad resonates with L_{s1} to reduce insertion loss.

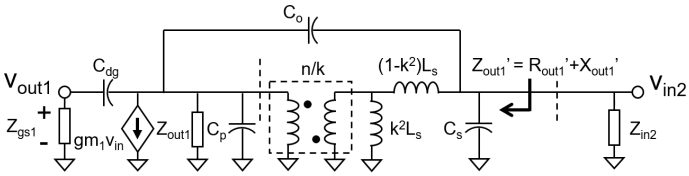


Fig. 2. Interstage coupling transformer model with leakage shifted to the secondary (Z_{out1}=R_{out1}+jX_{out1})

The transformer secondary winding is also a low-impedance path to ground for static discharge (ESD) events. Large-signal simulations for the human-body model (HBM) predict that input voltages ranging from -3kV to +600V can be safely handled at the LNA input.

The first stage consumes 5mW from a 0.42-V supply (V_{DD1}). Backgate voltage V_{BG} may be adjusted to trade-off gain and NF for lower power consumption in the first stage.

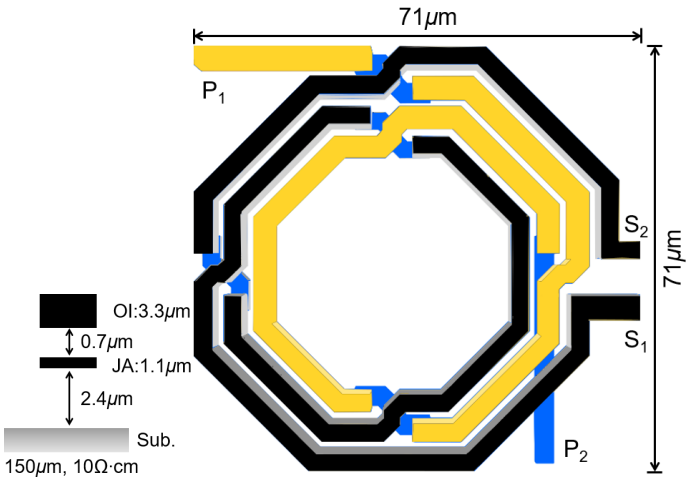
B. *Interstage Noise Matching*

The LNA developed in this work utilizes interstage transformer coupling to set the second-stage noise factor F_2 equal to F_{min2} (i.e., noise matching). In this way, SNR degradation by the second stage is minimized. Other LNA designs have maximized power gain by impedance matching stages, e.g., [5]-[7].

Consider the lumped-element transformer model of Fig. 2. The turns ratio (n/k) of T_2 may be used to synthesize $Z_{n,opt2}$ at the second stage input to yield F_{min2} from transistor M_2. Assuming low insertion loss, the transformer also provides an opportunity for passive voltage gain between stages due to mismatch between the real part of the first stage's output impedance (R_{out1}), and the real part of the input impedance to the second stage (i.e., $R_{n,opt2}$), which is larger.

An additional inductor is needed to realize the reactance for noise matching (i.e., $X_{n,opt2}$), as FET drain reactance X_{out1} is capacitive, and the reactance required to realize F_{min2} is inductive. Leakage inductance $(1\text{-}k^2)L_s$, provides most of the inductance required to realize $X_{n,opt2}$. The impedance seen looking into the secondary output should be Z_{out1}'=$R_{n,opt2}$+$jX_{n,opt2}$ across the desired bandwidth, but there is a limitation imposed by the transformer's frequency response.

Fig. 3a shows the top-copper layers used to realize the interstage transformer, and the physical layout is shown in Fig. 3b. Similar to T_1, the 3-μm wide, 3.3-μm thick second-metal copper windings with 2-μm gap between turns realizes a compact layout (i.e., 71×71μm^2). The primary and secondary self-inductances are 170pH and 330pH, respectively, yielding an electrical turns ratio of 1:2.5 and a k-factor of 0.56. The inductance of the interconnect in the physical layout and the transformer leakage inductance create the reactance required to realize noise matching at the second stage input. The drain supply voltage of M_1 is fed via the transformer primary, and the parasitic interconnect inductance of the supply lines are absorbed in the transformer tuning. Shunt tuning capacitances across the primary (C_p) and secondary (C_s) are 127fF and 93fF,



(a) BEOL metals (b) Physical layout

Fig. 3. (a) BEOL Stack-11 top copper layers, (b) Physical layout of the interstage transformer (primary: P_1/P_2, secondary: S_1/S_2 are both in OI with JA underpass)

respectively. They are comprised of parasitic capacitances at the drain of M_1 and gate of M_2, together with shunt parasitics from the transformer. Capacitive tuning of the transformer's self-inductance synthesizes the desired impedance seen at the second stage input ($Z_{n,opt2}$).

C. *Output Stage*

Gate areas for M_2 and M_3 are chosen to realize the desired in-band gain (20dB) and NF (<2dB). Increasing the width of M_2 lowers $R_{n,opt2}$ and the turns ratio of the interstage transformer, which leads to lower voltage gain from the interstage mismatch. Simulations predict that gate area optimization for the second stage yields only minor performance gains for NF and gain. Therefore, uniform device sizes are used (80μm, 1μm×20nm/finger) to simplify the layout and performance verification for the 22-nm prototype. All transistors are biased for lowest noise factor. The gates of M_2 and M_1 are set to the same voltage (i.e., 0.25V) via isolation network R_{bias} and C_{D2}.

Inductors $L_{1\text{-}3}$ (165, 150, 270pH, respectively) peak the second-stage frequency response. Shunt feedback around M_3 forces the real part of the LNA output impedance to 50Ω when R_1 is 145Ω. The reactive portion is nulled between 24 and 32GHz by inductance L_3 and the output bondpad capacitance.

A 1.05-V supply for the output stage (V_{DD2}) maximizes headroom and linearity from the common-gate amplifier. Power consumption of this stage is 12mW. The bias-T at the output facilitates characterization with a 2-port network analyzer (VNA). A folded-cascode output using a PMOS device for M_3 is a potential alernative when interfacing the LNA to another stage on a chip. Power consumption and linearity trade-offs are also possible with a folded cascode, as the load impedance on-chip could be set larger than 50Ω.

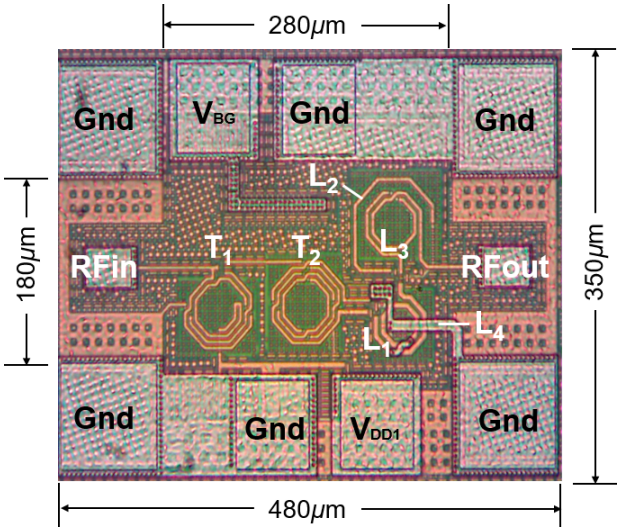


Fig. 4. Die micrograph of the LNA prototype

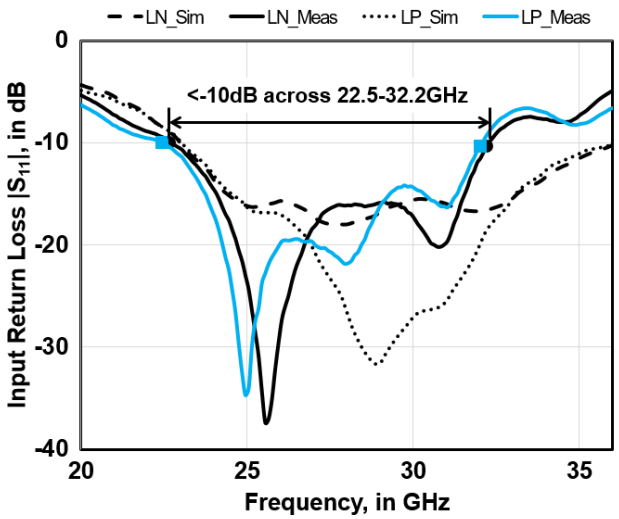


Fig. 6. Measured and simulated input return loss

D. Stability

Circuit stability must be considered in feedback amplifier design, especially at out-of-band frequencies where transistor gains may be relatively large. The secondary winding of T_1 is a low-impedance path to ground for frequencies below the passband. Therefore, the LNA does not require additional damping at the input to ensure stability (which may degrade gain and NF). The high-gain second stage is stabilized by source degeneration inductor L_4 (100pH). The μ-stability test predicts that the LNA is unconditionally stable, with $|\mu| > 1$ across the entire frequency range from simulations.

III. Measurement Results

A micrograph of the LNA prototype fabricated in Global Foundries 22FDX® process is shown in Fig. 4. The total and active chip areas are 0.17mm^2 and 0.05mm^2, respectively. The S-parameters, NF, and third-order intercept point (IP_3) of multiple LNA samples were measured on-wafer using a wideband VNA.

The backend of 22FDX (BEOL, Stack-11) is comprised of 10 interconnect metals and optimized for RF/mm-wave applications with 3 thick layers (2 copper, 1 aluminum) at the top of the stack. A quality factor of 17 is achieved for inductors $L_{1\text{-}4}$. Control of the FD-SOI transistor backgate enables trade-offs on the fly between RF performance (low-noise mode) and power consumption (low-power mode) for the LNA.

Fig. 5 shows measured and simulated small-signal forward ($|S_{21}|$) and reverse ($|S_{12}|$) gains. In low-noise mode (LN), V_{BG} is set to 2V and the peak gain is 21.5dB at 22GHz. The measured -3dB BW is 19 to 36.2GHz (i.e., 17.2GHz of BW), giving a gain-bandwidth product (GBW) of 174GHz. The DC power consumption in LN mode is 17.3mW. When V_{BG} is reduced to 0.62V (i.e., LP mode), the power consumption falls to 5.6mW. Gain decreases by 3.6dB to a peak of 17.9dB at 22.5GHz, and -3dB BW is 19.6 to 35.6GHz (GBW of 113GHz). Very good agreement between measurement and simulation is seen for both modes.

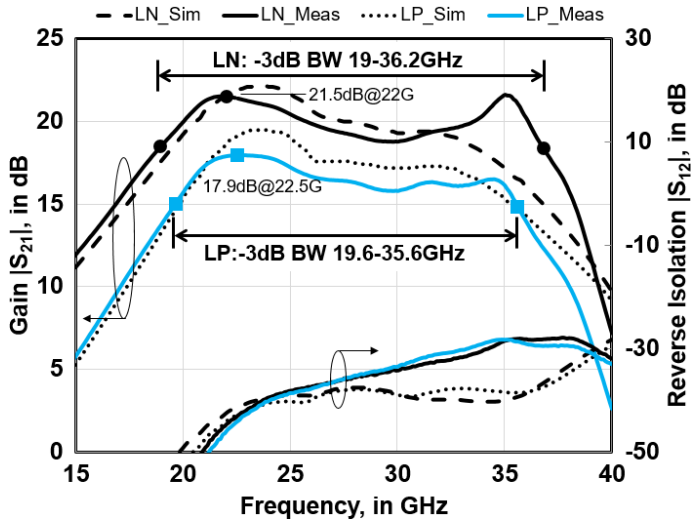


Fig. 5. Measured and simulated small-signal gain and reverse isolation

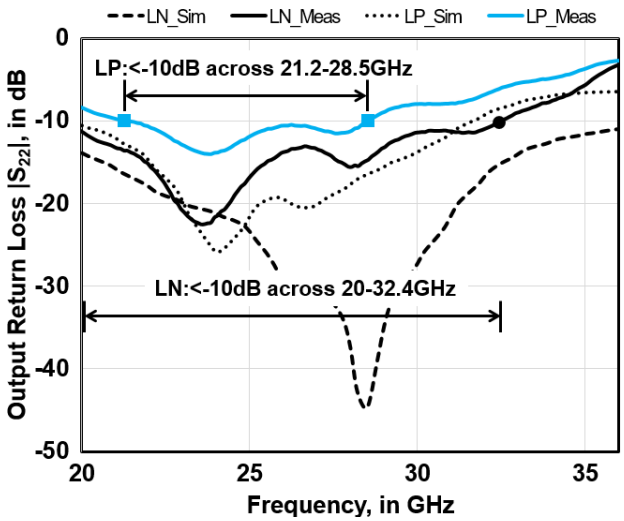


Fig. 7. Measured and simulated output return loss

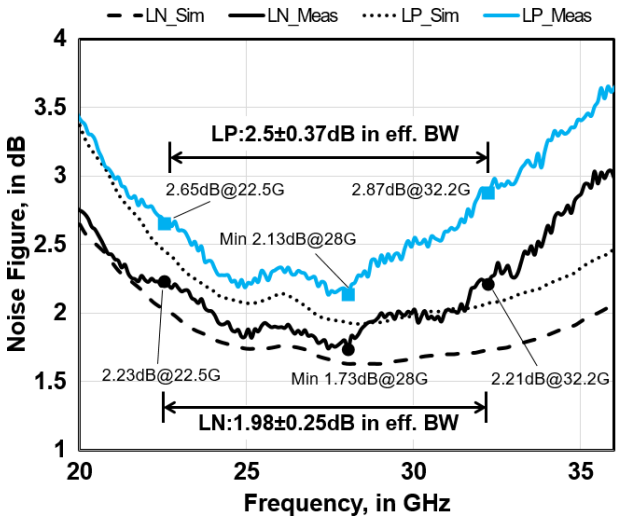


Fig. 8. Measured and simulated noise figure

Figs. 6 and 7 show measured and simulated input ($|S_{11}|$) and output ($|S_{22}|$) return losses, respectively. Again, simulation and measurement agree well. Input and output impedances are near 50Ω (i.e., >10dB return loss) from 22.5 to 32.2GHz in LN mode and 21.2 to 28.5GHz for LP mode. Note that $|S_{22}|$ varies between power modes, which is expected due to the change in transistor drain currents.

We define an effective bandwidth (BW_{eff}) for the LNA as the frequency range where $|S_{21}|$ gain is within -3dB of its peak and $|S_{11}|$ is below -10dB. The measured BW_{eff} is 9.7GHz (22.5 to 32.2GHz) in both LN and LP modes.

The 50-Ω noise figure (NF) is plotted in Fig. 8. The measured NF at 28GHz (passband center) in LN and LP modes is 1.73dB and 2.13dB, respectively. Within BW_{eff}, the NF in low-noise mode is 1.98±0.25dB, and increases by 0.5dB in LP mode. The discrepancy between simulation and measurement beyond 28GHz is likely due to two factors. Firstly, noise matching between stages is affected by interwinding parasitic capacitance of the transformer and transistor parasitics. Also, uncertainty in the measured NF increases with increasing frequency.

Two input tones near 22GHz (i.e., at peak gain) with a frequency separation of 500kHz are applied at the LNA input to determine the IP_3. Equal power levels of -35dBm (i.e., near small-signal) were used for the fundamental tones. The measured IP_3 referred to the input (IIP_3) is -13.4dBm and -14.4dBm in LN and LP modes, respectively. IIP_3 degrades as the bias current is decreased between modes, but only by 1dB.

Table 1 compares the performance of the LNA prototype in LN and LP modes with other LNAs operating in the 28-GHz band. In LN mode, the prototype realizes substantially lower NF while consuming less DC power and chip area than the other amplifiers listed. Variation in NF is also reduced to just 0.5dB across 10GHz bandwidth. Moreover, backgate modulation enables a 3x reduction in DC power consumption, while maintaining low NF and wide BW. The narrowband

Table 1. Wideband mm-Wave LNA Performance Comparison

	This work		GSMM	RFIC	MWCL
	LN	**LP**	2018 [5]	2018 [6]	2017 [7]
BW_{eff}* (GHz)	22-32 (10)	22-32 (10)	27-47.5 (20.5)	29-37 (8)	26-32.7 (7.7)
Gain (dB)	20.1±1.4	17±0.9	18.5±1.5	27±1.5	25.6±1.5
Peak Gain (dB)	21.5@ 22GHz	17.9@ 22GHz	20@ 28GHz	28.5@ 32GHz	27.1@ 27GHz
NF (dB)	1.7-2.2	2.1-2.9	4.2-5.5	3.1-4.1	3.3-4.3
IIP_3 (dBm)	-13.4@ 22GHz	-14.4@ 22GHz	-9.4@ 28GHz	-12.5@ 32GHz	-12.6@ 27GHz
P_{DC} (mW)	17.3	5.6	58	80	31.4
Act. Area (mm^2)	0.05	0.05	0.2	0.21	0.26
Process	22-SOI CMOS	22-SOI CMOS	45-SOI CMOS	0.25-μm SiGe	40-Bulk CMOS

*gain is within the -3dB BW for $|S_{21}|$ and $|S_{11}|$<-10dB

cascode amplifier in [8] reported a lower NF of 1.45±0.15dB across 24 to 28GHz. However, the single-stage design has ∼7dB less gain (13.4±0.6dB), and the input and output return losses do not exceed 10dB.

IV. Conclusions

A 22-nm FD-SOI CMOS technology developed for RF/mm-wave applications enables broader bandwidth, lower noise, and trimmable power consumption in a 2-stage LNA. The prototype achieves 21.5-dB peak gain, 1.7-dB minimum NF and 10-GHz BW when consuming 17mW. When power consumption is lowered to just 5.6mW, 18-dB gain, 2.1-dB minimum NF and 10-GHz BW are maintained.

Acknowledgments

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