23.4 A CMOS TV Tuner/Demodulator IC with Digital Image Rejection

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TV tuners covering the 48-860MHz frequency band have been implemented using passive RF tuning elements in shielded cans. One way to realize TV tuners without tuning elements is to use a dual-conversion approach that needs no RF tuning, but still requires external SAW filters for image rejection. In dual down-conversion zero-IF systems with no signal at DC, external filters are replaced using active low-pass filters [1]. A recent active integrated filter approach based on poly-phase I/Q filtering and double-quadrature down-conversion replaces RF tuning elements by selectable on-chip RF band-pass filters [2]. The poly-phase filtering approach is effective only for out-of-band image, and in-band image suppression still relies on I/Q path matching. The proposed CMOS TV tuner chip employs a dual-conversion low-IF architecture, and implements all tuner/demodulator functions such as channel filtering, in-band image rejection, and video/sound demodulation digitally. The complex video carrier is moved to 1.75MHz rather than to the standard TV IF of 36 or 44MHz. The complex image rejection uses an LMS-based noise cancellation block with one complex tap.

The TV tuner/demodulator IC, shown in Fig. 23.4.1, contains a low-noise programmable gain amplifier/attenuator, an up-conversion mixer, down-conversion I/Q mixers, I/Q complex anti-aliasing filters with programmable gain, two 11b ADCs, and a baseband processor. Two complex signals are made digitally after the I/Q down-conversion. I+jQ is a complex signal while I-jQ is a complex image. After complex channel filtering and image rejection, a complex PLL recovers a complex carrier from the I+jQ signal. The sound is demodulated using another PLL with 50 or 70μs de-emphasis in FM demodulation. After the sound trapping or sound filtering, two 11b thermometer-coded DACs reconstruct video and sound outputs. The DAC outputs are low-pass filtered, and the composite video baseband signal (CVBS) output is buffered with a 75Ω line driver. The system needs two frequency synthesizers for LO1 and LO2. To cover a frequency range wider than 4 octaves, three VCOs are switched for LO1. The PLL1 for LO1 is an integer-N synthesizer while the PLL2 for LO2 is a fractional-N synthesizer. The PLL2 works at 2×LO2 so that the I/Q at LO2 can be obtained using a divide-by-2 stage. The only external components are a 27MHz crystal and loop filter capacitors. All VCOs and integrated filters are self-calibrated.

One key obstacle to the successful implementation of a low-IF TV tuner/demodulator is the image rejection. I/Q down-conversion systems, limited by I/Q path mismatch and phase error, achieve an image rejection (IR) of typically 30 to 40dB. Since I+jQ and I-jQ are vectors rotating in the opposite directions, the I-jQ image component leaked into the I+jQ signal can be correlated and cancelled as shown in Fig. 23.4.2. The correlation between I-jQ and the conjugate of I+jQ is weighted by μ, and integrated to detect the polarity of the image component leaked into the signal path. Similarly, the signal leaked into the image is detected by correlating I+jQ with the conjugate of I-jQ. A simple integrator is used as a low-pass filter. For the system to have IR>60dB, the I/Q ADCs should be 11b.

Another critical design issue is the high linearity in the variable gain amplifier and the mixers because the tuner should be able to receive about 130 TV channels. The variable gain stages are shown in Figs. 23.4.3 and 23.4.4. They cover a gain/attenuation range from –15dB to 25dB with a 0.85dB step. To maintain flat gain within the wide bandwidth, a series inductor is used to raise the gain at high frequencies. The NF at 25dB gain and the IIP3 at 0dB gain are designed to be 6.7dB and 15dBm, respectively. For digital gain setting, the output current and the source/load resistors are switched. To achieve high linearity, the 2-stage variable gain amplifier works either as an amplifier or as an attenuator to keep the signal level at the first mixer input below $3mV_{rms}$. It works with a single-ended input, but a difference amplifier is used to make internal signals differential. Two mixers are Gilbert-type with large V_{gs} for the input transistors, and the first mixer is loaded with a differential inductor, that is tuned to the first IF of 1.01GHz to suppress harmonic mixing. All analog filters use RC integrators for high linearity, and capacitors are self-calibrated using a master/slave tuning method. In the video/sound channel filtering, the group delay should be controlled tightly within ±75ns so that the step response can be over-damped without ringing, and nulls should be placed on the video, color, and sound carriers of all adjacent channels. This challenging task is performed digitally so that all three different standards of NTSC, PAL, and SECAM can be received using programmable filters and demodulators. The group delays of the 20^{th}-order channel-select filter and the sound-trap filter are equalized to be less than ±3 sample delays.

The prototype chip, fabricated in a 0.25μm CMOS technology, occupies $6\times6mm^2$, and consumes 1W from a 2.5V supply including a 75Ω video buffer driver. The analog portion of the chip consumes about 750mW. Measured system noise figures are 14 and 24dB at 25 and 0dB gains, respectively, and measured system IIP3 is –5dBm at 0dB gain. An image rejection of about 60dB is measured as shown in Fig. 23.4.5. A 10dB stronger image channel is used in this image rejection testing. The spectrum measurement shows the demodulated video signal. The luminance carrier is at DC, and the demodulated color carrier is about 3.58MHz. The image shown in the spectrum is the luminance carrier of the adjacent channel at –4.25MHz leaked into the signal band since the IF is 1.75MHz. Therefore, the folded image is at 4.25-1.75=2.5MHz. The integrated phase noises of the two synthesizers LO1 and LO2 are 0.66° and 0.95° as shown in Fig. 23.4.6(a). MOS caps are used for VCO tuning and control, and the VCO gain is set to below 50MHz/V. The PLL1 and PLL2 use 5.4MHz and 27MHz references with 300kHz and 100kHz loop bandwidths, respectively. The PLL1 covers a frequency range from 1.064GHz to 1.87GHz with a coarse 5.4MHz step while the PLL2 is fixed at about 2.02GHz with a fine 100kHz step. After divide-by-2, the LO2 step is 50kHz. The anti-aliasing filter before the ADC is a 10^{th}-order complex low-pass filter with a cut-off frequency of 10MHz as shown in Fig. 23.4.6(b). The filter has a fixed 8dB gain, and the following AGC has a 20dB more gain with a 1dB step so that the ADC can have a $2V_{pp}$ input. Two pipelined ADCs sampling I/Q branches at 27MHz exhibit both INL and DNL less than 1LSB, SFDR of 69dB, and SNR of 60dB. The die micrograph is shown in Fig. 23.4.7.

References:

[1] M. Dawkins, A. Burdett, and N. Cowley, "A Single-Chip Tuner for DVB-T," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1307-1317, Aug., 2003.
[2] J. van Sinderen, F. Seneschal, E. Stikvoort, F. Mounaim, M. Notten, H. Brekelmans, O. Crand, F. Singh, M. Bernard, V. Fillatre, and A. Tombeur, "A 48-860MHz Digital Cable Tuner IC with Integrated RF and IF Selectivity," *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb., 2003.

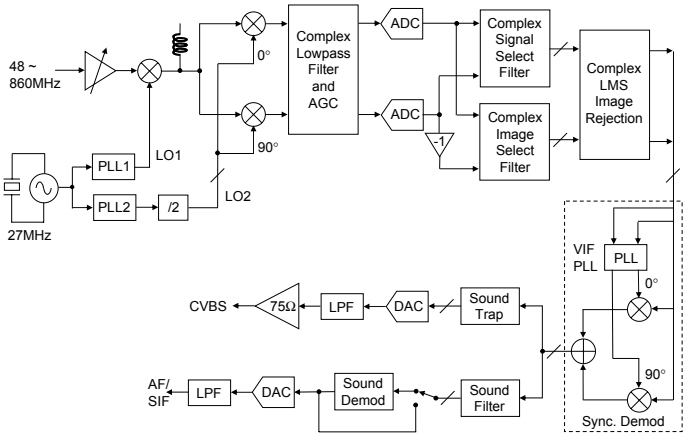


Figure 23.4.1: TV tuner/demodulator system.

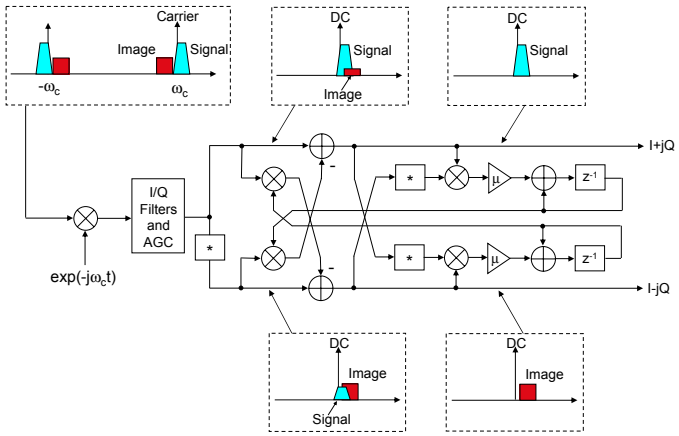


Figure 23.4.2: LMS-based complex image rejection concept.

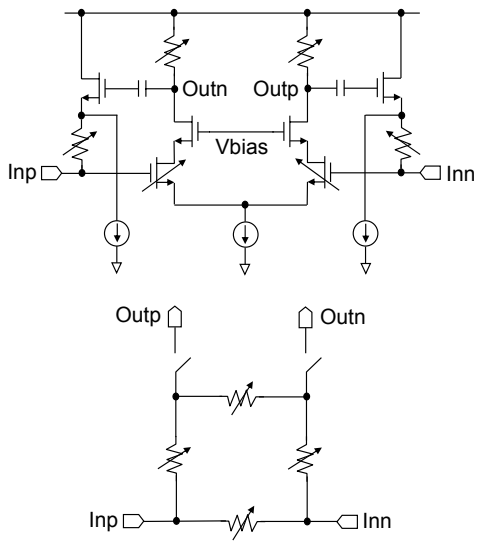


Figure 23.4.3: Low-noise variable gain amplifier/attenuator.

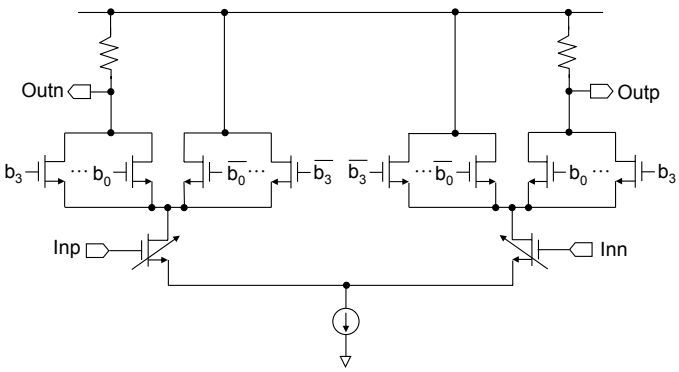
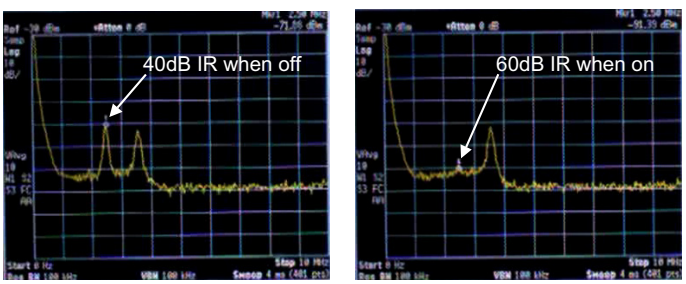
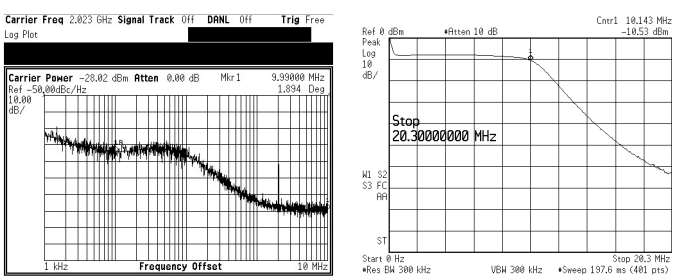


Figure 23.4.4: Wideband variable gain amplifier.



(a) (b)

Figure 23.4.5: Image rejection with LMS loop off (a) and on (b).



(a) (b)

Figure 23.4.6: (a) Phase noise of 2×LO2, and (b) complex anti-aliasing filter response.

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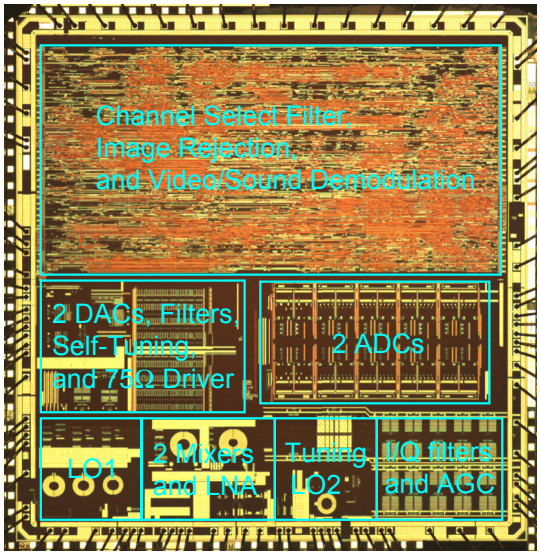

Figure 23.4.7: Die micrograph.

