A Methodology for Statistical Estimation of Read Access Yield in SRAMs

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ABSTRACT

The increase of process variations in advanced CMOS technologies is considered one of the biggest challenges for SRAM designers. This is aggravated by the strong demand for lower cost and power consumption, higher performance and density which complicates SRAM design process. In this paper, we present a methodology for statistical simulation of SRAM read access yield, which is tightly related to SRAM performance and power consumption. The proposed flow enables early SRAM yield predication and performance/power optimization in the design time, which is important for SRAM in nanometer technologies. The methodology is verified using measured silicon yield data from a 1Mb memory fabricated in an industrial 45nm technology.

Categories and Subject Descriptors

B.3.1 [**Semiconductor Memories**]: Static memory; B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Performance, Design, Reliability

Keywords

SRAM, memory, yield, worst-case, statistical modeling, access failure, variability, random variations

1. INTRODUCTION

Random variations in nanometer ranges technologies are considered one of the largest design considerations [1, 2]. This is especially true for SRAM memories, due to the large variations in bitcell characteristics. Typically, SRAM bitcells have the smallest device sizes on a chip. Therefore, they show the largest sensitivity to different sources of variations - such as random dopant fluctuations (RDF), line-edge roughness (LER) and others [3, 4]. While variations in logic circuits have been shown to cause delay spread [5, 6] which reduces parametric yield, for SRAMs, process variations also cause the memory to functionally fail, which reduces the chip's functional yield. With lower supply voltages and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power.

There are different types of SRAM bitcell failures, such as static noise margin stability fails (cell may flip when accessed), write fails (bitcell cannot be written within the write window) and access fails (incorrect read operation) [7, 4, 8]. In this paper, we concentrate on estimating yield loss due to read access failures, as this type of failure has a strong impact on determining the performance and power consumption of the memory. However, the methodology can be extended to account for other types of memory failures. Therefore, in this work, we use the word yield to refer to read (access) yield.

The statistical nature of SRAM failures requires statistical simulation techniques in order to account for these failure mechanisms early in the design cycle. However, due to the large size of SRAM memories, it is very difficult to run Monte Carlo simulations for the whole memory. Even if the computational resources allow Monte Carlo simulation for the whole memory, a large number of Monte Carlo runs is required. For example, more than 2×10^6 Monte Carlo runs are required to examine for one failure in a 2Mb memory, due to the rare event of having read current a weak bitcell exceeding 5σ of bitcell variations. Therefore, SRAM designers typically use worst-case approaches to insure high yield by designing for the worst-case bitcell for a given memory density [4]. However, this worst-case design technique negatively impacts the performance as well as increases power consumption.

Recently, there have been few works in the area of SRAM design methodologies. In [4], the authors present a worst-case analysis to account for weak cells and presented guidelines for SRAM timing to achieve high yield. In [7, 8] the authors model access failures by statistically accounting for bitcell read current variation as well as for the impact of access transistor leakage [8]. These previous works have focused on determining memory yield for a given sense amplifier (SA) offset (i.e., estimating access yield for a fixed value

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of bitlines differential voltage), which implies that worst-case analysis is assumed for the SA offset, although statistical analysis is used for bitcell read current variations.

In this work, we generalize the access failures to "statistically" include the SA offset distribution. This is important for SRAM circuit designers as it reduces the pessimism of assuming worst-case SA offset and worst-case bitcell. In addition, for the first time, we include the impact of sensing window variation on yield, which can have a strong impact on memory performance. The proposed statistical yield estimation methodology for access failures accounts for bitcell read current variations, sense amplifier offset, and sensing window variations, as well as leakage from other bitcells on the same column. In particular, the proposed methodology helps answer the following questions for SRAM designers:

1. What is the maximum achieved performance (minimum sensing window) for a given yield requirement;
2. How much is the achievable improvement in yield if SA offset is improved by a certain amount (i.e., increasing SA area or changing SA topology);
3. How to compare the expected yield for memories having similar density but different architecture (i.e., yield for different memory options).

The methodology is verified using measured yield results for a 1Mb memory in 45nm technology.

2. SOURCES OF READ ACCESS FAILURES

The read path in SRAM memories is typically a part of the critical path, which determines the memory access time (performance). Fig. 1 shows read path in an SRAM memory, where read operation begins by selecting the column using the PMOS pass gate and activating the wordline (WL) of the selected row. Depending on the stored data in the bitcell, one side of the bitlines begins to discharge due to the read current (I_{read}) of the bitcell. Therefore, a small differential voltage is generated at the inputs of the voltage sense amplifier (V_{SAin}). To ensure correct read operation, the SA is enabled using a control signal (SAEN) after a sufficient differential signal V_{SAin} is developed, which is amplified by the SA to a digital output level.

The delay difference between the WL activated and the SA enabled is called "SA read (sensing) window" ($t_{wl2saen}$). $t_{wl2saen}$ has direct impact on the memory performance as it contributes a large percentage of the memory access time. In addition, $t_{wl2saen}$ has direct impact on the dynamic power consumption. As $t_{wl2saen}$ increases, the bitlines differential increases, which should be recovered by the precharge circuitry after each memory access cycle. In the mean time, increasing $t_{wl2saen}$ increases V_{SAin}, which reduces the probability of read failure due to SA input offset. Hence, it is always desirable to reduce $t_{wl2saen}$ as long as correct read operation is ensured. Therefore, there is a strong tradeoff between yield and performance/power for SRAM, which is one of the most important design decisions for memory designers. To our best knowledge, there are currently no statistical tools or methodologies to analyze this type of tradeoff in the design time. Therefore, SRAM designers typically rely on worst-case approaches.

Previous works [7, 8] define a successful read access as the probability of having the bitlines reach a **fixed** voltage

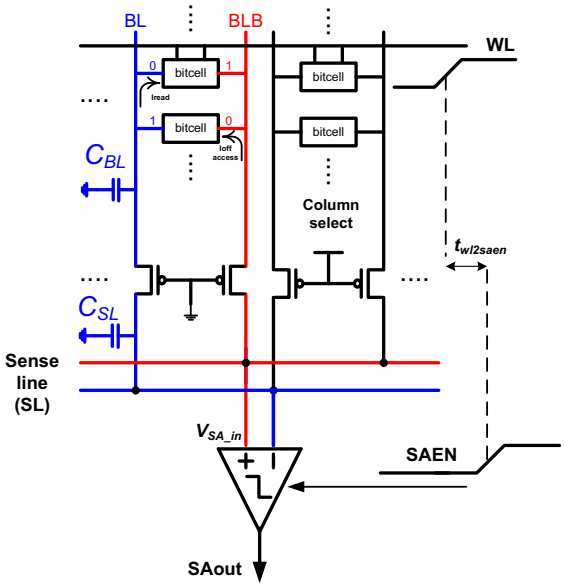

Figure 1: Simplified SRAM read path.

Δ_{min} for a **fixed** access (sensing) window $t_{wl2saen}$. In [7, 8], although statistical analysis is performed on I_{read}, however, by assuming fixed Δ_{min} and $t_{wl2saen}$, this means that worst-case is assumed for the sense amplifiers as well as for the sensing window. In addition, previous models assumed that BL discharge could be coupled directly to the SA inputs. However, in reality, due to the on resistance of PMOS column select device, the sense line is usually slower than the bitline discharge, and more time is required to achieve certain differential voltage [9]. Hence, the above mentioned techniques are more appropriate for bitcell technology optimization, while a new access failure estimation methodology is required for memory circuit design that can account for different sources of access failures in a single statistical yield estimation flow.

In the following sections, we go through the different sources that affect access failures. Following that, we present a new read failure definition that is used in the proposed flow.

2.1 Read Current and Sensing Slope Variations

Due to the small size of SRAM bitcell and the inverse relation between transistor variation and device area [10, 11], bitcell read current I_{read} shows large within die (WID) variations [3, 8], and typically follows a normal distribution. From a memory design point of view, I_{read} determines the time required to develop enough differential signal before enabling the SA. I_{read} variation is considered one of the largest sources of parametric yield loss in memories [8].

As mentioned earlier, sense lines discharge slower than bitlines. This is due to the ON resistance of the column select device (PMOS) shown in Fig. 1, which adds RC delay at the SA input [9]. Lets define the sense lines discharge slope as $K_{eff} = \Delta V_{SL}/\Delta t$. It can be shown that K_{eff} is proportional to I_{read} [9]. The statistical variation in I_{read} will also cause similar variation in K_{eff}, therefore, $\frac{\sigma}{\mu}|_{K_{eff}} = \frac{\sigma}{\mu}|_{I_{read}}$.

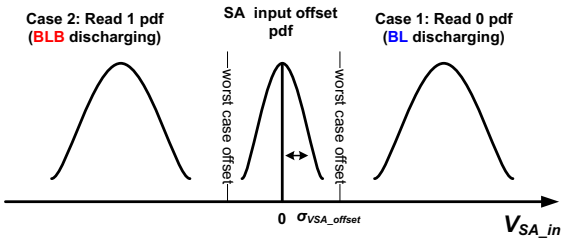

Figure 2: SA input offset and read 0/1 distributions.

2.2 Sense Amplifier Variations

Sense Amplifiers (SA) are typically used to amplify the small differential voltage on the bitlines (∼100mv) to a digital output level [4]. SAs are also sensitive to WID variations (mismatch) [12, 13], which cause SAs to show offset voltages that affect the accuracy of read operation. In addition, systematic variations due to asymmetric layout can increase the SA input offset. One way to reduce SA's input offset is increasing the size of input devices [10, 13]. Due to the strict limitations on area in memory design, the SA area-mismatch tradeoff is difficult because the SA should pitch-match the accessed bitcells. Therefore, the specification on SA offset is an important metric for memory designers.

Monte Carlo transient simulation is usually used to estimate the input offset distribution of SA [4]. Typically, the SA input offset can be modeled using a gaussian distribution with a mean of zero and standard deviation of $\sigma_{V_{SAoffset}}$ as shown in Fig. 2. In a worst-case design scenario, it is required to have the minimum sensing voltage V_{SAin} larger than the worst-case SA offset (as shown in Fig. 2). This is a pessimistic approach because the probability of having the slowest bitcell accessed using the SA suffering the largest offset is very small.

In this paper, we mainly focus on voltage sense amplifiers, however, the proposed methodology can be easily extended to current sense amplifiers as well.

2.3 Sensing Window Variations

As mentioned earlier, the read sensing window $t_{wl2saen}$ is an important parameter for correct read operation. In memory design, a centralized control block (timer circuit) is used to generate the timing for all the critical signals for memory operation - which include WL and SAEN signals [4]. To ensure good tracking with PVT variations, usually similar transistor sizes are used in the two logic paths [4]. However, due to random WID variations, the delay in these paths will show statistical variation [14, 5, 15]. Therefore, the sensing window will have spread around its mean value (as shown in Fig. 3).

Lets assume that the number of logic stages between internal CLK to WL and SAEN is m and n stages, respectively. For sake of simplicity, lets further assume that delay of each path can be modeled as a chain of inverters, with t_d being the delay of one stage. In an ideal scenario with no random WID variations, $t_{wl2saen}$ can be computed as $(n-m)t_d$. However, due to uncorrelated random variations, $t_{wl2saen}$ will have a statistical distribution, which is typically assumed gaussian [5, 15, 6]. Therefore, the mean and variance of $t_{wl2saen}$ can be computed as $\mu_{t_{wl2saen}} = (n-m)\mu_{t_d}$ and ${\sigma^2}_{t_{wl2saen}} = (n^2+m^2){\sigma^2}_{t_d}$, respectively, where ${\sigma^2}_{t_d}$ is

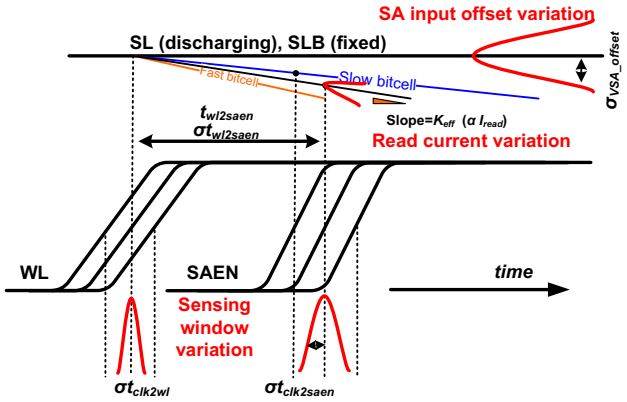

Figure 3: Main sources of variation affecting access failures.

the variance of one delay stage. In the case of memories, n and m are comparable, where $n-m$ determines the nominal $t_{wl2saen}$. However, there is a large spread in the sensing window since the spread in each logic path adds up to the $t_{wl2saen}$ variation (n^2+m^2 term). Note also that the spread $\sigma_{t_{wl2saen}}$ increases as n and m increase even if $n-m$ is constant (i.e, for a fixed $t_{wl2saen}$ delay). This implies that as the memory size increases and more logic stages are required in the CLK to WL and SAEN paths, this effect becomes more severe. This variation in sensing window can reduce the SA input voltage, which increases access failure probability - especially at low supply voltages (since $\frac{\sigma}{\mu}|_{t_{wl2saen}}$ increases due to reduced headroom [5]).

While a chain of inverters can be used to qualitatively explain the importance of accounting for read window variations, a more comprehensive delay variation analysis is required to account for different logic gates and fan outs in the CLK to WL and CLK to SAEN paths. In this paper, we use Monte Carlo simulation to determine $\mu_{t_{wl2saen}}$ and $\sigma_{t_{wl2saen}}$. Moreover, statistical timing analysis [6] can also be used for the same purpose.

2.4 Access Transistor Leakage

It is well known that bitcell access device leakage also reduces the SA input differential due to subthreshold leakage from the other side of the bitlines as shown in Fig. 1 [8]. The worst-case sensing occurs when all the unselected bitcells on the column store the opposite data for the selected bitcell. Access transistor leakage determines the upper limit of the number of bitcells per column. This effect is usually important in high performance memories due to the high leakage (low V_{th}) of the access device. In addition, due to the exponential dependence of subthreshold leakage on V_{th} variations, it is important to statistically calculate the total leakage on the bitline. Similar to [16, 8, 17], in this work, we account for leakage variation by calculating the total subthreshold leakage of bitcells associated with the bitlines using $N \times \mu_{I_{subth}}$ and subtract it from the bitcell's I_{read}, where $\mu_{I_{subth}}$ is the mean of the lognormal pdf of access transistor subthreshold leakage, and N is the number of bitcells per column.

Another source that can increase read access failures is dynamic noise coupling at the SA inputs. Due to the small differential signal developed on the sense lines, an aggressor

located near the SA may couple large noise at the SA input which can affect the accuracy of the read data. This situation is exacerbated if a weak bitcell is selected, the read sensing window is reduced, or if the noise occurs just before the SA is enabled. However, modeling of this dynamic noise component is very complex, as it strongly depends on the layout of the SA and sense lines, as well as the timing of the aggressors relative to the SA enable signal (SAEN). Nevertheless, by using layout noise shielding techniques and highly symmetric SA layout styles, the impact of this component can be minimized.

3. YIELD ESTIMATION

Fig. 3 shows a simplified timing diagram for an accessed bitcell including critical signals such as WL, SAEN and sense lines (SL). Also shown in the figure are the statistical variations on different components that affect the probability of access failure, which were described in the previous section (Section 2). When the WL is enabled, SL begins discharging, and the slope of SL discharge varies statistically depending on I_{read} variations as well as leakage from other bitcells (Section 2.4).

For the SA, the offset voltage distribution is superimposed on the V_{DD} (precharge level). As explained in Section 2.2, SA offset distribution is centered around zero (typically small asymmetry), as shown in Fig. 2, which means that some SAs will show positive or negative offsets. Note that positive offset will increase the failure probability of reading a 0 and reduce the failure probability of reading a 1, and vice versa. Therefore, in order to account for SA offset statistically in yield estimation, both read 0 and read 1 cases need to be addressed.

In addition to I_{read} and SA offset variations, $t_{wl2saen}$ variation can affect access failure probability, as described in Section 2.3. As shown in Fig. 3, if $t_{wl2saen}$ reduces due to statistical variations, V_{SAin} decreases, and hence the probability of access failure increases.

In order to estimate SRAM yield, it is important to statistically account for all the above mentioned sources in the same flow. Therefore, we define access failure for a certain bitcell as follows: For read 0 case, the probability of access failure is the probability of having SA input voltage V_{SAin} less than SA input offset $V_{SAoffset}$ **of that particular SA**. Note that in this case we are not assuming a fixed value of SA offset as in [7, 8]. Instead, the SA offset follows the normal distribution that can be determined from Monte Carlo simulations. Moreover, V_{SAin} needs to be computed statistically since it is a function of the statistical distribution on bitcell I_{read} and $t_{wl2saen}$ distribution.

In this case, the probability of access failure for bitcell $P_{AF,cell}$ in case of reading a 0 can be expressed mathematically as follows[1]:

$$P_{AF,cell,read0} = P(\mathbf{V_{SAin}} - \mathbf{V_{SAoffset}} < 0) \quad (1)$$

$$= P(\mathbf{K_{eff0}}\mathbf{t_{wl2saen}} - \mathbf{V_{SAoffset}} < 0) \quad (2)$$

Similar expression can be applied for the read 1 access failure.

Based on the proposed access failure definition, the flow for read access yield computation is as follows:

1. From the memory architecture (number of columns, muxing), calculate the number of SAs (N_{SA}) in a bank. Also, N_{SA} is the number of blocks in a bank, where a block is defined as the SA and associated bitcells accessed by that SA;
2. Generate N_{SA} samples of SA input offset distribution following $\mathcal{N} \backsim (\mu_{V_{SAoffset}}, {\sigma^2}_{V_{SAoffset}})$;
3. From the memory density and bank information, calculate the number of bitcells per bank ($N_{bit-bank}$);
4. Generate $2N_{bit-bank}$ samples of K_{eff} normal distribution with $\mu_{K_{eff}}$ mean and standard deviation of $\sigma_{K_{eff}} = \mu_{K_{eff}} \frac{\sigma}{\mu}|_{I_{read}}$ to represent the read 0 and read 1 sensing slope distributions ($\mathbf{K_{eff0}}$, $\mathbf{K_{eff1}}$);
5. Generate one sample of $t_{wl2saen}$ following the distribution $\mathcal{N} \backsim (\mu_{t_{wl2saen}}, {\sigma^2}_{t_{wl2saen}})$;[2]
6. Failure calculation step: For each SAs offset sample created in step 2, loop on all the bitcells that are accessed using this particular SA. Check the following conditions for each bitcell;
   - Read 0 fail: $\mathbf{K_{eff0}}\,\mathbf{t_{wl2saen}} - \mathbf{V_{SAoffset}} < 0$
   - Read 1 fail: $\mathbf{K_{eff1}}\,\mathbf{t_{wl2saen}} - \mathbf{V_{SAoffset}} > 0$
   - Count the number of read failures.
7. Repeat all the above steps for different banks;
8. Repeat all the above steps for large number of dies;
9. Calculate the yield based on the number of dies that can correctly be accessed for read 0 and 1 cases.

While the above steps focused on WID variation, the proposed methodology can be easily extended to account for die-to-die (D2D) variations. This can be done by including the statistical distributions of D2D variations and including different D2D samples for each run at the chip level (i.e., in step 8 shown above).

4. EXPERIMENTAL RESULTS

The proposed yield estimation methodology was verified using a 1Mb SRAM design fabricated in an industrial 45nm CMOS technology. Prior to running the proposed yield estimation flow, a characterization step is required to compute the above mentioned distributions (i.e., I_{read}, $V_{SAoffset}$, $t_{wls2saen}$). However, this characterization step is not computationally expensive due to the reduced number of circuit elements for these simulation setups. In addition, I_{read} and $V_{SAoffset}$ Monte Carlo simulations are an integral part of any SRAM design, and therefore, will not add to characterization time.

Characterization for the different components of yield failures was performed as shown in Fig. 4 for different PVT conditions. I_{read} was characterized using DC Monte Carlo Spice simulations to estimate the mean and standard deviation. In addition, the same analysis was also used to estimate the access transistor leakage. Fig. 5 shows how $\sigma/\mu|_{I_{read}}$ changes for different voltage and temperature conditions. This is an

[1] **Bold** symbol is used to indicate a random variable.

[2] Here we assume that a bank contains one control block which generates WL and SAEN signals. Nevertheless, different types of banking styles can be easily included in the flow.

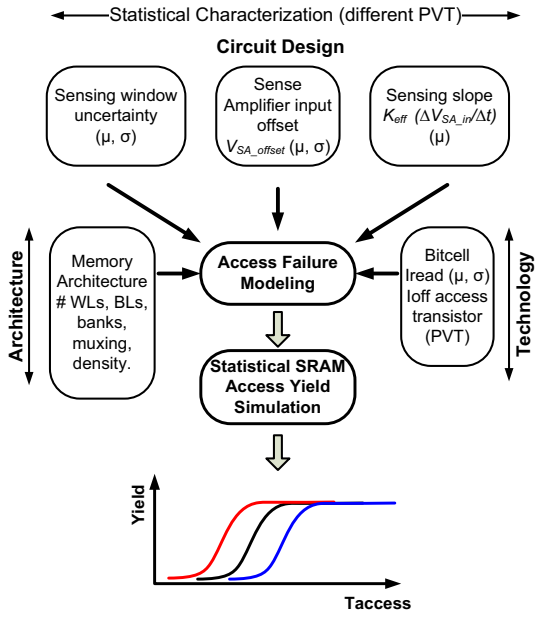

Figure 4: Yield estimation flow.

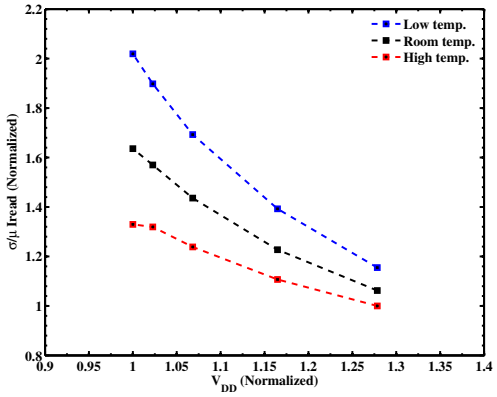

Figure 5: Characterization for bitcell I_{read} variation using DC Monte Carlo Analysis.

important part of the characterization as I_{read} mean and variances changes strongly across PVT conditions.

The sensing slope, K_{eff} for nominal conditions, was extracted by running transient Spice simulation on the critical path of the memory. Note that Monte Carlo simulation is not required in this case since we use I_{read} variations calculated from the first step to estimate K_{eff} variations as explained in Section 2.1. Also the same scaling rule is used to predict K_{eff} for other PVT conditions. SA offset distribution was simulated using Monte Carlo transient simulation as shown in Fig. 6, which shows the simulated/modeled cumulative distribution functions (CDF) for the SA input offset (normal distribution). Sensing window variation $t_{wl2saen}$ distribution was estimated using Monte Carlo transient simulation as well. After generating the characterization data, statistical yield simulation described in Section 3 was implemented using Matlab.

Fig. 7 shows the measured yield from the 1Mb memory

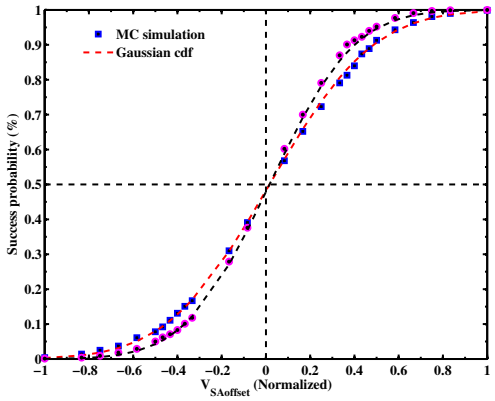

Figure 6: Characterization for SA offset using transient Monte Carlo Analysis for different PVT.

compared to the simulation for different supply voltage conditions. Good agreement between silicon and simulation results validate the accuracy of the proposed methodology. For these simulation results, 1000 chips of the 1Mb memory were simulated using the proposed flow. All bitcells were tested for read 0 and read 1 fails. Yield estimation for the proposed methodology takes less than 30 minutes to generate the results shown in Fig. 7 using a 3GHz PC with 1.5GB of memory which shows the efficiency of the proposed flow. The simulation results in Fig. 7 can be used explore the critical tradeoff between performance and yield requirement.

It is useful to compare the difference between using the proposed statistical yield estimation flow versus the worst-case analysis. This is shown in Fig. 8 where in the worst-case approach, the worst bitcell is assumed to occur with the SA having the largest offset and the smallest sensing window. Also shown is the statistical design approach to meet a yield of 99.7%. The statistical design enables reducing $t_{wls2saen}$ by 26% which translates to higher memory performance. This translates to 18% faster access time when assuming $t_{wls2saen}$ is 30% of access time, . In the mean time, the memory read power consumption also reduces because of reduced differential voltage on the bitlines.

It is important to note that the performance benefit of using statistical methodology versus worst-case approaches is a function of the memory density. It is expected that the difference between the two approaches increase with scaling due to the continuous increase in process variations as well as the higher SRAM density requirements. This shows the importance of statistically accounting for different components of read failures as proposed in this work, so that pessimism in worst-case approaches can be recovered in the design time.

5. CONCLUSIONS

The large increase in statistical variations in nanometer technologies is presenting huge challenges for SRAM designers. In this paper, a methodology for statistical estimation of access yield is proposed. The proposed flow accounts for the impact of bitcell read current variation, sense amplifier offset distribution, timing window variation and leakage variation on read failure. The methodology overcomes the pessimism inherited in worst-case design techniques that are

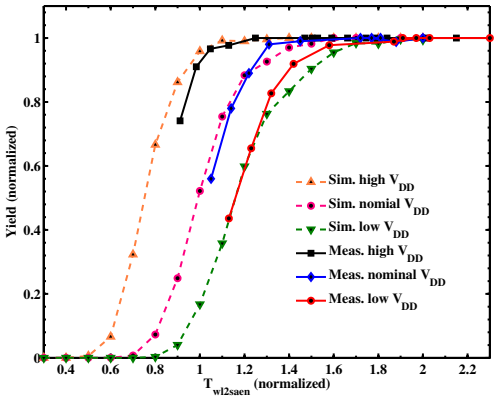

Figure 7: Comparison between the proposed yield estimation methodology and measured access yield for a 1Mb memory in 45nm technology.

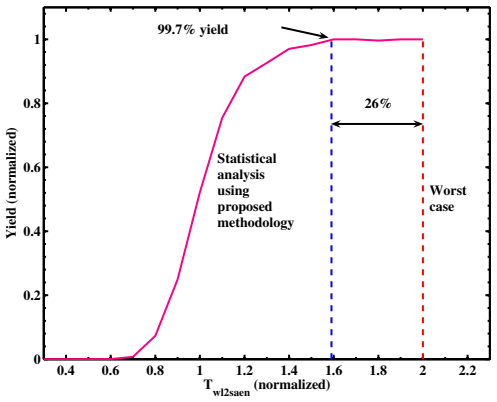

Figure 8: Comparison between the proposed statistical yield estimation methodology and worst-case analysis.

usually used in SRAM design. The methodology is verified using measured yield data from a 1Mb memory in an industrial 45nm technology. The proposed statistical SRAM yield estimation methodology allows early yield prediction in the design cycle, which can be used to trade off performance and power requirements for SRAM.

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