A Dual-28Gb/s Digital-Assisted Distributed Driver with CDR for Optical-DAC PAM4 Modulation in 40nm CMOS

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***Abstract*—This paper presents a dual 28Gb/s modulator driver with on-chip PAM4 clock and data recovery (CDR) in 40nm CMOS. Used in the 400G Ethernet, 56Gb/s PAM4 signal is recovered by the CDR and demodulates into dual-28Gb/s NRZ data streams to drive the silicon photonic MZM DAC. Push-pull driver cells are employed to reuse the current for power saving with high-swing output. A digital-assisted distributed topology is proposed, extending the driver bandwidth and enabling low-power flexible pre-emphasis within each segment. Precise retiming is implemented by phase interpolation for the velocity match both in distributed driver segments and MZM DAC segments. Measurement results show the CDR+driver achieves 4Vpp differential voltage swing, 1.78ps RMS jitter and 1.34W power consumption (including PAM4 CDR and dual-channel driver) at 50Gb/s PAM4 input, while the standalone driver contributes to 1.5ps RMS jitter at 28Gb/s NRZ outputs.**

***Keywords*— silicon photonics, MZ modulator, driver, CMOS**

I. Introduction

The ever-growing bandwidth of the datacenter interconnects is evolving from 100 to 400Gb/s. One of the promising solutions to achieve 400G (400GBase-LR8) is to build 8-channel 50Gb/s data links running in parallel with PAM4 modulation. Due to the high wavelength stability, high-linearity and wide bandwidth, the Mach-Zehnder modulator (MZM)-based link is widely employed for medium and long-range optical interconnects intra and inter the datacenters [1]. The PAM4 modulator driver is required to be linear with high-swing outputs and high-bandwidth. Standalone driver chips implemented in SiGe or III-V process are thus common, which features high power consumption and low integration level.

For data rate beyond 25Gb/s, the input channel loss introduces significant ISI and data-dependent jitter (DDJ), which could only be removed through data decision and retiming. A PAM4 CDR is needed prior to the 50Gb/s MZM driver (Fig. 1), which removes the jitter and enlarges the link margin. Moreover, the distributed amplifier (DA) topology is usually adopted to extend the bandwidth, which absorbs the circuit parasitic capacitor into a T-line [2] [3] [4]. However, besides of the intrinsic driver bandwidth, additional pre-emphasis is always needed for the MZM and E/O co-packaging, which is preferred to be flexible. In this work, a digital-assisted distributed topology is proposed, which utilizes the multi-phase clock recovered by the integrated CDR, providing in-segment tunable pre-emphasis without power-hungry analog delay cells, as well as precisely regulating the propagating timing across all segments of the DA.

Thirdly, the PAM4 modulation is traditionally realized in the electrical domain by outputting 4-level analog signals from the driver. The limited tolerable voltage swing is further divided by 3, which leads to poor extinction ratio. An alternative way is to implement it in the optical domain, by driving an MZM DAC with multiple low-swing drivers [3]. Particularly, a two segments MZM weighted by length can be driven by a dual-NRZ driver proposed in this work for the PAM4 modulation. Precise electrical/optical velocity match across the two segments is regulated by phase interpolation and in-segment 2:1 multiplexing.

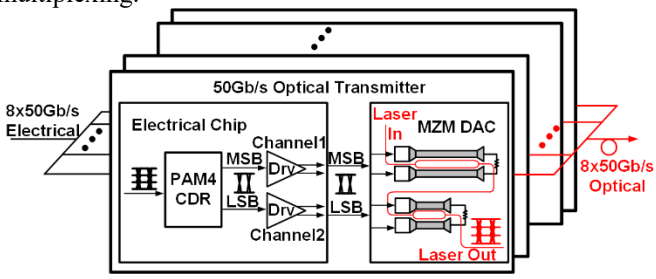

Fig. 1 8x50Gb/s optical transmitter array for 400GbE

II. System Architecture

Fig. 2 shows the block diagram of the proposed driver, consisting of a PAM4 CDR, a distributed driver and an interface between them. To characterize the driver performance without CDR, a PRBS pattern generator is integrated generating quadrature-phase clocks with the aid of external clock to produce dual channel 4Vpp swing outputs for MZM. In the CDR+driver mode, the CDR directly recovers clock from the 50Gb/s PAM4 signal and makes data decision by sampling the PAM4 signal with the recovered clock.

The PAM4 CDR incorporates the half-rate Bang-Bang phase detector (BB PD), charge pump (CP), loop filter (LPF), voltage controlled oscillator (VCO) and clock distribution chain. The PD receives input PAM4 signals and produces recovered data and UP/DN signals to CP, with sampling clocks from VCO and frequency divider. By tuning the CP current and resistor of LPF, 5-15MHz bandwidth is implemented.

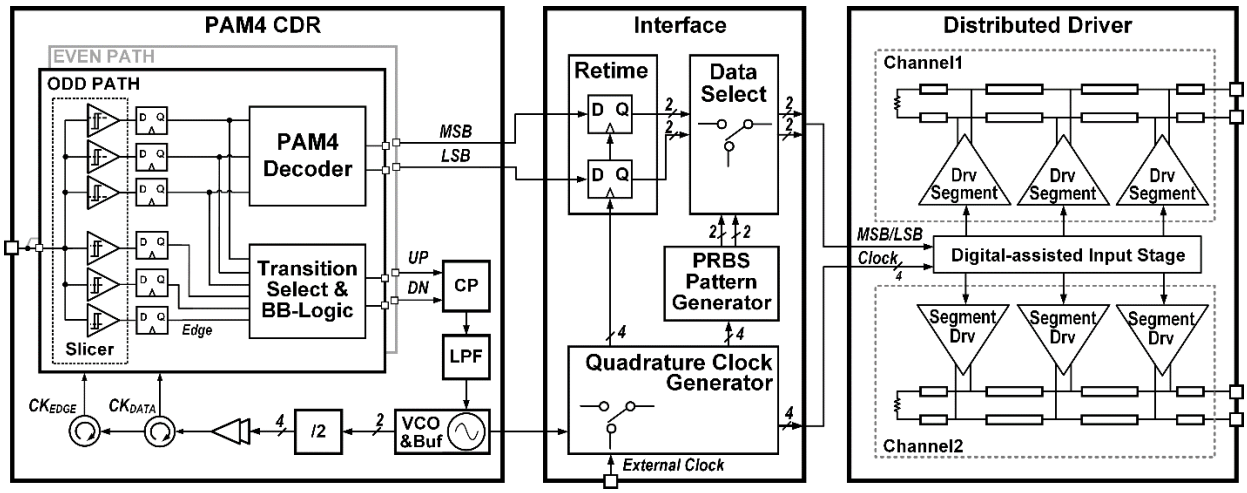

Fig. 2. Schematic of the system diagram of the proposed MZM driver

In the Interface, there are quadrature clock generator, PRBS pattern generator, data retimer and data selector. The quadrature clock generator consists of a clock selection switch and a CML high speed /2 divider. The PRBS pattern generator produces 4 bits half-rate PRBS7 data stream. The data from CDR is retimed by quadrature clock I and Q before feeding to two channels of the driver. The data fed to driver is chosen by the data selector. With the clock and data selector, the work states of the driver are configurable.

As there is optical velocity delay between two segments of MZM DAC, the retimer is precisely designed to eliminate distortion of optical PAM4 signal. The MSB data and LSB data are retimed by quadrature clock I and Q, which is digitally adjustable from 0 to 2π. The delay between retimed MSB and LSB data is optimized with good match to the optical delay.

The Distributed Driver consists of a digital-assisted input chain and two channels distributed driver, in which there are three segment drivers and the artificial transmission line.

III. Driver Implementation

There are four challenges in the design of distributed MZM driver. Firstly, a ~4Vpp large voltage swing is required, which means a large tail current in current-mode driver. The second challenge is bandwidth limit caused by large parasitic capacitance of large size transistors. Thirdly, the delay matching of input stages with output transmission line, which has great impact on output signal. The fourth challenge is accurate timing control of feed forward equalization (FFE) taps, considering the PVT variation of previous analog delay cells.

A. Distributed driver design

To achieve over 4Vpp output with 50Ω load, the push-pull amplifier in segment driver is used with current efficiency improvement than conventional CML structure [3] [5]. The proposed cascode push-pull amplifier circuit is shown in Fig. 3. The thick oxide MOS transistor M_{N3}, M_{N4}, M_{P3}, M_{P4} is used as the common gate of the cascode to protect the transistors from breakdown, considering the single-end 2Vpp swing at the output node. However, the output bandwidth is severely limited by large parasitic capacitance of these thick oxide transistors, especially the stack of NMOS and PMOS comparing to only NMOS in CML. To extend the bandwidth, the DA structure is proposed with artificial transmission line to absorb the parasitic capacitance.

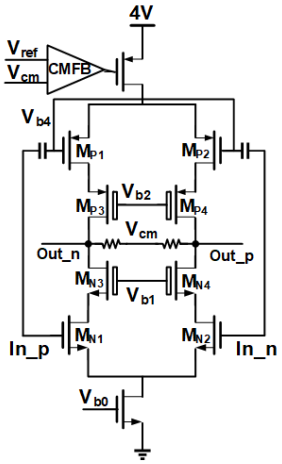

Fig. 3 The cascode push-pull amplifier in segment driver

The detailed circuits of proposed driver is shown in Fig. 4. Every segment driver shown in Fig. 2 includes a phase interpolator (PI), a 2:1 multiplexer (MUX) and a two-taps driver with main tap and post tap for FFE. The PI is used to adjust the sampling clock phase between 0 to 2π with control words. The MUX works as the serializer to produce full-rate data for driver stage. The digital-assisted input chain incorporates a quadrature clock distribution chain with three stages clock buffers (CK BUF) and two inverter-based data distribution chains for channel1 and channel2, respectively.

Based on the DA and artificial transmission line to extend bandwidth, the input delay matching is important for output signal quality. Previous works [3] use transmission line for input data distribution, which is hard to adjust the delay time and faced with attenuation, reflection and distortion. To make the input delay matching flexibly adjustable, the digitally controlled distributed amplifier was proposed [4]. In [4], the full-rate data is retimed by digitally controlled full-rate clock before feeding to predriver. By adjusting the clock phase with

clock synchronization circuit, the input delay matching is digitally controlled.

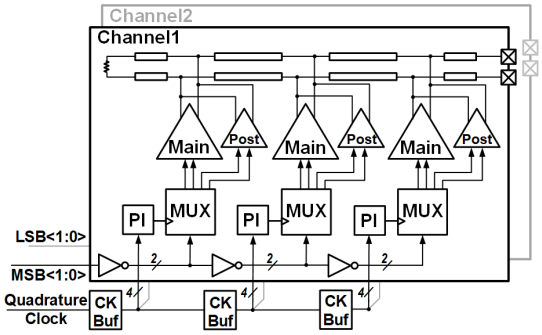

Fig. 4 Block diagrams of proposed two channels distributed driver

In this work, the digital-assisted input delay matching is utilized with half-rate architecture, including both half-rate quadrature clock and half-rate data, which is different from the full-rate architecture in [4]. One of the most significant advantages of the half-rate architecture is the large sampling margin for the retiming clock, which exhibits nearly two times wider adjusting region, shown in Fig. 5 (a). The large sampling margin is especially of great importance when the jitter of input data is large, which would compress the high SNR sampling location significantly. Additionally, the half-rate architecture is power efficient than the full-rate architecture.

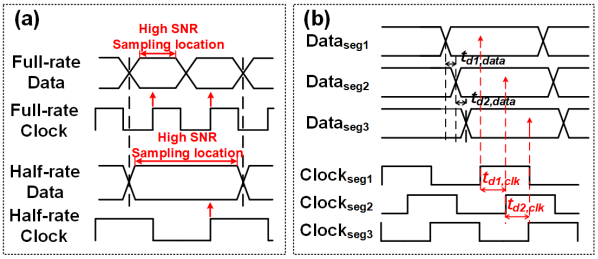

Fig. 5 (a) High SNR sampling region comparison between full-rate and half-rate architecture, (b) Timing diagram of input data and clock of three segments

The input delay calibration procedure of three segments is divided to three steps, the timing diagram of input data and clock of three segments is shown in Fig. 5 (b). Because the inverters are used to distribute the data, there are some delay of the input data between any two segments, denoted as $t_{d1,data}$ and $t_{d2,data}$.The first step is single segment calibration by tuning the polarity and strength of quadrature clock I/IB and Q/QB to get the optimized sampling range and the corresponding PI control words for every segment. At the next step, adjust the second clock phase to the center of optimized sampling range of the second segment to guarantee the global optimized sampling. The third step is tuning the clock phases of the first segment and the third segment based on the control words setting of the second clock phase to get an optimized eye diagram at the channel output. The relative clock phases of three segments is shown in Fig. 5 (b), the delays are denoted as $t_{d1,clk}$ and $t_{d2,clk}$. The accurate delay times are determined by the length of output transmission line and the delay times of the inverters and clock buffers.

B. *Accurate timing control of FFE taps*

Besides the transmission line for bandwidth enhancement, the feed forward equalization (FFE) is incorporated to improve the output bandwidth and compensate the output channel loss, like bonding wire, PCB trace and MZM transmission line. In previous work [3], the analog delay cells are utilized to produce one or more unit interval (UI) delay for FFE taps. However, analog delay cell is less flexible, power hungry and sensitive to PVT variation. Based on the proposed digital-assisted input chain, a 2-to-1 MUX shown in Fig. 4 is designed to produce data for main-tap and post-tap with accurate 1UI delay. Firstly, the 2 bits data is retimed by clock from PI with two D-flipflop. Then three D-flipflop are utilized to make accurate 1 UI delay between main-tap and post-tap data

IV. Experimental Results

The proposed driver was fabricated in standard 40nm CMOS process, occupying 2.24mm^2 area including ESD, PADs and decoupling capacitors, the chip photograph is shown in Fig. 6. Each channel of the distributed driver occupies 0.25mm^2, including artificial transmission line.

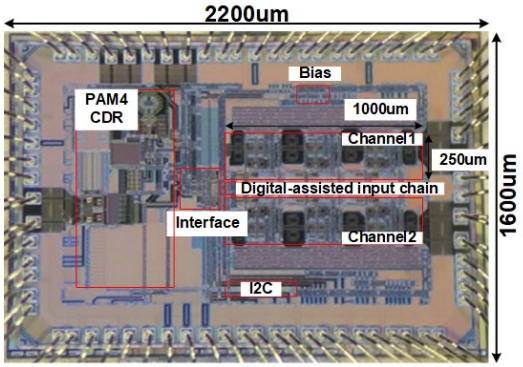

Fig. 6 MZM driver photograph

A differential full-rate clock is provided by a programmable pattern generator (Keysight M9505A) as the clock source of quadrature clock generator and on-chip PRBS generator. The differential output of the driver is firstly connected with DC block and 12dB attenuator and fed to the wide-band oscilloscope. With 25GHz and 28GHz clock in, the 25Gb/s and 28Gb/s NRZ electrical signals were produced in every channel with good input delay matching, the clear eye diagrams were shown in Fig. 7.

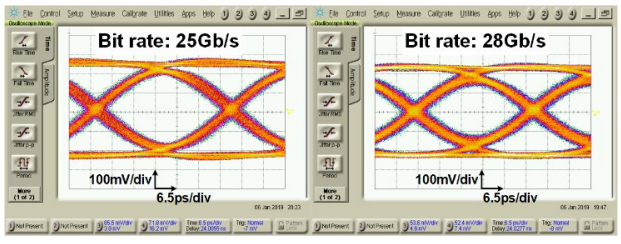

Fig. 7 Measured driver output eye diagrams at different speeds

The input delay matching is calibrated according to the calibration procedure illustrated above. To illustrate the effect of input delay mismatch, the optimized delay setting is changed

with different extra delay offset. As shown in Fig. 8, comparing to the good delay matching in (a), the (b), (c), (d) are distorted with different delay offsets. Apparently, the eyes closed gradually as more segments with delay offsets.

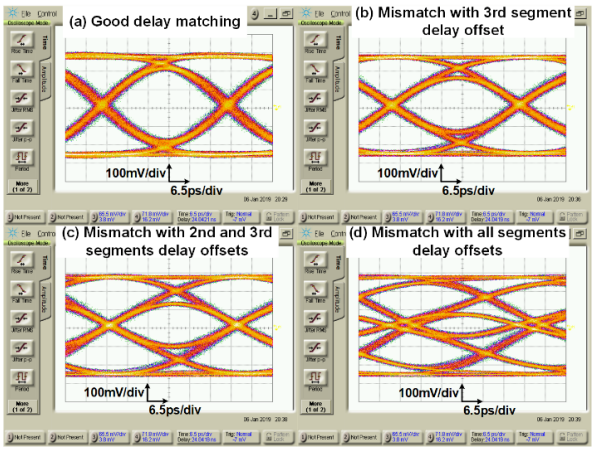

Fig. 8 Eye diagrams of 25Gb/s driver outputs with different input delay offset

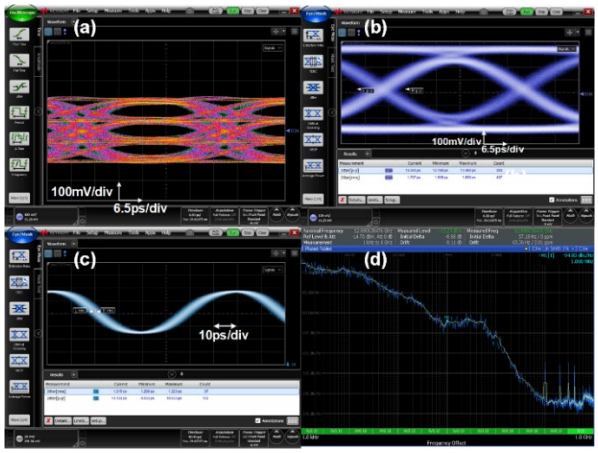

Fig. 9 (a) 25.78Gbaud PAM4 signal input, (b) driver output of recovered MSB data, (c) recovered half-rate clock, (d) phase noise of recovered clock

In the joint test of CDR+Driver, a 25.78Gbaud PAM4 signal with 300mVpp swing is fed to CDR, shown in Fig. 9 (a). The Fig. 9 (b) is eye diagram of driver output of recovered MSB data with 1.79ps $jitter_{RMS}$ and 13.3ps $jitter_{p-p}$, (c) is eye diagram of recovered half-rate clock with 1.22ps $jitter_{RMS}$ and 10.1ps $jitter_{p-p}$, (d) is phase noise curve of recovered clock with 94.8 dBc/Hz at 1MHz offset.

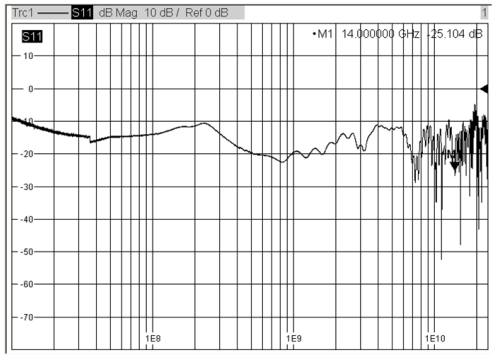

Fig. 10 Measured output return loss of proposed MZM driver (single-ended)

To eliminate the reflection of on-chip artificial transmission line, bonding wire and TW-MZM transmission line, a differential 100Ω back termination resistor is utilized. Output return loss S22 is measured with all segments open. A good impedance matching is achieved with less than -10dB S22 measured from 10MHz to over 14GHz.

Table 1 summarizes the performance metrics of this work and makes comparisons with the recent published MZM drivers.

Table 1. Performance summary and comparisons

	[2] OFC15	[4] JSSC17	[6] RFIC15	This work
Data Rate(Gb/s)	25	40	30	28
Equalization	No	No	No	**FFE**
Driver structure	DA	DA	Single	DA
Input mode	Analog	Digital	Analog	**Digital**
Output Swing(V)	6.4	6	3.3	4
Area(mm2)	No	1.8	0.072	0.25
Power(mW)	520	1920	438.5	585*/channel
Process	65nm CMOS	130nm SiGe	65nm CMOS	40nm CMOS

*Including Interface and clock distribution

V. Conclusion

A dual 28Gb/s modulator driver with on-chip PAM4 CDR is proposed in 40nm CMOS. Push-pull driver cells are employed to reuse current and generate high-swing output. The digital-assisted DA extends the bandwidth and enables low-power flexible pre-emphasis in segments. Precise retiming is implemented by phase interpolation for the velocity match both in distributed driver segments and MZM DAC segments. Based on techniques above, the driver is implemented in 40nm CMOS and tested with 4Vpp output swing, 1.5ps RMS jitter at 28Gb/s.

Acknowledgment

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