2.3 A 1.2V 23nm 6F² 4Gb DDR3 SDRAM with Local-Bitline Sense Amplifier, Hybrid LIO Sense Amplifier and Dummy-Less Array Architecture

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We present a sensing scheme with local bitline sense amplifier (L-BLSA) for sub-1V DRAM core operation, which activates a low-Vt latch locally in time, the same as [1] but shares a common ground with a high-Vt latch. Hybrid LIO sense amplifier (H-LSA) is developed for robust LIO read operation at low voltage and high clock frequency. In order to reduce the die area, we develop a dummy-less $6F^2$ array architecture with no edge dummy array. These schemes are employed in a 1.2V 23nm $6F^2$ 4Gb DDR3 SDRAM.

For sub-1V DRAM core operation, [1] proposes an LGA bitline sense amplifier that operates as depicted in Fig. 2.3.1(b). In this paper, we present an evolutionary version of LGA, the local bitline sense amplifier (L-BLSA), shown in Fig. 2.3.1(a). The L-BLSA activates a low-Vt latch locally in time, the same as LGA [1] but shares the common ground node (SB) with the high-Vt latch. The advantage of L-BLSA over LGA comes from the fact that LGA scheme is vulnerable to standby current issue. When DRAM enters precharge standby state, the drain-source bias voltage of LGA's M1, M2 through M7, M8 (SG) Tr. is VBLP (BL precharge voltage). At such a V_{DS} voltage, SG transistor's V_{th} should be modified to large one in order to remove standby current issue. In our calculation, SG's V_{th} should be modified more than 300mV to be free from the standby current issue. A 300mV V_{th} change does not fit for practical implementation. On the contrary to LGA, L-BLSA is robust to standby current issue as shown in Fig. 2.3.1(a).

The operation method of L-BLSA is shown at Fig. 2.3.1(d). SG signal is activated simultaneously with SB signal during the bitline sensing period. During cell read, Yi and SG signals are activated simultaneously. SG is fixed to ground during write operation so the write driver does not fight with L-BLSA. Figure 2.3.1(e) shows the simulation result of L-BLSA compared to conventional bitline sense amplifier. The minimum of tRCD+tAA means the minimum delay from bitline sensing start to 200mV LIO voltage development at read operation in the presence of the worst case V_{th} mismatch, bitline coupling and SIO coupling [2]. L-BLSA makes tRCD+tAA faster by 1.2ns compared to C-BLSA at V_{DD}=1.0V, V_{CORE}=0.9V, 100˚C.

A local sense amplifier scheme is adopted in the DRAM SIO/LIO multiplexer as a substitute for a simple SIO-LIO switch (IOSW) scheme [3-4]. When DRAM reads the cell data, Yi transfers BL data to SIO/LIO while SIO/LIO capacitance distorts BL data. Interaction between bitline and SIO/LIO shows itself as 2nd read tRCD and BLSA stability issue [2]. LSA reduces the bitline and SIO/LIO interaction in such a way that SIO and LIO are completely isolated and SIO/LIO capacitance shrinks to lessen bitline/SIO interaction. Figure 2.3.2 shows our hybrid LIO sense amplifier (H-LSA) (a) in parallel with the original LSA [4] (b) and IOSW (c).

During the read period, hybrid LSA drives IOSW transistor's gate to the regulated voltage (~1.4V). At early stage of I/O sensing, SIO and LIO are isolated so that H-LSA is free from BLSA stability and 2nd read tRCD issue. When SIO voltage swing is growing, IOSW transistor turns on strong between SIO and LIO so that it limits SIO voltage swing. Reduced SIO voltage swing reduces SIO coupling noise. In effect, H-LSA reduces SIO coupling noise compared to that of Orig. LSA. Figure 2.3.3 shows the simulation waveforms of H-LSA, Original-LSA and IOSW scheme.

In order to fully utilize the edge array of a $6F^2$ open bitline architecture, [5] proposes that the edge arrays consist of half-length BLs with the adjacent BLs connected together to achieve the same capacitance as in the normal array. To further decrease die area and increase net-die, dummy-less $6F^2$ open bitline array architecture is developed in this work. As shown in Fig. 2.3.4(b), an edge BLSA is connected to a dummy bitline so that we can utilize the dummy bitline. The edge BLSA will be unbalanced in bitline capacitance between True and Bar (Fig. 2.3.4(c)). The effect of capacitance mismatch to SA operation is investigated through simulation as shown in Fig. 2.3.5.

We calculate the bitline-sensing offset for different data patterns (solid-island, 0data-1data). The minimum bitline voltage difference for the correct sensing is defined as the sensing offset. The sensing offset is affected by several factors and dominated by sense amplifier NMOS V_{th} mismatch, which can be modeled as a Gaussian random variable in offset simulation. There is a different sensing offset depending on the data polarity (0 data, 1 data). The other major factor is the data pattern, such as solid and island. The solid "0" and island "1" data patterns complement each other in a way that the "0" and "1" target bitlines are surrounded by the background data "0". The same is true for the solid "1" and island "0". It is straightforward to carry out the sensing offset simulations for solid "0", island "1", solid "1" and island "0" as shown in Fig. 2.3.5.

Capacitance mismatch makes the "1" offset small and the "0" offset large as Fig. 2.3.5(b) shows. This is due to the SB fast sensing that the lightly loaded reference bitline discharges to ground easily so that the "1" offset decreases and "0" offset increases. Solid data offset is larger than that of island data. Usually the reverse is true for normal bitline sensing as shown in Fig. 2.3.5(a). The reason for the reversal is the Miller-feedback effect of BLSA. Due to Miller capacitance of BLSA, solid data pattern's BL more significantly affects the lightly loaded reference BL than in the case of island data pattern. To recover 0 data offset, we use the charge-coupling capacitor array made by MOS transistors so that reference BL is boosted upward by coupling capacitance. The Miller effect is reduced on the reference BL capacitance and is adjusted by the capacitor array, which is controlled by test mode code TM<0:2>, shown in Fig. 2.3.5(c). Charge-coupling capacitors correct the "0", "1" data-offset change and solid-island offset gap as shown in Fig. 2.3.5(c).

The shmoo plots for tRCD and tCK vs. V_{DD} are shown in Fig. 2.3.6 (a) and (b), respectively. Low-voltage tRCD and tCK at V_{DD}=1.2V, 100˚C are measured to be 9.9ns and 1.1ns, respectively. A micrograph of the fabricated 23nm $6F^2$ 4Gb DDR3 SDRAM is shown in Fig. 2.3.7. A 23nm $6F^2$ cell technology is developed with 2Cu+1Al metals and dual-gate CMOS process. The chip area is 30.9mm². Figure 2.3.7 summaries key design features.

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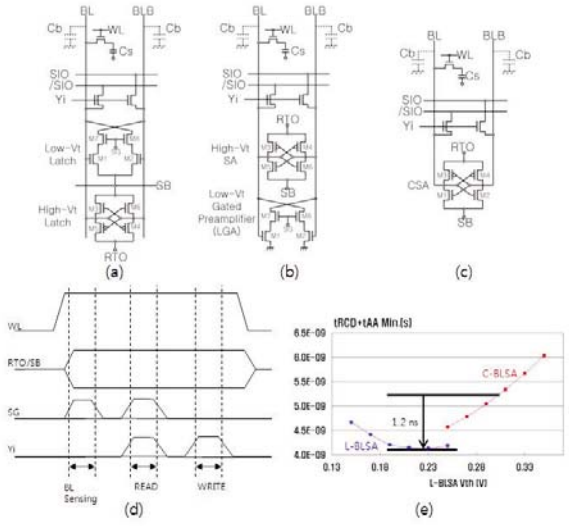


Figure 2.3.1: (a) L-BLSA, (b) LGA[1], (c) conventional BLSA, (d) L-BLSA operation method, (e) tRCD+tAA min. sim. result of L-BLSA vs. C-BLSA.

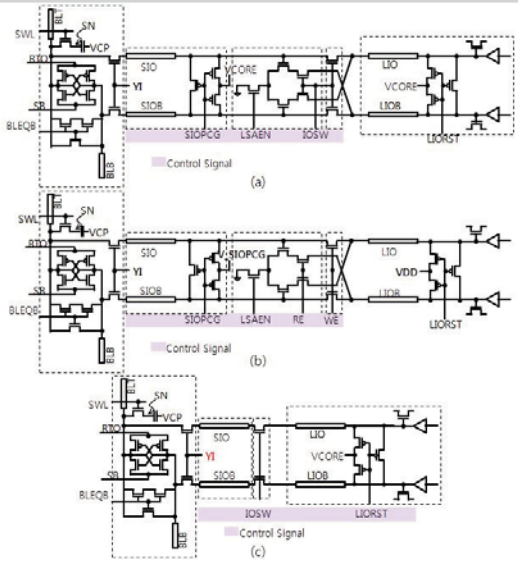


Figure 2.3.2: Schematics of (a) H-LSA, (b) Original LSA, (c) IOSW.

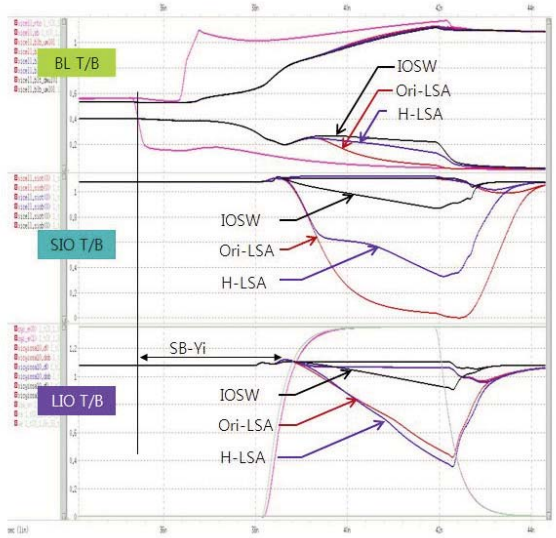


Figure 2.3.3: Simulation waveforms of H-LSA, O-LSA and IOSW scheme.

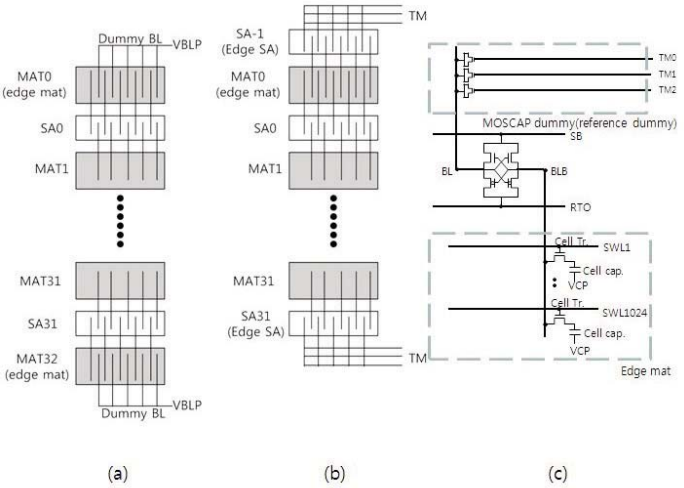


Figure 2.3.4: 6F2 Open-bit line architecture (a) conventional, (b) dummy-less array and (c) edge BLSA schematic.

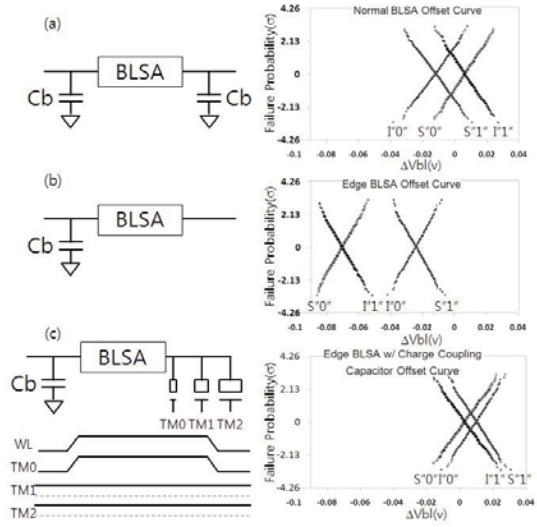


Figure 2.3.5: Sensing offset simulation results for (a) normal BLSA, (b) edge BLSA and (c) edge BLSA with charge coupling capacitors.

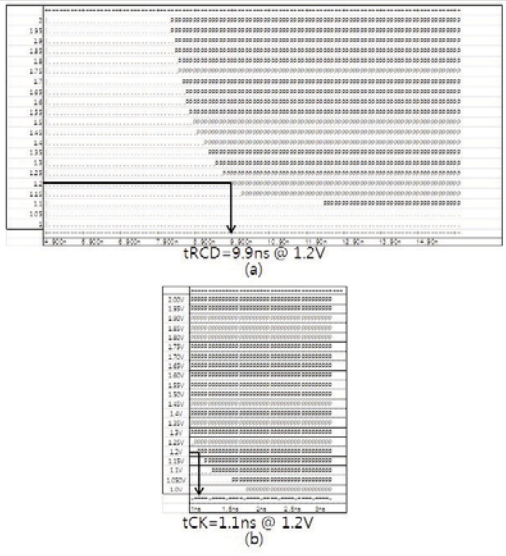
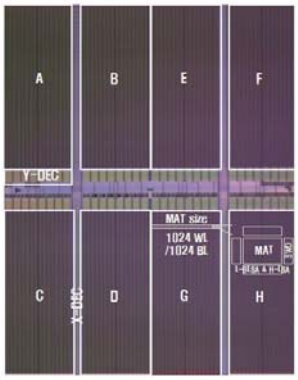


Figure 2.3.6: Shmoo plots for (a) tRCD and (b) tCK vs V_{DD} characteristic.



	Features
Process	23nm, 2Cu+1AL 6F2 Cell Dual gate CMOS DRAM process
Chip size	30.9mm² (1024 cell/BL, 1024 cell/WL)
Organization	8 bank, x4/x8
Operating Voltage	1.2V
DRAM core operating voltage	1.05V

Figure 2.3.7: Micrograph of fabricated 23nm 4Gb DDR3 SDRAM and summary of design features.

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