A Digitally Calibrated 64.3-66.2GHz Phase-Locked Loop

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***Abstract* — In this paper, a 64.3-66.2GHz digitally calibrated phase-locked loop (PLL) is presented in 0.13µm CMOS technology. A digital calibration circuit is adopted to align the center operation frequency between the VCO and the divider. At 64.3GHz, the measured phase noise at 1MHz offset is 84.1dBc/Hz. The PLL consumes 72mW without output buffers from 1.2V supply.**

***Index Terms* — Phase-locked loop, frequency divider, digital calibration, CMOS, clock generator.**

I. Introduction

The broadband communication systems require high-speed receivers to transmit and receive serial data at tens of gigabits per second. In wireless communications, the millimeter wave band of 57-66GHz has been announced for the general unlicensed use and it offers the wireless communication at several gigabits data transmission. In wireline communications, 100Gbps Ethernet may be the next generation standard. Therefore, a very high-speed clock generator is indispensable while realize the transceiver for those broadband wireless and wireline communication. However, due to inaccurate passive/active device modeling and large process variations in millimeter-wave band, the tuning range of the VCO and the operational range of the first FD may not align exactly. Thus, it may result in the millimeter-wave PLL fail to work. Hence, a digitally calibrated injection-locked FD (ILFD) and the digital calibration circuit are presented to overcome the above issues. By adopting the proposed calibration method, the proposed PLL can reduce the effect of inaccurate device modeling and then operate during the frequency range from 64.3 to 66.2GHz.

II. Proposed Architecture

Fig. 1 shows the block diagram of the proposed digitally calibrated PLL. This PLL is composed of a push-push voltage-controlled oscillator (VCO)[1], a digitally calibrated ILFD, a divide-by-64 static divider chain,

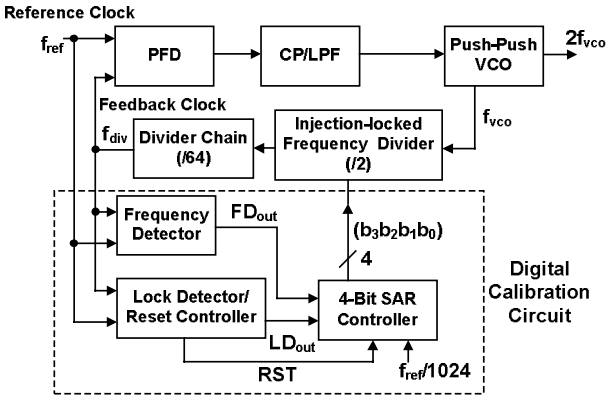

Fig. 1. The proposed digitally calibrated PLL.

a phase frequency divider (PFD), a charge pump (CP), a loop filter, and a digital calibration circuit. The digital calibration circuit includes a frequency detector (FD)[2], a locked detector(LD) with the reset controller, and a 4-bit successive-approximation register(SAR) controller[3]. According to the input reference frequency, this digital calibration circuit calibrates the free running frequency of the digitally calibrated ILFD by a binary search algorithm.

Next, the operation of the digital calibration circuit is briefly described as follows. In Fig. 1, if a PLL is designed to work with the widest operational range, the free running frequency f_{free} of the ILFD should be equal to $64f_{ref}$. However, it may not be true, owing to the process variations and inaccurate device modeling. In the beginning, assume the ILFD can not divide the f_{vco} properly and the ILFD outputs its free running frequency, the output of the ILFD is divided by the divide-by-64 divider chain. Thus, the divider chain generates the feedback clock with the frequency of the f_{div}. Then, a conventional digital quadricorrelator FD compares the reference clock (f_{ref}) with the feedback clock (f_{div}). By the binary search algorithm, the output FD_{out} of the FD will enable the SAR controller and then output the digital code ($b_3b_2b_1b_0$) to adjust the free running frequency of the ILFD. The calibration circuit allows the free running frequency of the ILFD is closed to $64f_{ref}$ after four searching cycle. According to the calibration method, the digitally calibrated PLL will re-lock again while every controlled

bit is generated. In the worse case, the proposed PLL needs four re-locked cycles. Fortunately, if the ILFD can divide the f_{vco} during the four searching cycle, the LD will notify the SAR controller to stop the calibration algorithm and shorten the locked time of the PLL within four re-locked cycles.

III. Circuit Description

In the section, the circuit blocks include the push-push VCO, digitally calibrated ILFD, and the digital calibration circuit will be illustrated briefly as follows.

A. Push-push VCO

Fig. 2 shows the circuit diagram of the push-push VCO. It is composed of a conventional LC VCO and a push-push frequency doubler[1]. The conventional VCO is realized by a NMOS cross-coupled pair, a symmetric inductor, and two NMOS varactors. The push-push frequency doubler is composed of two NMOS transistor and three inductors. According to [1], as the two input signals of the push-push doubler is fully differential, the transistor M_3 is turned on and M_4 is turned off in the time period t_0 to t_1. The AC small signal current flows through M_3 toward the output load inductor and it causes a voltage drop at the output node. On the contrary, M_4 is turn on and M_3 is turned off during the time period t_1 to t_2, it also makes a voltage drop during this time period. Since the output waveform of output node is exactly the same during the two time period, the frequency of the output waveform is twice of the input signal frequency.

B. Digitally calibrated ILFD

Fig. 3 shows the digitally calibrated ILFD. The proposed ILFD consists of a differential injection-locked frequency divider modified from[4] and a digitally controlled capacitor array. In the proposed ILFD, the free running frequency of the ILFD depends on the effective capacitance of the digitally controlled capacitor array. The capacitor array is composed of eight binary-weighted NMOS varactors. Depending on the controlled code ($b_3b_2b_1b_0$) form the SAR controller, its capacitance is scaled from C_0 to $8C_0$. Therefore, the digitally controlled capacitor array not only changes the free running frequency of the ILFD, but also extends the operation range of the frequency divider.

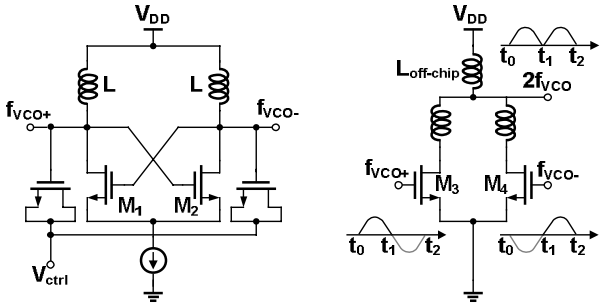

Fig. 2. The circuit diagram of push-push VCO.

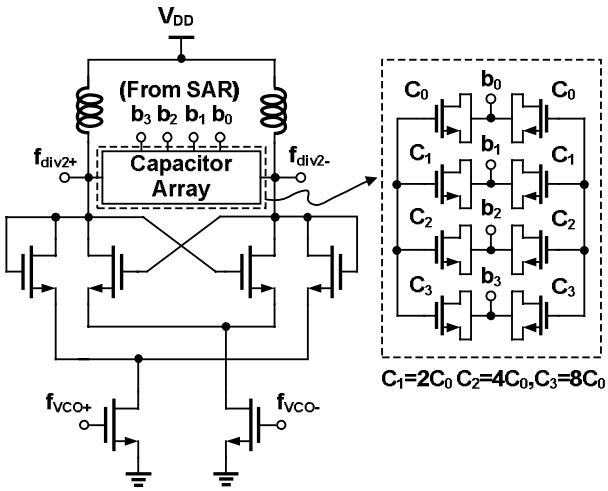

Fig. 3. The digitally calibrated injection-locked frequency divider.

C. Digital calibration circuit

The digital calibration circuit consists of three parts, the FD, LD with reset controller, and 4-bit SAR controller. The architecture of the FD is similar with[2]. As the timing diagram shown in Fig. 4(a), the FD_{out} will output logic 1 and logic 0 when the $f_{div}>f_{ref}$ or $f_{div}<f_{ref}$, respectively. The LD is shown as Fig. 4(b). In the LD structure, two delay lines, ΔT and $2\Delta T$, realize the time window to judge whether the frequencies of these two clocks are close enough or not. Two DFFs are used to sample the reference clock (f_{ref}) and feedback clocks (f_{div}). Supposed $f_{ref}=f_{div}$, when the reference clock leads or lags the feedback clock by less than ΔT, the LD outputs LD_{out} =high to indicate this PLL locked. Finally, the high signal of LD_{out} will stop the 4-bit SAR controller simultaneously. Furthermore, to eliminate the undesired glitch, the right-hand-side two DFFs and the AND gate in Fig. 4(b) are added.

Fig. 4(c) shows the reset controller and it is used to reset the SAR controller. For some undesired

perturbations, LD_{out} of the LD may transit from high to low and it indicates that the PLL is out of lock. From the timing diagram in Fig. 4(c), the signal RST will be low after LD_{out} transits from high to low. A short low pulse of RST resets the SAR controller and allows the digital calibration circuit to re-start again. Eventually, the signal RST recovers to high again and the SAR controller work normally.

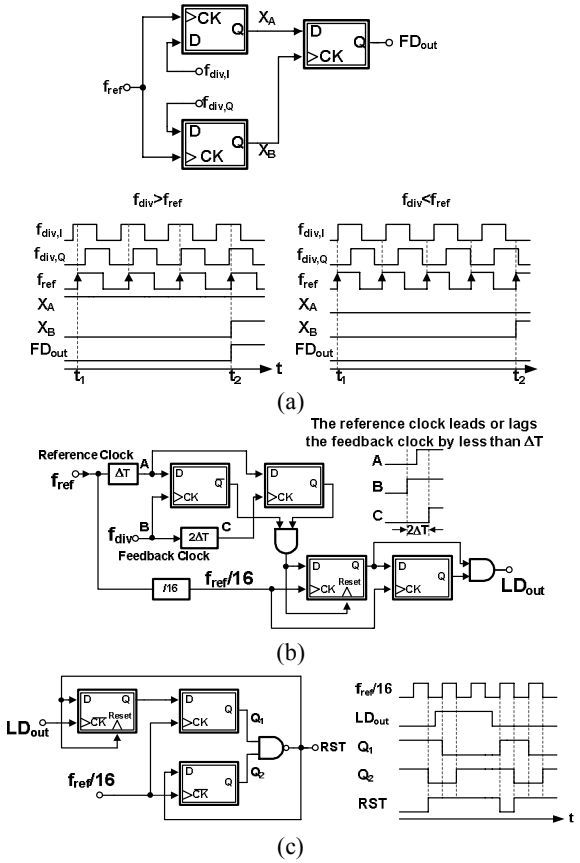

Fig. 4. The block diagrams of (a) frequency detector, (b) lock detector, and (c) reset controller.

IV. Experimental Results

Fig. 5 shows the chip micrograph of the digitally calibrated PLL, which occupies 1.24×1.14 mm^2 including pads. The loop filter is entirely off-chip. The simulated loop bandwidth, the damping factor, and the phase margin of this digitally calibrated PLL is 1.8MHz, 1.77, and 65^0, respectively. The simulated locked time of this proposed PLL is less than 4μs and the frequency of input reference clock is 251.3MHz. To let the SAR controller work properly, the period of the clock for the SAR controller is chosen as $f_{ref}/1024$ and its period is slightly larger than the locked time of this PLL. Therefore, in the worst case, the total locked time for this digitally calibrated PLL is 16μs to complete the SAR controller. This PLL consumes 72mW from 1.2V supply without buffers. The power consumption of the stand-alone push-push VCO is 13.2mW. As shown in Fig. 6, the measured tuning range of the push-push VCO is from 64.2 to 66.4GHz. The closed loop measurement result is shown in Fig. 7. When the frequency of input reference clock is 251.3MHz, the measured output spectrum of 64.33GHz is shown as Fig. 7. In Fig. 7, the measured phase noise at 1MHz offset is -84.16dBc/Hz. The locking range of the proposed PLL is from 64.33 to 66.2GHz by changing the reference clock. Fig. 8 presents the output code of the digital calibration circuit. After calibration, the 4-bit SAR controller outputs the code (1111) and calibrates the proposed ILFD to the highest operational band. The total locked time of the proposed is around 16μs and almost the same as the simulation results. Finally, the measured performance is summarized in Table I and compared with previous works. The poor reference spur is caused by the entire off-chip loop filter and the undesired reference clock coupling.

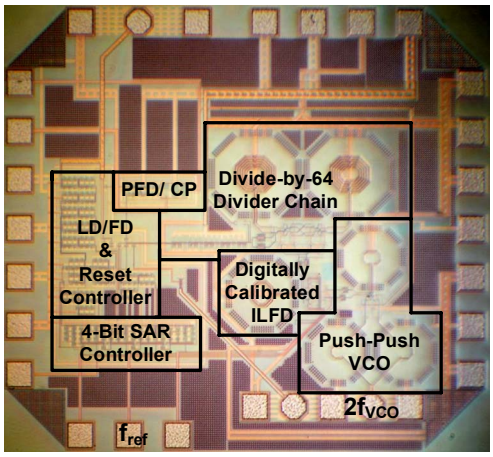

Fig. 5. Chip micrograph.

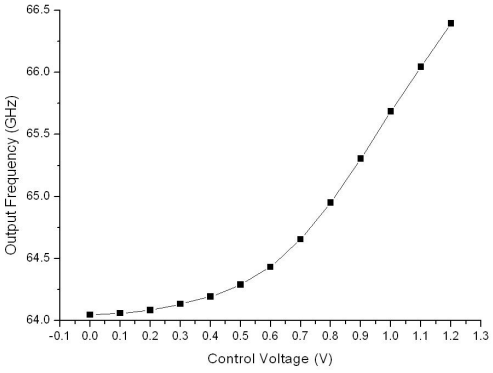

Fig. 6. Measured transfer curve of the push-push VCO.

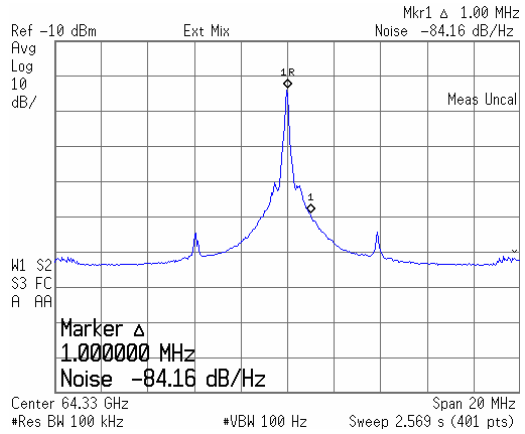

Fig. 7. The measued spectrum of the PLL.

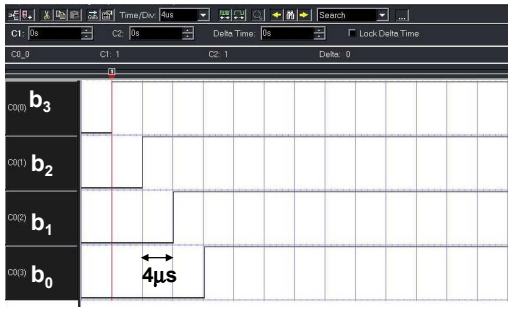

Fig. 8. Output code measurement of the 4-bit SAR controller.

V. Conclusion

In this paper, a 64.3 to 66.2GHz digitally calibrated PLL is presented for the unlicense 60GHz band application. The measured in-band phase noise at 1MHz offset and the reference spur are -84.16dBc/Hz and -15.2dBc, respectively. The proposed circuit has been fabricated in CMOS 0.13μm porcess and consumes 72mW without output buffers.

Acknowledgement

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[6]	[7]	[8]	**This work**
Locking Range (GHz)	49.5-50.5	58-60.4	75±320MHz	**64.3-66.2**
Divided Ratio	512	256/258	64	**128**
Reference Spur (dBc)	-27 to-40	-50.75	<-72	**-15.2**
Phase Noise[1] (dBc/Hz)	-72	-85.1	-88[2]	**-84.16**
Power	57mW	80mW	88mW	**72mW**
Supply Voltage	1.5V	1.2V	1.45V	**1.2V**
Technology	0.13μm CMOS	90nm CMOS	90nm CMOS	**0.13μm CMOS**
Chip Area(mm^2)	1.16×0.75	0.95×1	0.8×1	**1.24×1.14**

[1]1MHz offset, [2]100kHz offset.