RF-CMOS-MEMS based Frequency-Reconfigurable Amplifiers

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***Abstract*-Chips from a foundry RF process are post-processed to release MEMS passive devices and enable single-chip reconfigurable circuits. A MEMS variable capacitor, capable of 7:1 tuning ratio, reconfigures a narrow-band low-noise amplifier and a power amplifier over a 1 GHz frequency range. A suspended MEMS inductor, with > 50% improvement in Q, lowers amplifier power consumption.**

I. Introduction

Multiband transceivers are a critical component in envisioned software-controlled radios. In power-constrained mobile terminals, they either need wideband RF front ends, or frequency-reconfigurable narrowband front-ends. The wideband approach is fraught with inadequate sampling rates, inferior linearity and high power. An ideal solution is a fully-integrated frequency-reconfigurable architecture [1].

RF MEMS technology has the potential to help achieve this ideal solution in multiple ways. The excellent insertion loss and isolation properties of ohmic RF MEMS switches have been exploited for a switched power amplifier based on PHEMT devices [2]. Capacitive RF MEMS switches have been integrated with inductors in foundry silicon processes for reconfigurable filter and voltage-controlled oscillators [3]. The LC resonators in [3] are medium-Q (~10-100). For higher Q, micromechanical resonators are needed. An above-IC process integrating a film bulk acoustic resonator (FBAR) has been used for a 5.4 GHz oscillator [4]. FBAR resonant frequencies are set by film thicknesses. Resonators whose frequency can be lithographically defined have also been integrated in CMOS processes [5]. The examples described in [2-5] are all integrated monolithically with transistors for potential fully-integrated frequency-reconfigurable radios.

One of the advantages of integrating MEMS with CMOS is the low parasitic capacitances that can be achieved at the terminals of the MEMS devices. This not only improves tuning range, but also enhances the Q of the LC tank. This paper describes an improved reconfigurable RF CMOS-MEMS capacitor with low parasitic (< 50 fF) capacitances and high tuning range (>7:1) [6], and its use in the design of a low-noise amplifier and a switched power amplifier [7].

II. CMOS-MEMS Passive Devices

RF MEMS passive devices are integrated with foundry CMOS using the CMOS-MEMS process in [8]. Designers use the foundry metal/dielectric layers to specify particular device structure. A set of mask-less, post-foundry subtractive etch steps removes the passivation layer above the top metal, and any exposed oxide. Subsequent anisotropic and isotropic silicon etches of the underlying silicon releases the device. The resulting MEMS structures are composed of the CMOS metal/dielectric stack. This paper focuses on a 6-metal 0.18 µm and a 4-metal 0.35 µm foundry process. Multi-project wafer chips from both processes are processed identically except that the oxide etch for the 0.18 µm case is extended to compensate for the thicker 6-metal stack.

A. MEMS Variable Capacitor

A MEMS variable capacitor for use in reconfigurable RF circuits should have high tuning range, linearity and Q, and low parasitic capacitance and resistance at its terminals. The latest MEMS variable capacitor extends an electrothermal design [9], in which large displacements (~10 µm) can be achieved using low voltages (< 5V) unlike the electrostatic designs typically used in RF MEMS capacitive switches. The capacitor is formed by two sets of interdigitated beams (see Fig 1). Varying the gap between the (fixed) stator and (moveable) rotor beams using an electrothermal actuator alters the capacitance. A flexible RF interconnect (connected to Port 1) is used to route the RF signal to the interdigitated rotor beams. The interconnect connected to Port 2 does not move, but is suspended to limit parasitic capacitance to the substrate.

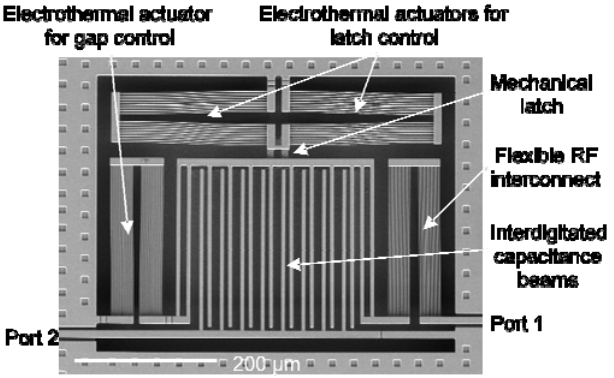

Fig 1. SEM of CMOS-MEMS variable capacitor

The electrothermal actuators are operated by passing current through polysilicon resistors embedded within the actuator structure (made from foundry gate polysilicon). For zero quiescent power operation, a mechanical latch, also controlled with electrothermal actuators, is used. The latch consists of a stair-step structure (see Fig. 2) with 11 positions resulting in 11 capacitance values, defined by lithography. Residual stresses close the latch to the self-assembled position at ambient temperatures less than 60 ºC. Heating the latch actuators retracts the stair step structure so that the rotor beams can be moved. Power to the latch actuators is shut off, and the stair-step re-engages, holding the device at a constant capacitance value until the next reconfiguration event.

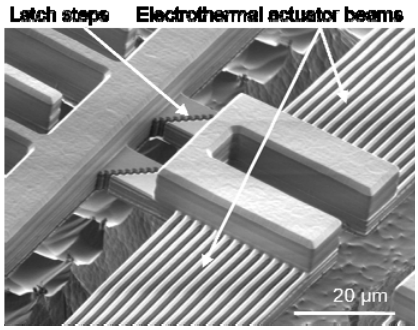

Fig. 2. SEM of stair-step structure in mechanical latch

The overall capacitor is a 7 terminal device. Each of the electrothermal actuators (for the capacitor and for the latch) requires two terminals. Three terminals are needed for the RF model as shown in Fig. 3 (Port 1 and 2 map to the labels in Fig. 1), and the ground terminal represents the substrate and the top-level protective metal used to prevent etching of the oxide and silicon around the capacitor. The RF model also includes the RF interconnect, which must simultaneously be wide for low electrical resistance, and narrow for low mechanical stiffness (such that the electrothermal actuator can close the 10 µm gap between the interdigitated capacitance beams). A parallel array of narrow beams is used in the RF interconnect to best meet these conflicting goals.

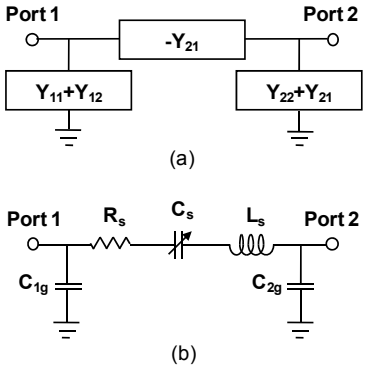

Fig. 3. Extracted (a)) Y-parameter and (b) lumped model of variable capacitor

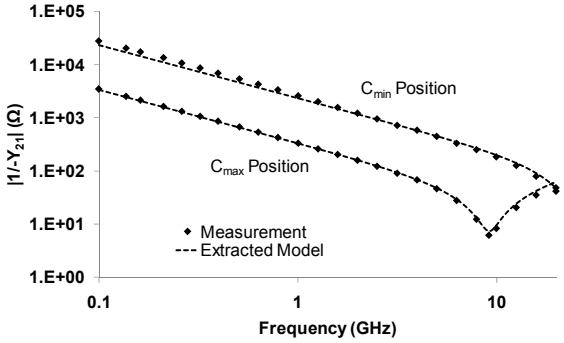

Fig. 4. Plot of magnitude of series impedance of the 0.18 µm MEMS variable capacitor for both minimum and maximum capacitance positions

The π-model in Fig. 3 is chosen to include the series resistance and capacitance of the U-shaped RF interconnect, as well as any resistance, capacitance and inductance in the interdigitated beams. The shunt capacitances at each end models the parasitic capacitance between the device and the substrate. Measured S-parameters obtained after open-short de-embedding to remove the effects of the probe pads were transformed to Y-parameters and mapped to the lumped equivalent circuit as in Fig. 3.

This model is a good fit to the capacitance at both low and high capacitance configurations as shown in Fig. 4 (only shows 0.18 µm device). C_{max} resonates with L_s at 9.2 GHz causing the dip. The maximum voltage and current needed to power the electrothermal actuators in the 0.18 µm device was 4 V and 4.6 mA. Table 1 shows the measured variable capacitor parameters for 4 different capacitors. The original 0.35 µm design [9] had poor tuning range and high shunt parasitic capacitances. An improved 0.35 µm design had better tuning range of about 7:1 and shunt parasitic of ~ 10 fF [6]. A change in the silicide between the 0.35 and 0.18 µm processes accounts for the larger shunt parasitic capacitances (C_{1g} and C_{2g}) seen in the 0.18 µm device. The silicon release etch is able to successfully remove the silicide in the 0.35 µm process, but fails to completely remove the silicide in the 0.18 µm process. Future runs will include a silicide block layer around the MEMS capacitor to prevent this. Focused-ion beam etching of substrate contacts close to the capacitor results in a device that operates as expected.

Table. 1. Measured CMOS-MEMS variable capacitor parameters

Parameter	1st Gen. 0.35 µm [9]	2nd Gen. 0.35 µm [6]	0.18 µm [This work]	0.18 µm after FIB [This work]
$C_{s,min}$	150 fF	54 fF	68 fF	65 fF
$C_{s,max}$	380 fF	372 fF	482 fF	367 fF
$C_{s,max}$:$C_{s,min}$	2.5:1	6.9:1	7.1:1	5.6:1
C_{1g}	71 fF	13 fF	440 fF	17 fF
C_{2g}	425 fF	30 fF	133 fF	35 fF
R_s	7.2 Ω	4.5 Ω	7.5 Ω	8.4 Ω
L_s	522 pH	531 pH	615 pH	621 pH
Q	18 (@ 3 GHz)	28 (@ 3 GHz)	10.8 (@ 3.5 GHz)	13.2 (@ 3.5 GHz)

B. MEMS Inductor

Foundry spiral inductors which undergo post-CMOS etching are modified in two ways [10]. First, the oxide between inductor turns is etched away, and, second, the silicon beneath the inductor is removed, suspending it more than 30 µm above the substrate. Both modifications decrease parasitic capacitance which, then, increases the self-resonant frequency and Q, giving the designer larger inductances with enhanced Q at higher operating frequencies.

III. Low Noise Amplifier

A single-stage emitter-degenerated cascaded common-emitter LNA was augmented with RF MEMS passive components [7]. MEMS variable capacitors were employed for frequency reconfiguration and MEMS inductors for high quality factors (and low power consumption). SiGe BiCMOS

transistors in both 0.35 and 0.18 µm foundry processes were chosen over CMOS transistors for concurrent low-noise and low-power operation.

The MEMS variable capacitors, C_{in} and C_{load}, were added to the input and output LC networks to reconfigure their resonance frequencies, and thus the LNA operating frequency (see Fig. 5). To achieve proper narrow-band operation, the resonance frequencies of both networks were designed to match at all operating frequencies. The L-match circuit at the output is only needed for testing. All bias voltages are externally supplied.

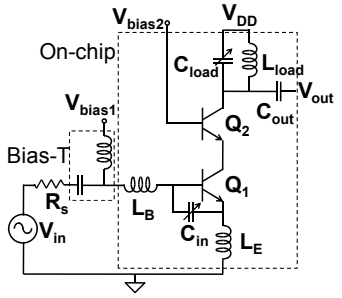

Fig. 5. Schematic of low-noise amplifier

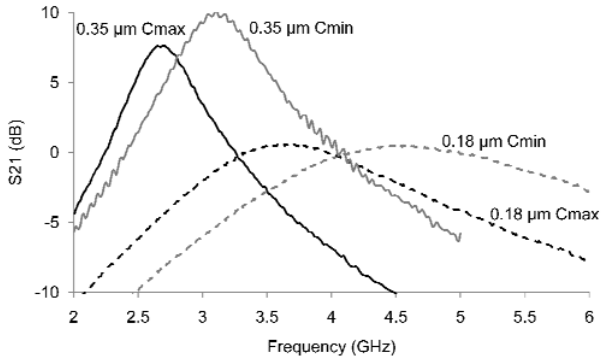

Fig. 6. Plot of low-noise amplifier S21 for both low and high frequency settings in the 0.18 and 0.35 µm LNAs.

Measured S-parameters of the LNA in 0.35 µm and 0.18 µm processes are shown in Fig. 6 and Table 2. The 0.35 µm design uses the first generation (2.5:1 tuning range) variable capacitor [9]. The 0.18 µm design uses the enhanced (7:1 tuning range) variable capacitor, and shows a wider tuning range than the 0.35 µm design. Measurements of both the gain and tuning range in the 0.18 µm are significantly less than those predicted with initial simulation, and can be explained by the higher than expected shunt parasitic capacitances. Focused-ion beam etching to fix the capacitors in the LNA is underway, and measurement results, if available will be updated in the final paper.

The 0.35 µm LNA operated as an amplifier, and additional performance measures are reported in Table 2. Using the figure of merit (computed from gain, noise figure and power consumption), this amplifier had better performance than other recently reported frequency-reconfigurable LNAs [12-14] (even from those in more advanced technologies). This is because the f_T degradation by locating C_{in} at the base-emitter of Q_1 is compensated by the high Q available from the inductors to get low overall power.

Table 2. Measured low-noise amplifier performance summary

Parameter	0.35 µm [7] (1st Gen. capacitor)		0.18 µm [This work] (2nd Gen. capacitor)	
Freq (GHz)	2.7	3.1	3.6	4.6
S21 (dB)	7.7	10.2	0.6	0.5
NF (dB)	4.2	4.7		
S11 (dB)	-30.0	-16.0	-5.4	-7.0
S22 (dB)	-6.9	-13.7	-1.9	-2.9
P_{1dB} (dBm)	-10	-11		
IIP3 (dBm)	-0.5	-3		
Power (mW)	2.5 mW		3.3 mW	
FoM [11] (S_{21}/NF*P_{DC})	0.37	0.44		

IV. Power Amplifier

The PA consists of a class E output stage [15] driven by a class B pre-amplifier (see Fig. 7). In the 0.18 µm design, frequency-reconfiguration is accomplished by a combination of MEMS variable capacitors and NMOS-switched MIM capacitors. MEMS variable capacitors are used when the design requires a variable series capacitance with low series resistance and high linearity, as is the case for C_2. Switched capacitors, C_1 and C_3, are used to minimize area when a variable one-port shunt capacitance is sufficient. In the 0.35 µm design, all the variable capacitors were MEMS-based. The input match of the pre-amplifier is simply a 50 Ω resistor shunted to RF ground to minimize area.

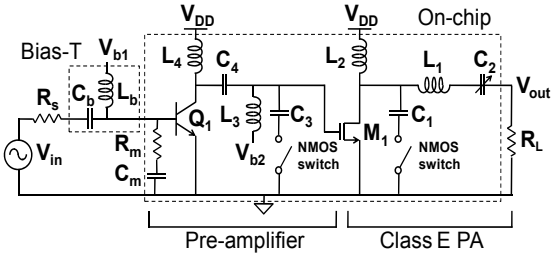

Fig. 7. Schematic of power amplifier

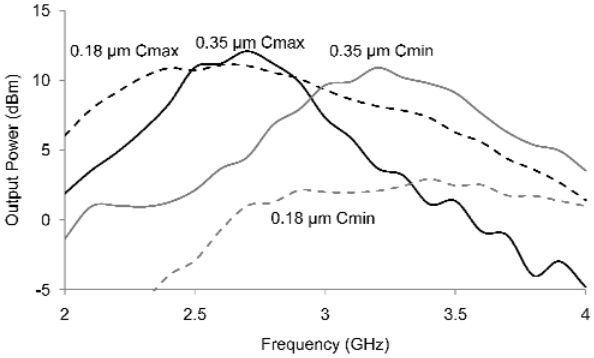

Fig. 8. Plot of power amplifier output power for both low and high frequency settings in the 0.18 and 0.35 µm PAs.

As with the LNA, the 0.35 µm design uses the first generation (2.5:1 tuning range) variable capacitor [9]. The

0.18 µm design uses the enhanced (7:1 tuning range) variable capacitor, and shows a wider tuning range than the 0.35 µm design. Measurements of the output power indicate that the 0.18 µm PA is frequency-reconfigurable from 2.6 GHz to 3.4 GHz, a tuning range of 27% of the center frequency (see Fig. 8 and Table 3). This measured tuning range and the output powers, and efficiency measures of the PA are degraded by the higher than expected shunt parasitic capacitances discussed earlier. A re-simulation of the PA with the measured S-parameters of the MEMS capacitor matches PA measurements confirming this effect.

Table 3. Measured power amplifier performance summary

Parameter	0.35 µm [7] (1st Gen. capacitor)		0.18 µm [This work] (2nd Gen. capacitor)	
Freq (GHz)	2.7	3.2	2.6	3.4
Pout (dBm)	13.7	10.1	11.9	1.2
Pin (dBm)*	7.0	4.8	3.3	1.3
DE (%)	21.7	10.6	9.1	1.4
PAE (%)	17.0	7.5	7.9	0.0
HD_2 (dBc)	-24.2	-20.0	-17	-30
HD_3 (dBc)	-51.6	-46.2	-37	-41

Other reconfigurable PAs in the literature [16] use discrete components and have power added efficiencies exceeding 60%. This is the first fully-integrated frequency reconfigurable power amplifier that the authors are aware of. The 0.35 µm design operated as an amplifier, but is an early design that had not yet been optimized to include layout parasitic adequately, adversely affecting drain efficiency and power-added efficiency. In the 0.18 µm design, focused-ion beam etching to fix the shunt parasitic capacitances on the MEMS variable capacitor is under way and measurement results, if available will be updated in the final paper.

A SEM image of the 0.18 µm chip showing the LNA and PA with their suspended inductors and MEMS variable capacitors is shown in Fig. 9. The chip also included a capacitor, an inductor, and MEMS release test structures.

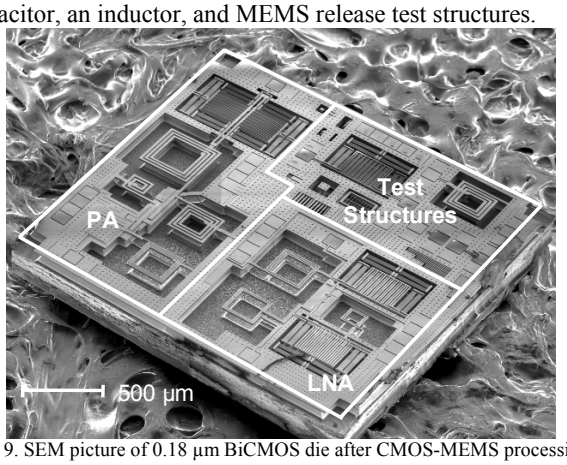

Fig. 9. SEM picture of 0.18 µm BiCMOS die after CMOS-MEMS processing

V. Conclusion

Fully-integrated frequency reconfigurable LNA and PA circuits in two foundry BiCMOS processes were demonstrated. The 0.35µm designs are based on an old CMOS-MEMS variable capacitor with limited tuning range. The 0.18µm designs uses a CMOS-MEMS variable capacitor with an improved tuning range of 7.1, with the potential of just ~10 fF shunt parasitic capacitance. The LNA has a better figure of merit than other reconfigurable LNAs and this is the first known fully integrated reconfigurable PA.

Acknowledgments

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