Test-Cost Reduction for 2.5D ICs Using Microspring Technology for Die Attachment and Rework

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***Abstract*—Interposer-based 2.5D integrated circuits (ICs) are being increasingly adopted in the semiconductor industry for FPGAs and GPUs. However, the cost of testing is still a major concern for 2.5D ICs because if a faulty die is detected after it is bonded to the interposer, the entire 2.5D assembly has to be discarded. We consider 2.5D integration based on the use of microsprings for attaching dies to the interposer. A key advantage of microsprings is that they allow the 2.5D assembly to be reworkable. If a faulty die is detected during post-bond testing, we can replace the faulty die with a fault-free one. In order to quantify the benefit of the reworkable 2.5D assembly, we present a test-flow selection method for 2.5D ICs with microsprings. We compare the test cost of microspring-based integration with a baseline of test flows for microbump-only integration, with respect to some key parameters such as pre-bond test cost, fault coverage of tests, and microspring cost. For a large number of dies and a relatively low die yield, microsprings provide significant benefits over the baseline.**

I. Introduction

A lot of effort has been devoted in recent years to bring through-silicon via (TSV)-based 2.5D IC technology to market [1], [2]. This technology has many benefits, such as lower power consumption, heterogeneous integration, and smaller form factor. Therefore, it is now being increasingly used in industry (e.g., FPGA from Xilinx and GPUs from AMD and Nvidia) as a technology platform [3]–[5].

Ensuring acceptable product quality is a major concern in 2.5D integration. In order to screen defects, a multi-stage test flow, including multiple test insertions, is often adopted [6], [7]. However, the testing of 2.5D ICs involves more steps than the testing of traditional 2D ICs, because there is a need for defect screening before die bonding, during die bonding, and after all dies are attached. Different test-related decisions at each step (i.e., no test, low-quality test or high-quality test) and the associated cost/yield trade-offs lead to a large space of possible test flows. Each test flow may result in a different test cost and test escape level [8], [9]. The problem of determining the most cost-efficient test flow is critical for test economics [10].

A number of cost models and cost-optimization methods have been proposed for 2.5D and 3D stacked ICs [7], [11]–[13]. These methods have focused on cost-model analysis [11], [12] and cost optimization [7], [13]. However, all of them are based on the assumption that dies are attached to the interposer using microbumps. In other words, the dies that are bonded to the interposer cannot be removed after assembly. As a result, if a faulty die is detected after bonding, it is impossible to replace it with a fault-free die, and the entire 2.5D assembly must be discarded.

In order to overcome this problem, microspring technology for die attachment was proposed in [14], [15]. With this technology, a die can be replaced (referred to as "reworked") after it is placed on the interposer (Fig. 1). As a result, if a faulty die is detected after assembly, it is easy to replace it. This integration flexibility has the potential to reduce test cost. For certain combinations of yield and cost of specific test steps, pre-bond test can be omitted and die rework utilized.

In this paper, we first present a test flow based on the judicious use of microspring technology. We minimize the test cost using a combination of a greedy algorithm and simulate annealing. We compare our test-flow results with a baseline of test flows for microbump-only integration. By varying some key parameters, such as the pre-bond test cost, fault coverage profile, and microspring cost, we are able to identify the range of parameter values for which microsprings provide significant benefits over test flows for microbump-only 2.5D assembly.

The remainder of this paper is organized as follows, Section II provides an introduction to microspring technology, and presents an motivational example. Section III formulates the test-cost minimization problem. Section IV presents the proposed cost-minimization method. Section V presents results on test-flow selection. Finally, Section VI concludes the paper.

II. Microspring Technology

A. Overview

Microsprings can be fabricated using standard wafer-scale thin films [14]. The fabrication process consists of three steps as shown in Fig. 2(a)-(c). First, a large balanced stress gradient (1 GPa/m) is applied to the spring metal. Because of the inherent stress gradient in the spring metal, when the underlying sacrificial layer is etched, the spring metal rises and protrudes from the surface. Next, a layer of overplated metal is coated on the surface of the spring metal to mechanically strengthen the spring and increase conductivity.

Typical materials used in this process are MoCr or Ni for the spring metal, and Cu, Ni alloys and gold for the overplate layer. The thicknesses of the spring layer and the overplate layer are typically 1-2 μm and 1-5 μm, respectively. The process is associated with low variability, because tip heights (the vertical distance that a spring rises above the substrate) vary by less than 5%, and yields of 99.99% have been demonstrated in PARC's research lab environment [14]. In addition, a

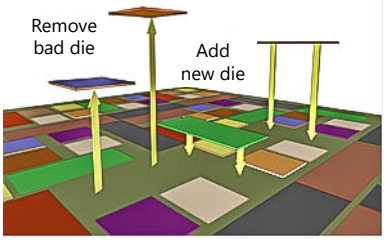

Fig. 1. An illustration of the reworkable 2.5D integration .

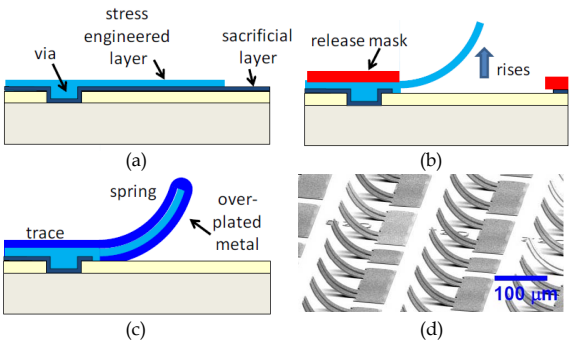

Fig. 2. Three steps in microspring fabrication: (a) applying stress on the spring metal, (b) spring metal rises because of the stress gradient, and (c) a layer of overplated metal is coated on the spring metal. (d) Microspring arrays fabricated on a ceramic substrate (adopted from [14]).

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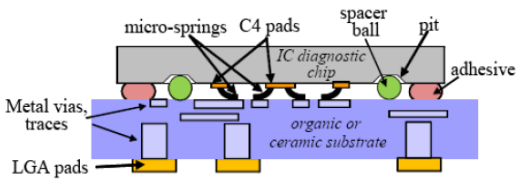

Fig. 3. A cross-sectional view of microspring-based integration (adapted from [14]).

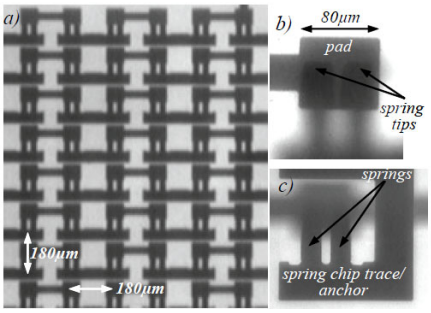

Fig. 4. (a) Top view of the package, (b) individual pad and (c) individual microspring [16].

very high density of microsprings can be achieved, because the films are thin and photolithography is used in the fabrication process. As shown in Fig. 2(d), 2D arrays of microsprings (180 μm $\times$ 180 μm in dimension) have been successfully fabricated.

Fig. 3 shows a cross-sectional view of microspring-based integration. The die and the interposer are connected by a physical contact between the protruding microsprings of the die and the metal pad of the interposer. The microsprings form a pressure contact with a gold metal pad on the other chip. The low force enables both testing, with mate and remate capability, as well as reliable contacts for packaging [14]. Adhesive is normally used to secure the chip, which can be applied as an underfill or only on the edges. To enable replacement of dies in final systems already in the field, where precise die handling equipment is not available, an integrated ball and pit structures can also be used, which enables micrometer alignment with human handling.

B. Reliability and Compatibility of Microsprings

In order to demonstrate the reliability of the microspring technology, rigorous testing of the microspring has been carried out. According to [16], a package that consists of 2844 micro-spring contacts was used in the tests. In this package, each metal pad is 80 μm $\times$ 80 μm in dimension, and the pads are arranged in a square array of 180 μm pitch. The details of the tests and the corresponding results are described below:

Connectivity test. A die with microsprings was placed on and then removed from the package 20 times to test the reliability of the microspring interconnect in a "re-workable" flow. There was no microspring deterioration, and no appreciable increase in resistance.

Temperature cycling test. The package was placed in an oven, and made to go through a thermal range of $0^{\circ}C$ and $100^{\circ}C$ within 10 minutes. All 2844 contacts continued to function for 1000 thermal cycles, and the resistance variation was less than 3%.

Humidity cycling test. The package was placed in a $85^{\circ}C/85\%$ RH oven, and it was baked at $100^{\circ}C$ to dry, and cooled to room temperature. This process was repeated for a total of 500 hours. All 2844 contacts continued to function, and the resistance variation was less than 5%.

High current soak test. The package was placed on a thermal stage of $65^{\circ}C$ to mimic the temperature of a fully operating processor. In addition, a current of 250 mA was passed through each spring contact for 196 hours. All 2844 contacts continued to function normally.

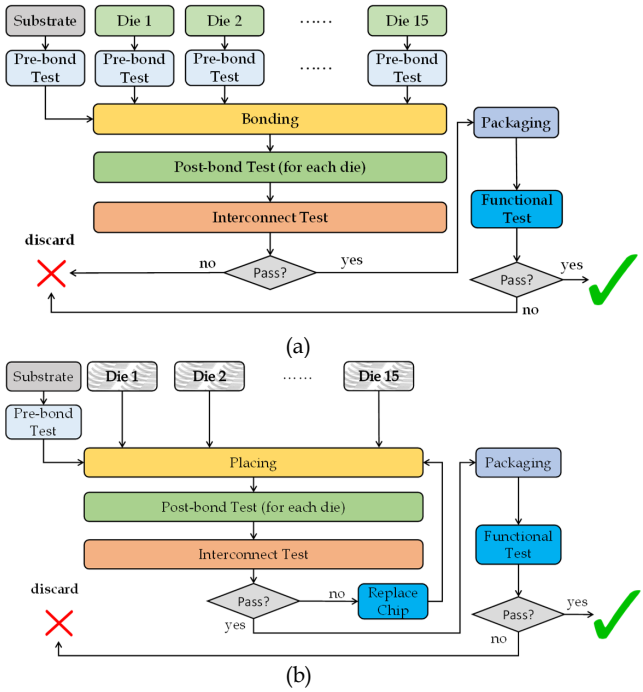

Fig. 5. Test flows for four dies with (a) microbump-based and (b) microspring-based 2.5D integration.

The integration solution based on microsprings is compatible with 2.5D IC fabrication flows. A microspring array at 180 μm pitch has been demonstrated, and the resistance of each spring is only 70 mΩ. The pitch of the microspring array and the resistance per microspring are slightly larger than that for commercially fabricated microbumps (45 μm and 30 mΩ, respectively [5]). Microspring arrays are scalable to even smaller pitches because their fabrication is based on lithographic patterning of thin films [17]; Moreover, the height of a microspring can be reduced to ensure lower resistance. Finally, dense linear arrays of microsprings at both 20 μm [18] and 6 μm [19] pitch have been assembled into flip-chip packages.

Microsprings can be a good substitute for microbumps for 2.5D IC integration because of similar spatial and electric characteristics.

C. Motivational Example

Fig. 5 illustrates test-insertion scenarios for 15 dies assembled on an interposer. All the test insertions can be viewed as options. The user can decide whether to apply a test, and these choices determine the test quality and yield/cost trade-offs.

In microbump-based integration, all 15 dies are mounted on the interposer using microbumps after (optional) pre-bond tests are carried out. Next, post-bond test for each die and an interconnect test step are potential test insertions. Finally, 2.5D IC packaging can be followed by functional testing of the entire 2.5D IC. If one of the test fails, the 2.5D IC is deemed to be defective and discarded.

In microspring-based integration, microsprings are fabricated on the interposer. If a die is detected to be faulty before the packaging step, we can replace (rework) the faulty die with a fault-free one, and the 2.5D IC can pass qualification instead of being discarded, which can significantly increase yield and reduce cost. Because of this "re-workable" feature, pre-bond tests for dies are less important (and can often be avoided) in microspring-based integration.

Next, we use a simple example to highlight the benefits of microspring-based integration. Without loss of generality, we make the following assumptions: (i) three types of dies (5 dies per type) are assembled on the interposer (namely Type A, Type B and Type C),

and the fabrication cost of a die of Type A, Type B and Type C are \$10 (80% yield), \$15 (80% yield) and \$20 (80% yield), respectively; (ii) pre-bond tests with 80% fault coverage are inserted for microbump-based assembly at the cost of \$2 per die, and post-bond tests with 99% fault coverage are inserted at the cost of \$1 per die; (iii) the cost of the substrate is \$10 (90% yield) and the pre-bond test cost for the interposer is \$2 (90% fault coverage); (iv) the microspring cost on the interposer is \$1 per die.

For a pre-bond, post-bond and interconnection test, suppose the incoming yield is Y_{in} and the fault coverage of the test is FC, then the outgoing yield Y_{out} (i.e., the probability that a die passes the test) is defined as [20]: $Y_{out} = Y_{in}/Y_{in}^{1-FC} = Y_{in}^{FC}$. The test escape TE is defined as: $TE = 1 - Y_{in}^{1-FC}$.

In the test flow for microbump-based integration, suppose all 15 dies and the interposer undergo pre-bond test, and then all dies are mounted on the interposer. At this stage, the equivalent cost (EC_1) for the entire assembly is given by:

$$EC_1 = \frac{\$10+\$2}{0.8^{0.8}} \times 5 + \frac{\$15+\$2}{0.8^{0.8}} \times 5 + \frac{\$20+\$2}{0.8^{0.8}} \times 5 + \frac{\$10+\$2}{0.9^{0.9}} = \$318.01 \quad (1)$$

After dies are mounted on an interposer, post-bond tests with 99% fault coverage are applied to each mounted die. At this stage, the equivalent cost (EC_2) for the entire assembly is given by:

$$EC_2 = \frac{EC_1 + \$1 \times 15}{(0.8^{0.99}/0.8^{0.80})^{5\times3}} = \$629.10 \quad (2)$$

Finally, interconnect test is applied to fully test the interposer (100% fault coverage). At this stage, the equivalent cost and test escape for the entire assembly are given by:

$$EC_3 = \frac{EC_2 + \$1}{0.9^{1.00}/0.9^{0.9}} = \$636.77$$
$$TE_3 = 1 - 0.8^{(0.01\times5\times3)} = 0.032 \quad (3)$$

Therefore, the overall test cost (OCT) for microbump-based integration is: $OCT_{mb} = EC_3 \times (1 + \alpha \times TE_3) = \$840.53$, where α is the penalty factor for test escape. According to [20], if a faulty chip is not detected at the die level, it would take about 10 times the cost to detect the faulty chip at the board level. Therefore, we set the value of α to 10.

On the other hand, in the test flow for microspring-based integration, only the interposer undergoes pre-bond test, and the equivalent cost for the interposer with microsprings is:

$$EC_{sub} = \frac{\$10 + \$1 \times 15 + \$2}{0.9^{0.9}} = \$29.68 \quad (4)$$

After that, dies are placed on the interposer and are subjected to post-bond tests. The equivalent cost for all dies is:

$$EC_{die} = \frac{\$10+\$1}{0.8^{0.99}} \times 5 \times 3 = \$205.79 \quad (5)$$

Finally, interconnect test is applied to fully test the interposer. The equivalent cost and test escape for the entire assembly is given by:

$$EC_{all} = \frac{EC_{sub} + EC_{die} + \$1}{0.9^{1.00}/0.9^{0.9}} = \$238.97$$
$$TE_{all} = 1 - 0.8^{(0.01\times5\times3)} = 0.032 \quad (6)$$

Therefore, the overall test cost (OCT) for microspring-based integration is: $OCT_{ms} = EC_{all} \times (1+\alpha \times TE_{all}) = \$315.44$. The test flow for microspring-based integration offers a 63% test-cost reduction compared to microbump-based integration. Note that HBM dies have a lane repair feature [21], and can therefore be repaired post-bond. However, the microspring and the reflow process can allow the IC designer to to be more "aggressive" with respect to the performance. Therefore, in this work, the post-bond self-repair feature is not considered.

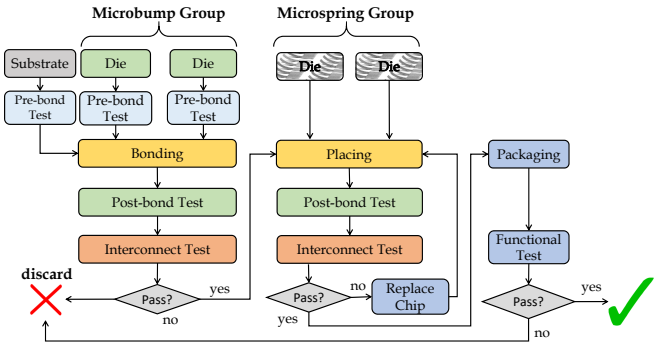

Fig. 6. A more generalized test flow that includes both microbump-based and microspring-based 2.5D integration.

III. Problem Formulation

In Section II, we assumed that all dies are connected to an interposer with microsprings. However, in reality, the fabrication of microsprings will introduce additional cost. Therefore, fabricating all dies with microsprings might not ensure minimum test cost. For example, if a die has high yield (e.g., 99%) and is associated with low fabrication cost, then it might not need microsprings because it is unlikely to need rework and microsprings will add to the cost. Therefore, in this section, we propose a more general and realistic test flow in which both microbumps and microsprings are used for 2.5D integration.

As shown in Fig. 6, each die is assigned either to a microbump group or to a microspring group. Dies in the microbump group are mounted on the interposer using microbumps while dies in the microspring group are placed on the interposer using microsprings. In this test flow, there are three test-flow stages: the microbump group testing stage, the microspring group testing stage, and the final functional testing stage. Note that test escape is also considered in the calculation of the cost of each potential test flow.

Based on the above description, we now consider the following problem formulation.

Input: (1) Relevant information about dies (e.g., fabrication cost, yield and quantity); (2) Test-cost profiles (i.e., the relationship between test cost and fault coverage) of pre-bond and post-bond tests for each die; (3) Spring fabrication cost, die bonding cost (for microbump) and die placement cost (for microspring).

Output: An optimized test flow for a combination of microbump-based and microspring-based 2.5D integration as shown in Fig. 6. Each die should be assigned to either a bonding group or a spring group. The fault coverage and test cost of each pre-bond test and post-bond test should be determined.

Objective: Minimize the overall test cost (OTC) of the test flow:

$$OTC = EC \times (1 + \alpha \times TE) \quad (7)$$

where EC is the equivalent cost per "fault-free" 2.5D IC (might be faulty but not detected by any of the inserted tests), TE is the test escape of the 2.5D IC, and α is the penalty factor for test escape.

IV. Proposed Cost-Minimization Method

Since all test insertions in the proposed test flow are viewed as options (decision points), the total number of potential test flows is extremely large, as analyzed in [7]. Therefore, we develop an efficient search method that can quickly provide a low-cost test flow. The proposed method involves a combination of a greedy algorithm and simulated annealing. First, simulated annealing is used to assign each die to either a microbump group or a microspring group. Next, for a particular group assignment, a greedy algorithm is used to search and obtain the target test flow with minimum overall test cost (OTC). Finally, we compare

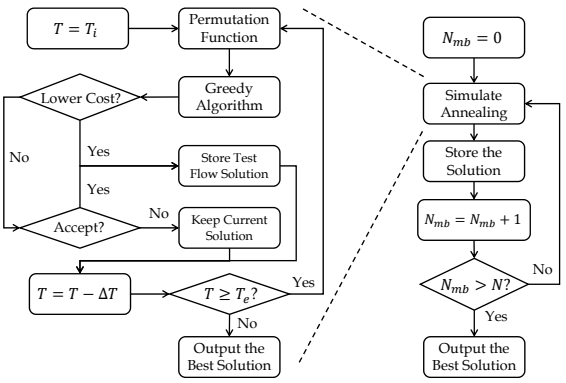

Fig. 7. The overall flow of the proposed cost-minimization method.

the minimum OTCs from different group assignments and select the test flow with the minimum OTC.

A. Overall Optimization Flow

The overall flow of the cost-minimization method is shown in Fig. 7. It has two loops: an outer loop (on the right) and an inner loop (on the left). Suppose the total number of dies is N. In the outer loop, we first vary the size of the microbump group N_{mb} from 0 to N, and the size of the spring group is thus $N - N_{mb}$. In each outer loop, a test flow with the minimum OTC with respect to the value of N_{mb} is generated. Finally, a total of N candidate test flows are generated, and the test flow with the minimum OTC is selected.

In simulated annealing, we first set the initial and ending temperature to user-defined values T_i and T_e, respectively. Next, for each inner loop, a permutation function is used to randomly switch the position of two dies. For example, if Die A is in the microbump group and Die B is in the microspring group, then, after the permutation function, Die A will be in the microspring group and Die B will be in the microbump group. After we obtain the new group assignment, a greedy algorithm is used to find out the test flow with the minimum OTC with respect to the new group assignment.

Next, we examine if the newly obtained OTC is the smallest so far. If it is the case, the corresponding group assignment is stored, and the next permutation function is considered based on this group assignment. Otherwise, an "Accept" function is used to determine whether we need to store the new group assignment. If the temperature T is high, there is a higher probability to "accept" and store the new group assignment. Otherwise, it is more likely that the algorithm will discard this group assignment. The "Accept" function reduces the chances of a local minima.

B. Greedy Algorithm for the Microbump Group

We next execute a greedy algorithms separately on the microbump group testing stage and the microspring group testing stage. We divide the computation into three phases. In Phase 1, N_{mb} dies and an interposer first go through pre-bond testing. Next, N_{mb} dies are mounted on the interposer, and the equivalent cost, namely EC_1, is given by:

$$EC_1 = \frac{C_{sub} + C_{ms} + C_{pre}(sub)}{Y_{pre\cdot out}(sub)} + \sum_{i=1}^{N_{mb}} \left(\frac{C_{die}(i) + C_{pre}(i)}{Y_{pre\cdot out}(i)} + C_{bon} \right) \tag{8}$$

where C_{sub} is the fabrication cost of the interposer, C_{ms} is the fabrication cost of microsprings on the interposer, $C_{die}(i)$ is the fabrication cost of die i, $Y_{pre\cdot out}(sub)$ is the yield of the interposer for pre-bond testing, $Y_{pre\cdot out}(i)$ is the yield of die i for pre-bond testing, C_{bon} is the bonding cost for each die, $C_{pre}(sub)$ is the cost of the pre-bond test for the interposer and $C_{pre}(i)$ is the cost of the pre-bond test for die i.

In Phase 2, all the mounted dies go through post-bond testing. Because pre-bond testing tends to be more expensive than post-bond testing [22], the fault coverage of a post-bond test is assumed to be higher than that for pre-bond testing. Suppose that the fault coverage of pre-bond testing is a subset of that for post-bond testing, then the yield of post-bond testing for die i after pre-bond testing can be expressed as $Y_{pos\cdot out}(i)/Y_{pre\cdot out}(i)$, where $Y_{pos\cdot out}(i)$ is the yield of post-bond testing for die i if no pre-bond testing is applied. The yield of all post-bond testing for dies that are mounted on the interposer (i.e., the probability that all mounted dies pass post-bond tests) is given by: $Y_{pos} = \prod_{i=1}^{N_{mb}} Y_{pos\cdot out}(i)/Y_{pre\cdot out}(i)$.

Therefore, the equivalent cost for Phase 2 can be expressed as:

$$EC_2 = \left(EC_1 + \sum_{i=1}^{N_{bon}} C_{pos}(i) \right) / Y_{pos} \tag{9}$$

where $C_{pos}(i)$ is the cost of post-bond testing for die i.

In Phase 3, all dies are subjected to interconnect testing to examine the connectivity between each die and the interposer. The fault coverage is assumed to be 100%, therefore, the yield of an interconnect test is equal to the bonding yield for die i, i.e., $Y_{int\cdot out}(i) = Y_{bon}(i)$. The yield of all interconnect testing for all mounted dies is given by:

$$Y_{int} = \prod_{i=1}^{N_{mb}} Y_{int\cdot out}(i) = \prod_{i=1}^{N_{mb}} Y_{bon}(i) \tag{10}$$

The equivalent cost for Phase 3 is given by:

$$EC_3 = (EC_2 + \sum_{i=1}^{N_{mb}} C_{int}(i))/Y_{int} \tag{11}$$

where $C_{int}(i)$ is the cost of interconnect testing for die i.

Finally, the test escape for Phase 3, namely TE_3 is given by:

$$TE_3 = 1 - (1 - TE_{pre}(sub)) \times \prod_{i=1}^{N_{mb}} [(1 - TE_{pos}(i)) \times (1 - TE_{int}(i))] \tag{12}$$

where $TE_{pos}(i)$ is the test escape of post-bond testing for die i, $TE_{int}(i)$ is the test escape of interconnect testing for die i, and $TE_{pre}(sub)$ is the test escape of pre-bond testing for the interposer.

In the greedy algorithm, we assume that identical dies are subjected to the same pre-bond and post-bond tests. Under this constraint, the greedy algorithm performs a search over every possible combination of pre-bond, post-bond, and interconnect tests, and calculates the overall test cost for Phase 3, namely OCT_3, as follows:

$$OTC_3 = EC_3 \times (1 + \alpha \times TE_3) \tag{13}$$

where α is the test escape penalty factor.

Finally, the test insertions for the microbump group testing stage are determined by minimizing OTC_3.

C. Greedy Algorithm for the Microspring Group

Next, we discuss the microspring group testing stage. In this stage, if a die is detected to be faulty, it will be replaced with a new die, and we also assume that the newly replaced die can be faulty. We divide the computation into three phases (4-6). In Phase 4, T_{ms} types of dies are placed on an interposer, and the equivalent cost for dies associated with type j ($1 \leq j \leq T_{ms}$) is given by:

$$\Delta EC_4(j) = \sum_{i \in \mathbb{S}(j)} (C_{die}(i) + C_{pla}) \tag{14}$$

where $C_{die}(i)$ is the fabrication cost of die i, C_{pla} is the placement cost for a die, and $\mathbb{S}(j)$ is the set of dies of type j.

In Phase 5, all placed dies are subjected to post-bond testing, and the yield of post-bond testing for dies of type j (i.e., the probability that all dies of type j pass post-bond tests) is given by: $Y_{pos}(j) = \sum_{i \in \mathbb{S}(j)} Y_{pos \cdot out}(i)$, where $Y_{pos \cdot out}(i)$ is the yield of post-bond testing for die i.

Therefore, the equivalent cost for Phase 5 can be expressed as:

$$\Delta EC_5(j) = \left(\Delta EC_4(j) + \sum_{i \in \mathbb{S}(j)} C_{pos}(i) \right) / Y_{pos}(j) \tag{15}$$

where $C_{pos}(j)$ is the cost of post-bond testing for a die i.

In Phase 6, all dies are subjected to interconnect testing. The fault coverage is assumed to be 100%, therefore, the yield for the interconnect test is equal to the placement yield for Die i, i.e., $Y_{int \cdot out}(i) = Y_{pla}(i)$. The yield of all interconnect testing for all placed dies of type j is given by:

$$Y_{int}(j) = \prod_{i \in \mathbb{S}(j)} Y_{int \cdot out}(i) = \prod_{i \in \mathbb{S}(j)} Y_{pla}(i) \tag{16}$$

The equivalent cost for dies of type j in Phase 6 is given by:

$$\Delta EC_6(j) = \left(\Delta EC_5(j) + \sum_{i \in \mathbb{S}(j)} C_{int}(i) \right) / Y_{int}(j) \tag{17}$$

where $C_{int}(i)$ is the cost of the interconnect test for die i.

Finally, the test escape for dies of type j in Phase 6, namely $TE_6(j)$, is given by:

$$TE_6(j) = 1 - \prod_{i \in \mathbb{S}(j)} (1 - TE_{pos}(i)) \times (1 - TE_{int}(i)) \tag{18}$$

where $TE_{pos}(i)$ is the test escape of post-bond testing for die i, $TE_{int}(i)$ is the test escape of interconnect testing for die i.

Here, we again assume that identical dies are subjected to the same post-bond tests. Under this constraint, the greedy algorithm performs a search over every possible combination of post-bond and interconnect tests, and calculate the overall test cost for dies of type j in Phase 6, namely OCT_6, as follows:

$$\Delta OTC_6(j) = \Delta EC_6(j) \times (1 + \alpha \times TE_6(j)) \tag{19}$$

where α is the test escape penalty factor.

Finally, the test insertions for the microspring group testing stage are determine by minimizing $\Delta OTC_6(j)$ for all value of j. The equivalent test cost OTC for the entire test flow is:

$$\begin{aligned} OTC = (EC_3 + \sum_{j=1}^{T_{ms}} EC_6(j) + C_{int}(sub) + C_{pkg} + C_{func}) \\ \times (1 + \alpha \times (1 - TE_3) \times \prod_{j=1}^{T_{ms}} (1 - TE_6(j))) \end{aligned} \tag{20}$$

where C_{pkg} is the packaging cost and C_{func} is the functional test cost, T_{ms} is the number of die types in the microspring group, $C_{int}(sub)$ is the cost of interconnect test for the interposer.

V. Experimental Results

In the forseeable future, as described in [23], besides HBM memory dies, many different kinds of dies will be reused and integrated in a 2.5D IC. In order to investigate the benefits introduced by the microspring technology, we suppose that three types of dies (i.e., Type A, Type B and Type C) are assembled on the interposer, and the number of dies of each type are 4, 4 and 2, respectively. The cost of post-bond test is set to 1/3 of that of pre-bond test. The default parameter values are listed in Table I.

TABLE I
Default Parameter Values for Test-Flow Selection.

Parameter	Normalized Value	Parameter	Value
Cost of an interposer	1	Yield of an interposer	80%
Cost of a die (A,B,C)	(2,1,2)	Yield of a die (A,B,C)	(90%,95%,95%)
Cost of microsprings per die	0.05	Yield of microsprings	100%
Cost of microbumps per die	0.00	Yield of microbumps	100%
Cost of bonding/placement per die	0.01	Yield of bonding/placement	99%
Cost of packaging	1	High fault-coverage pre-bond test cost for a die (A,B,C)	(0.5, 0.2, 0.5)
Cost of functional test	1	High fault-coverage post-bond test cost for an interposer	0.5
Number of dies (A,B,C)	(4,4,2)	Number of interposer	1

We also consider three fault coverage profiles in our experiments. A fault coverage profile captures the relationship between normalized test cost and fault coverage (Fig. 8).

In Profile 1 (the blue curve), we can achieve high fault coverage with low cost; this profile models a high-volume and low-complexity digital die. In Profile 2 (the red curve), the test cost is higher; it models a more complex digital die. Finally, in Profile 3, extremely high test cost is needed to achieve the same fault coverage level, and the highest fault coverage is limited to 90%. This profile is indicative for an analog or mixed-signal die.

With the above default parameters and fault-coverage profiles, we are able to calculate the overall test cost (OCT) of the test flow for microbump-only, microspring-only and generalized 2.5D integration (a judicious mix of the two). In order to quantify the benefits introduced by microspring technology, we define two indicators:

$$CR_1 = TC_{mb}/TC_{ms}, CR_2 = TC_{mb}/TC_{mb+ms} \tag{21}$$

where TC_{mb} (TC_{ms}) is the cost of the test flow for microbump-only (microspring-only) integration, and TC_{mb+ms} is the cost of the test flow for generalized integration. The value of CR_1 (CR_2) quantifies the reduction in test cost due to the use of microsprings. Larger cost ratios are clearly desirable. For example, if CR_1 is 10, the test cost for the microspring-only integration is 10 times less than that for microbump-only integration.

In order to identify the scenarios for which microspring-only and generalized integration can achieve significant benefits over microbump-only integration, we scale the: (1) number of dies; (2) yield of each die; (3) microspring cost; (4) pre-bond test cost for full fault coverage; (5) interposer cost; and (6) interposer yield. We obtain the results shown in Fig. 9. Here, "scale" means that we multiply the value by the scaling factor, e.g., if the scaling factor for number of dies is 2, then the quantity of dies is (8, 8, 4) instead of (4, 4, 2). Note that in Fig. 9, "P1", "P2" and "P3" denote the three fault-coverage profiles. Because CR_2 values are very close to CR_1 values, we only show CR_1 in Fig. 9.

From the results, we draw the following key conclusions:

- The number of dies and the die yield have considerable impact on test-cost reduction. From Fig. 9(a) and Fig. 9(b), we see that, with a larger number of dies and lower die yield, the value of both CR_1 can be as high as 13 for Profile 3.
- The fault coverage profiles also have major impact on the results. For high test cost (i.e., Profile 3), the benefit is significant. For low test cost (i.e., Profile 1), the benefit is less, but still evident.
- The cost ratio does not vary much with microspring cost, interposer cost and interposer yield.

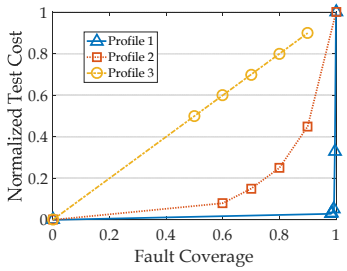

Fig. 8. Illustration of three fault-coverage profiles.

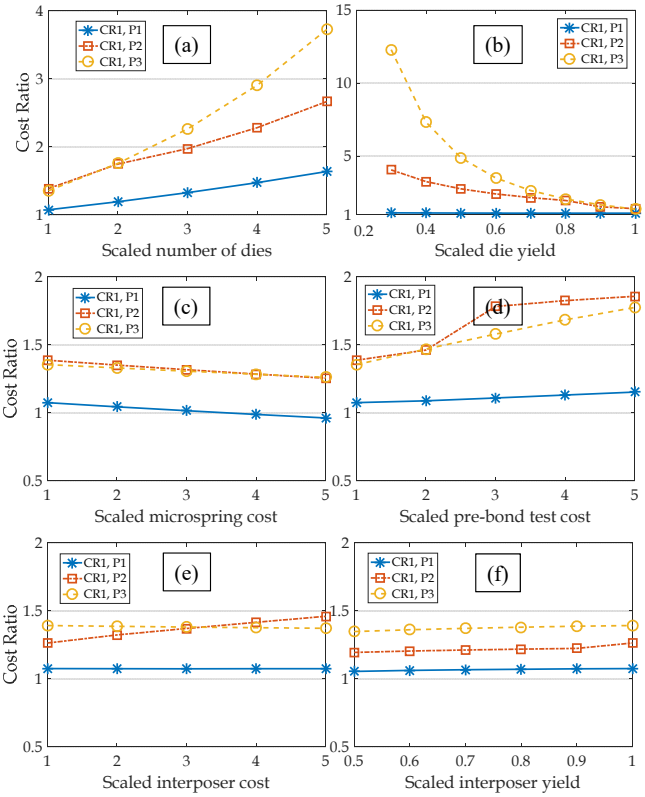

Fig. 9. The benefit of using microsprings for different scenarios.

Table II shows examples of test-flow selection results. When the normalized microspring cost is 0.2 per die, the yield of dies of type C is 99%, and the second fault coverage profile is used, the test-flow selection is denoted by "✓" (**S-1**). If we scale up the pre-bond and post-bond test by a factor of 2, the new test-flow selection is denoted by "✗" (**S-2**).

The OCT for the microbump-only, microspring-only and generalized test flow are (31.2, 29.4, 28.6) for **S-1** and (36.15, 34.15, 32.67) for **S-2**. The time to obtain the selected test flow are 0.17 s (microbump-only), 0.83 s (microspring-only) and 201 s (generalized) on a Core i5 3.0 GHz CPU with 16 GB memory (the memory usage is about 10 MB). The four dies of Type B are assigned to the microbump group because they have lower fabrication cost and higher yield. Using microsprings for these dies will result in higher overall cost. Each selected test flow in Table II includes interconnect test. Note that for **S-2**, lower fault-coverage tests are selected for dies due to relatively higher test cost.

VI. Conclusion

We have presented a test-flow selection method for 2.5D ICs with microsprings. The key advantage of the microspring is that it allows the 2.5D assembly to be "reworkable". Experimental results show that: for a 2.5D IC with a large number of dies or low yield dies, the test cost for the microspring-based integration reduced significantly. In future work, we will study the role of microsprings in reducing test cost through rework after functional testing.

TABLE II
Examples of Test-Flow Selection for Generalized Test Flow.

Group	Component Type	Pre-bond Test				Post-bond Test			
		70%	80%	90%	∼100%	70%	80%	90%	∼100%
N/A	Interposer				✗✓				
Microbump Group	B (Die 1)		✗	✓					✗✓
	B (Die 2)		✗	✓					✗✓
	B (Die 3)		✗	✓					✗✓
	B (Die 4)		✗	✓					✗✓
Microspring Group	A (Die 5)	Skip							✗✓
	A (Die 6)	Skip							✗✓
	A (Die 7)	Skip							✗✓
	A (Die 8)	Skip							✗✓
	C (Die 9)	Skip					✗	✓	
	C (Die 10)	Skip					✗	✓	

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