High Performance UTBB FDSOI Devices Featuring 20nm Gate Length for 14nm Node and Beyond

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Abstract

We report, for the first time, high performance Ultra-thin Body and Box (UTBB) FDSOI devices with a gate length (L_G) of 20nm and BOX thickness (T_{BOX}) of 25nm, featuring dual channel FETs (Si channel NFET and compressively strained SiGe channel PFET). Competitive effective current (I_{eff}) reaches 630µA/µm and 670µA/µm for NFET and PFET, respectively, at off current (I_{off}) of 100nA/µm and V_{dd} of 0.9V. Excellent electrostatics is obtained, demonstrating the scalability of these devices to14nm and beyond. Very low A_{Vt} (1.3mV•µm) of channel SiGe (cSiGe) PFET devices is reported for the first time. BTI was improved >20% vs a comparable bulk device and evidence of continued scalability beyond 14nm is provided.

Introduction

The UTBB FDSOI device is a key enabler for continued aggressive CMOS scaling at 28nm node and beyond. [1-4] Its advantages include superior short channel control, small V_t variation, flexible & dynamic multi-V_t options [4], a simplified planar manufacturing process, and ease of porting designs from existing conventional bulk technologies. It was recently reported that a 28nm FDSOI ARM-based chip operated at record fast 3GHz [5]. By incorporating strain into the channel and optimizing the RSD epitaxy and junction design, high-performing 2nd generation UTBB devices were developed which enable continued scaling to 14nm and beyond.

Experimental

A simplified UTBB integration flow is shown in Fig. 1. The PFET cSiGe channel used in this study was formed by epitaxy & condensation before STI formation. [6, 7] A thin SiN liner was deposited inside trench cavity to isolate the following epitaxial S/D structure from the substrate. After high-k/metal gate formation, a dual in-situ doped RSD process was applied to form NFET and PFET, respectively. Here, the NFET RSD is in-situ Phosphorus doped (ISPD) SiC, and the PFET RSD is in-situ Boron doped (ISBD) SiGe. Both doping levels are >5E20cm^{-3} to achieve low external resistance (R_{ext}). A combination of laser annealing & thermal treatment was applied to fully activate the dopants and minimize R_{ext}. Conventional MOL and BEOL process steps completed the device fabrication. Fig. 2 shows the final NFET and PFET devices featuring a channel thickness (T_{Si}) of 6nm, a BOX thickness (T_{BOX}) of 25nm, and 20nm gate lengths (L_G).

Device Characteristics

Fig. 3 shows the drive current (I_{on}) as a function of off current (I_{off}), with V_{dd}=0.9V. Here, the PFET cSiGe has a Ge content of 25%. NFET/PFET I_{on} of 1120/1220µA/µm, respectively, at I_{off}=100nA/µm are achieved. The effective current (I_{eff}), as a function of I_{off}, is shown in Fig. 4. At V_{dd}=0.9V, NFET/PFET I_{eff} reach 630/670µA/µm at I_{off}=100nA/µm, respectively. They are the best performing FDSOI CMOS devices reported so far, featuring non-strained Si channel NFET and strained SiGe channel PFET.

At a nominal L_G of 20nm, the transfer (I_D/V_G) characteristic is shown in Fig. 5. A DIBL = 80/100mV and SS=90/110mV/dec for NFET/PFET, respectively, are obtained. The R_{on} as a function of 1/DIBL is shown in Fig. 7. Low R_{on} was achieved through a combination of optimized in-situ doped RSD epitaxy, contact resistance reduction, and additionally for the PFET, a strained cSiGe channel. The extrapolated R_{ext} reaches 190/140 Ω•µm for NFET/PFET, respectively. Fig. 7 shows the I_D/V_G curves at V_{dd}=0.75V. A DIBL = 73/85mV, and SS = 90/97mV/dec for NFET/PFET, respectively, are achieved. The I_{on}/I_{off} and I_{eff}/I_{off}, as a function of back bias from -2V to 2V, are shown in Figs. 8 and 9. The cSiGe PFET sensitivity to back bias is shown here for the first time. With a back gate doping level at ~1E18cm^{-3}, the body factor is ~60/70

mV/V for NFET/PFET. The difference is mainly from the inversion gate dielectric (T_{inv}) delta between NFET and PFET, with PFET T_{inv} slightly thicker. Additionally, no performance degradation is seen with back bias, demonstrating the feasibility of multi-Vt and the dynamic power management capability of UTBB FDSOI.

Table I shows the benchmark of device characteristics of this work and state-of-the-art bulk FinFET devices. FDSOI NFET drive current and effective current are comparable to FinFET NFET, while FDSOI PFET outperforms FinFET PFET by ~10%, at V_{dd} of both 0.75 and 0.8V. Thanks to a much shorter gate length at 20nm vs 30nm in FinFET devices, and a planar device architecture, the total capacitance of FDSOI is estimated to be 20% lower than that of FinFET, which is critical to faster operation and lower power consumption.

Due to enhanced band-to-band tunneling resulting from a narrower bandgap, the cSiGe PFET GIDL was found to be higher than that of Si based PFET. Fig. 10 shows the I_D/V_G curve of cSiGe PFET with back bias. The GIDL is improved with increasing positive (reverse) back bias leading to increased V_t. GIDL is reduced from 0.5nA/μm to 0.2nA/μm when applying V_{bb} from -2V to 2V. A similar phenomenon was also reported previously in Si channel NFET devices with reverse back bias [4], due to the reduction of peak electric field at the drain side under negative bias. Excellent UTBB FDSOI cSiGe PFET A_{Vt} at 1.3mV•μm is shown for the first time in Fig. 11, evidence of well-controlled SiGe epitaxy and condensation processes used to form the undoped channel. By varying the amount of Ge in the cSiGe, different V_ts are obtained as shown in Fig. 12. The higher the Ge content, the lower the V_t. V_t is reduced approximately 10mV with 1% higher Ge in cSiGe channel. However, if not optimized with an anneal, elevated Dit may appear at these higher Ge levels, as indicated by the kink at lower V_G for the non-annealed case. Hole mobility was also measured as a function of Ge level in cSiGe as shown in Fig. 13, where 30% higher mobility was measured at 25%-Ge vs 15%-Ge, due to the higher channel strain. Further improvement was limited at 35%-Ge due to increasing Dit, unless annealed. With the anneal, the Dit is cured and the mobility is further improved by another 25% with 35%-Ge cSiGe.

Reliability

Bias temperature instability (BTI) and breakdown voltage (VBD) tests based on voltage ramp stress [10] were performed. A 20mV step was applied starting from 1V, with a stress time of 100ms and sense time of 10ms. The BTI value is given as the gate voltage needed to shift V_t by 50mV. Fig. 14 shows BTI of both UTBB NFET and PFET as a function of T_{inv} vs a comparable 20nm bulk device. [11] The UTBB NFET/PFET BTI is improved 33%/20% where T_{inv} is 20%/12% thinner, respectively. Fig. 15 shows VBD as a function of T_{oxgl}, where T_{oxgl} is the equivalent oxide thickness at the same gate leakage. Versus comparable 20nm bulk devices, UTBB NFET VBD improves 11% at 24% thinner T_{oxgl}, while PFET VBD degrades 12% at 28% thinner T_{oxgl}, which has generally a linear correlation to VBD. UTBB devices show superior reliability to bulk devices. This improvement is attributed to the un-doped channel, and the lower electric fields for the UTBB devices.

Further Scaling

Scaling to 10nm node and below will likely require further L_G reduction. To maintain electrostatic performance, a thinner channel thickness (T_{Si}) will also be needed as indicated in Fig. 16, which shows TCAD simulations of DIBL & short channel V_t vs. T_{Si} at 20nm L_G. Thinner T_{Si} also results in lower C_{ov}, as shown experimentally in Fig. 17. It is believed to be due to lower inner fringe capacitance. However, at very thin T_{Si} (< 3nm), quantum confinement starts to dominate V_t. Fortunately, UTBB devices have another scaling enabler: T_{BOX}. Fig. 18 shows DIBL & SS as a function of T_{BOX}. A DIBL reduction of 20mV is seen when scaling T_{BOX} from 25nm to 10nm, while SS remains well controlled.

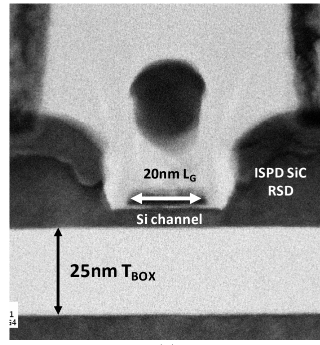
Finally, scaling also requires further performance improvement. It was demonstrated that, by incorporating more strain into the channel, such as tensile strained-SOI NFET [6] and higher Ge cSiGe PFET, higher Ge SiGe RSD, and combining with layout optimization [7], which utilizes striped widths to achieve uni-axial strain in channel and higher current, DC performance can be improved efficiently (Fig. 19). Lower gate height, more faceted RSD and low K spacer, etc., are effective enablers to reduce parasitic capacitances and improve AC performance.

Conclusions

In this paper, we reported high performance UTBB FDSOI devices with L_G at 20nm. Competitive drive current and excellent electrostatics are achieved. Very low cSiGe PFET A_{Vt} is presented for the first time. It is also demonstrated that BTI and VBD reliability are superior to bulk devices. UTBB FDSOI is planar and capable for 14nm & beyond.

- cSiGe formation at PFET area
- STI RIE and liner deposition
- STI fill and CMP
- Ground plane (GP) implantation and annealing
- High-k / metal gate patterning
- SiN spacer deposition
- NFET spacer formation and ISPD SiC RSD EPI
- Hard mask deposition
- PFET spacer formation and ISBD SiGe RSD EPI
- 2nd spacer formation
- Rapid thermal annealing (RTA) + laser annealing
- Salicide
- MOL and BEOL

Fig. 1 A simplified UTBB FDSOI integration flow, featuring cSiGe PFET, gate first high-k / metal gate and dual in-situ doped raised source/drain epitaxy process.



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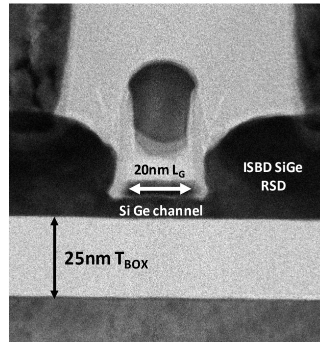
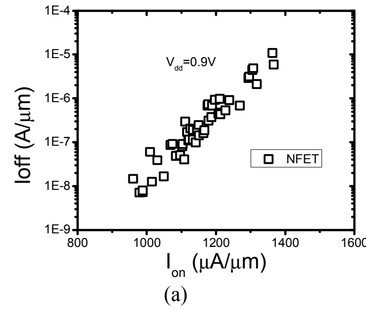


(b)

Fig. 2 TEM cross-section of (a) NFET with Si channel and in-situ P doped (ISPD) SiC RSD and (b) PFET with SiGe channel and ISBD SiGe RSD, with gate length of 20nm and Box thickness of 25nm.



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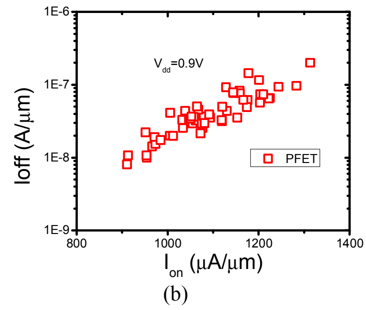
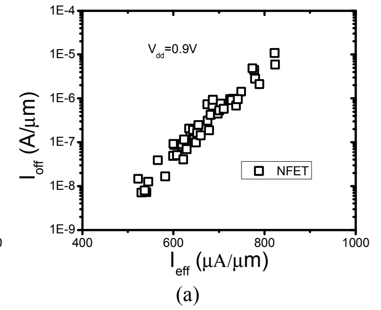


(b)

Fig. 3 I_{on}/I_{off} of (a) NFET with Si channel and (b) PFET with 25% cSiGe strained channel at V_{dd}=0.9V. At I_{off} of 100nA/μm, the drive current reaches 1120μA/μm and 1220μA/μm for NFET and PFET, respectively.



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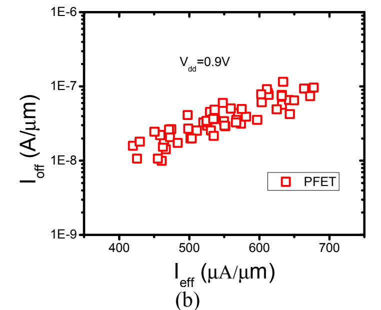


(b)

Fig. 4 At V_{dd}=0.9V, and an off current of 100nA/μ m, (a) NFET effective current is 630μA/μm, while (b) PFET effective current reaches 670μA/μm. The slope of PFET I_{eff}/I_{off} differs from NFET, due to the strain in the cSiGe channel.

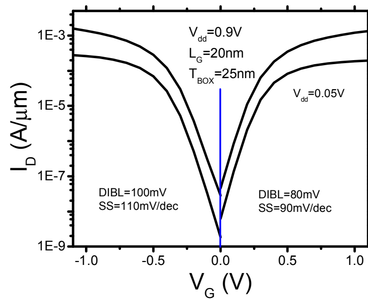
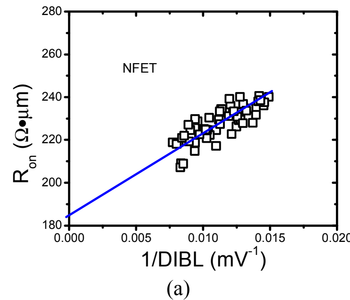


Fig. 5 I_D/V_G curves of N/PFET with gate length at 20nm, showing good SCE control.



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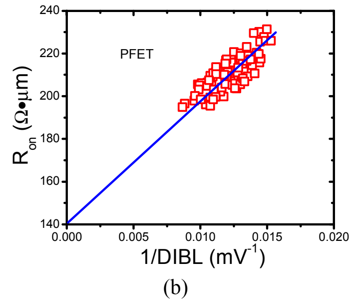


(b)

Fig. 6 The R_{on} vs. 1/DIBL of (a) NFET and (b) PFET. The extrapolated R_{ext} is as low as 190/140 Ω•μm for NFET/PFET, respectively.

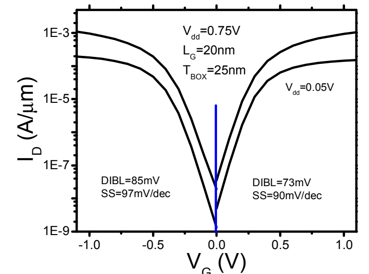
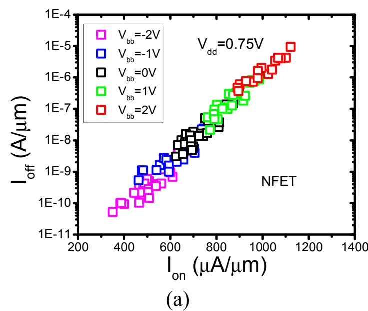


Fig. 7 I_D/V_G curves of N/PFET with L_G at 20nm, and V_{dd} at 0.75V, again, showing excellent electrostatics



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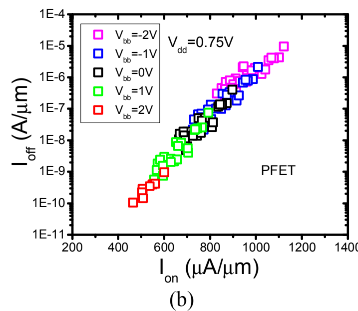

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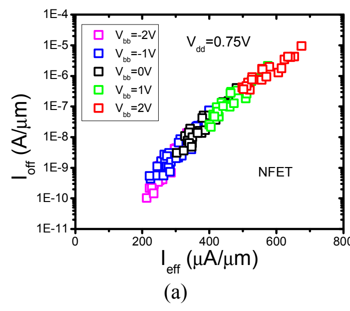
Fig 8 I_{on}/I_{off} of (a) NFET and (b) PFET, at V_{dd}=0.75V, with back bias from -2V to 2V.



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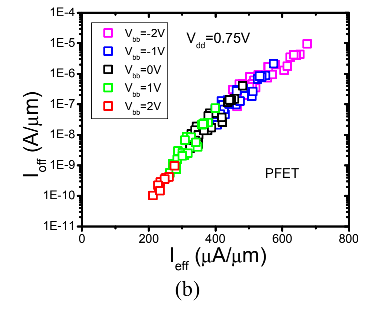

(b)

Fig 9 I_{eff}/I_{off} of (a) NFET and (b) PFET, at V_{dd}=0.75V, with back bias, showing the body factor is 60/70 mV/V.

Table 1 Comparison of the devices in this work with state-of-art 22nm Bulk FinFET devices. The drive current is normalized to the effective device channel width. At much shorter gate length, FDSOI shows competitive performance.

	Auth et al [8]	Jan et al [9]	This work		
CGP (nm)	90	90	100		
L_G (nm)	30	30	20		
V_{dd} (V)	**0.8**	**0.75**	**0.75**	**0.8**	**0.9**
N/P DIBL (mV/V)	46/50	30/35	73/85	78/90	80/100
N/P SS (mV/dec)	69/72	71/72	90/97	90/101	90/110
I_{off} (nA/μm)	100	100	100	100	100
N/P I_{on} (mA/μm)	1.02/0.9	0.88/0.74	0.86/0.82	0.99/0.98	1.12/1.22
N/P I_{eff} (mA/μm)	0.53/0.46		0.47/0.45	0.51/0.53	0.63/0.67

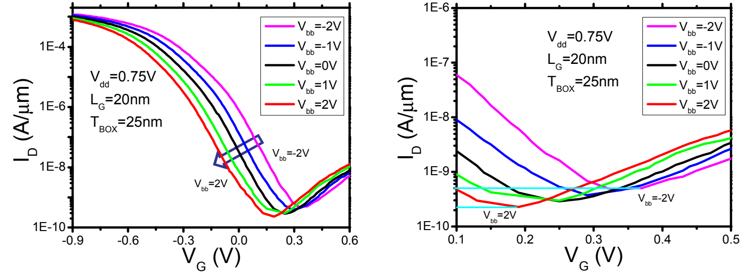

Fig. 10 I_D/V_G of PFET with back bias from -2V to 2V, at V_{dd}=0.75V, showing GIDL floor improvement by positive bias. A zoom in view at the GIDL floor is shown on the right. GIDL floor improves from 0.5nA/μm to 0.2nA/ μm when applying V_{bb} from -2V to 2V.

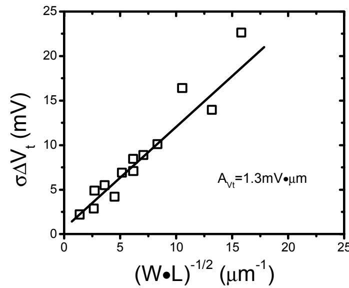

Fig. 11 Excellent A_{Vt} of 1.3mV•μm is obtained with cSiGe PFET pair transistors, showing well controlled processes.

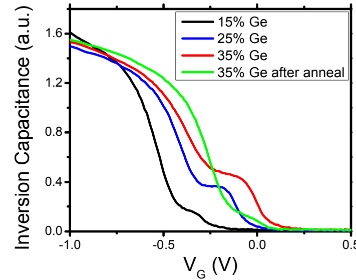

Fig. 12 Long channel C/V measurements showing V_t shift from Ge content. A kink shows up at low V_G, showing effect of Dit, which was eliminated by the anneal.

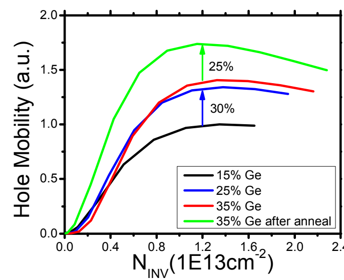

Fig. 13 Hole mobility increases by 30% from 15%-Ge channel to 25%-Ge channel. The anneal improves the mobility by 25% on cSiGe PFET with 35% -Ge.

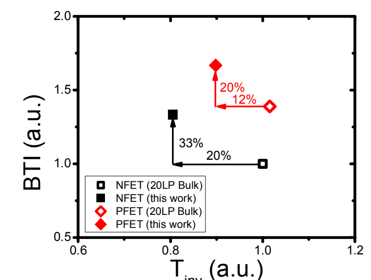

Fig. 14 FDSOI BTI shows superior capability compared with 20nm bulk devices. Even with thinner T_{inv}, the BTI improves on both NFET and PFET.

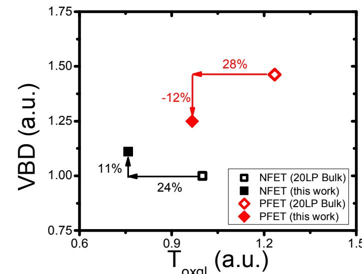

Fig. 15 FDSOI VBD is better than that of 20nm bulk devices, by taking account of T_{oxgl} difference, thanks to un-doped channel, and lower electric field.

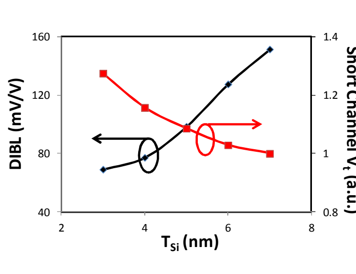

Fig. 16 TCAD simulations show that by thinning T_{Si}, DIBL improves, while the short channel V_t (normalized) increases.

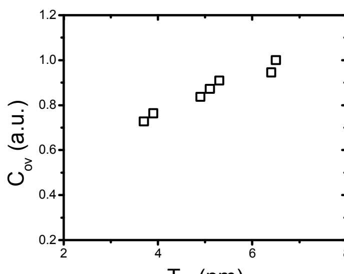

Fig. 17 Experimental data shows that C_{ov} decreases with thinner T_{Si}, which may relate to the inner fringe capacitance reduction.

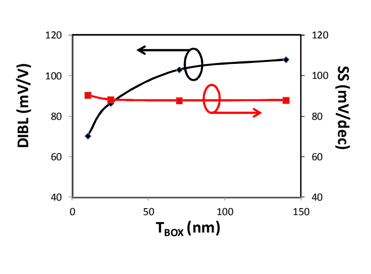

Fig. 18 TCAD simulations show that by thinning T_{BOX}, DIBL is improved while SS remains well controlled. Here, L_G=20nm and T_{inv}=10A.

Table 2 cSiGe strain/stress as a function of Ge content on FDSOI

Ge	Bi-axial strain (%)	Bi-axial stress (GPa)
15%	-0.6	-1.09
25%	-1.03	-1.76
35%	-1.44	-2.4

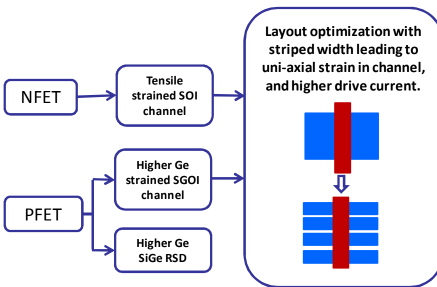

Fig. 19 To further improve FDSOI NFET and PFET performance to meet next generation requirement, different strain elements and layout optimization can be applied.

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References

[1] Q. Liu, *et al*, *VLSI*, p.61, 2010.
[2] O. Weber, *et al*, *IEDM*, p.58, 2010.
[3] O. Faynot, *et al*, *IEDM*, p.50, 2010.
[4] Q. Liu, *et al*, *VLSI*, p.160, 2011.
[5] Press release, *EETimes*, Feb. 2013
[6] A. Khakifirooz, *et al*, *VLSI*, p.117, 2012.
[7] K. Cheng, *et al*, *IEDM*, p.419, 2012
[8] C. Auth, *et al*, *VLSI*, p.131, 2012
[9] C.-H. Jan, *et al*, *IEDM*, p.44, 2012
[10] A.Kerber, *et al*, *EDL*, p.1347, 2009
[11] H. Shang, *et al*, *VLSI* p.129, 2012