20.2 A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping

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One of the main applications of System-in-a-Package (SiP) is a high-performance and yet power-aware system such as HDTV on a portable device. H.264/AVC for 1080HDTV requires 23.1Gb/s data bandwidth between microprocessors and memories. The data link should consume as low as 0.4pJ/b energy in order to keep the total power dissipation below 10mW. But conventional technologies consume much larger energy: 1.6pJ/b in a micro-bump technology [1] and 2.8pJ/b in an inductive-coupling transceiver [2]. This paper reports energy reduction in an inductive-coupling transceiver from 2.8pJ/b to 0.14pJ/b without degrading the data rate. The energy dissipation is the lowest published to date and far lower than [1-16] (Fig. 20.2.1). Precise pulse shaping reduces the transmitter's energy by 1/20, while device scaling lowers the receiver's energy by 1/20.

The shape of the transmit pulse is illustrated in Fig. 20.2.2. The transmitter's energy dissipation, E_{TX}, is determined by the transmit pulse shape and given by, $E_{TX}=V_{DD}I_P\tau$, where I_P is a pulse amplitude and 2τ is a pulse width. A received pulse signal, V_R, is induced by MdI_T/dt, and the amplitude is given by $V_P=2MI_P/\tau$. When the communication distance and the inductor size are given (i.e. M is given), a pulse slew rate, $S_P=I_P/\tau$, is determined by the Bit-Error Rate (BER) requirement. By reducing τ while keeping the slew rate, E_{TX} is reduced by τ^2, as $E_{TX}=V_{DD}S_P\tau^2$ indicates. On the other hand, since a receiver (latch comparator [2]) is a digital CMOS circuit, the receiver's energy dissipation, E_{RX}, is given by $E_{RX}=CV_{DD}^2$, and it is effectively reduced by device scaling.

Figure 20.2.2 depicts the pulse shaping circuit that consists of pulse width, pulse slew rate and pulse amplitude controls. In the pulse width control, a 4-phase clock generator provides 0°, 45°, 90°, 180° clocks to two Phase Interpolators (PIs). The left PI interpolates a clock phase between 90° and 180° by 1/256-UI (4ps) step. The right PI is a dummy circuit that always outputs 0° clock. A succeeding AND gate generates a pulse clock that determines the pulse width, τ. The pulse slew rate is digitally controlled by variable capacitors. The pulse amplitude is digitally controlled by changing channel width of the NMOS in the H-bridge driver.

Since the receiver's timing margin is reduced by reducing the pulse width, an accurate timing design is necessary to maintain the BER<10^{-12}. A clock transceiver is modified to reduce the timing jitter in the received clock, $Rxclk$. The timing jitter caused by supply noise and temperature variations can be effectively rejected as common-mode noise by the clock link that is located adjacent to the data link. A sampling timing control adjusts the timing by 4ps step to overcome timing shift due to process variations.

Figure 20.2.3 shows two sets of stacked test chips. One is fabricated in 0.18μm CMOS where the transceiver with the pulse shaping circuit is implemented. Energy reduction in the data transmitter is evaluated in the same process employed in [2]. The other is fabricated in 90nm CMOS to measure energy reduction in the data receiver due to device scaling. In both 0.18μm and 90nm CMOS, a 10μm-thick transmitter chip is stacked on top of a receiver chip and the communication distance including an adhesive layer is 15μm. The data transceiver communicates at 1Gb/s by a 30μm diameter metal inductor. A clock transceiver in the 0.18μm CMOS chip provides 1GHz clock link by a 200μm diameter metal inductor. The communication distance and inductor size are the same as [2].

Timing jitter in the clock transceiver is reduced to receive the narrow pulse correctly. The clock transceiver and simulated waveforms are depicted in Fig. 20.2.4(a). A conventional clock transceiver in [2] transmits a sinusoidal clock whose low slew rate increases the timing jitter when the transmitter generates I_{TC} and the receiver latches $Rxclk$. On the other hand, the clock

transceiver here transmits a rectangular clock of higher slew rate to solve this problem. Figure 20.2.4(b) depicts measured timing jitter of the received clock. By increasing the slew rate, the timing jitter is reduced to 4.8ps$_{rms}$ at minimum. It is half of the timing jitter of the conventional clock transceiver.

Figure 20.2.5(a) presents measured timing bathtub curve dependence on the pulse amplitude. The minimum pulse amplitude required for a BER<10^{-12} is seen to be 60mV. Figure 20.2.5(b) presents the bathtub curve dependence on the pulse width. It is confirmed that E_{TX} is reduced by τ^2. When τ is set to the minimum pulse width of 60ps, E_{TX} is reduced by 1/17 (0.13pJ/b) and the timing margin for a BER<10^{-12} is 25ps.

Figure 20.2.6 shows the measured BER dependence on supply noise. Since the clock link is located adjacent to the data link, timing jitter caused by supply noise is effectively rejected and suppressed within the timing margin of 25ps. Therefore, the data transceiver exhibits sufficiently high tolerance against a supply noise of 350mV. It is much larger than the 69mV supply noise monitored in a product-level microprocessor for 3G cellular phones [17]. Chip performance in both 0.18μm and 90nm CMOS is summarized in Fig. 20.2.7.

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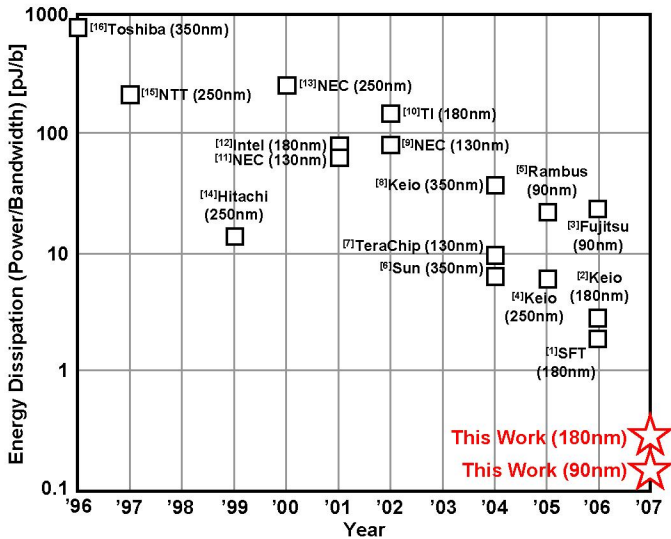
Figure 20.2.1: Energy dissipation of CMOS links presented at ISSCC.
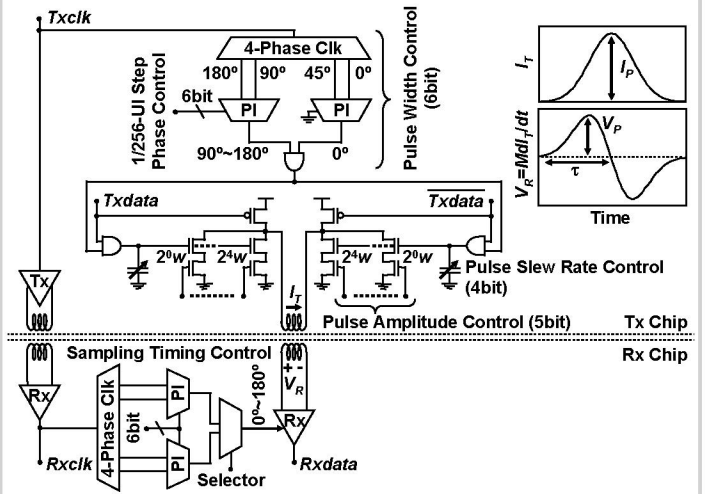

Figure 20.2.2: Inductive-coupling inter-chip data transceiver with digital control of pulse shaping.
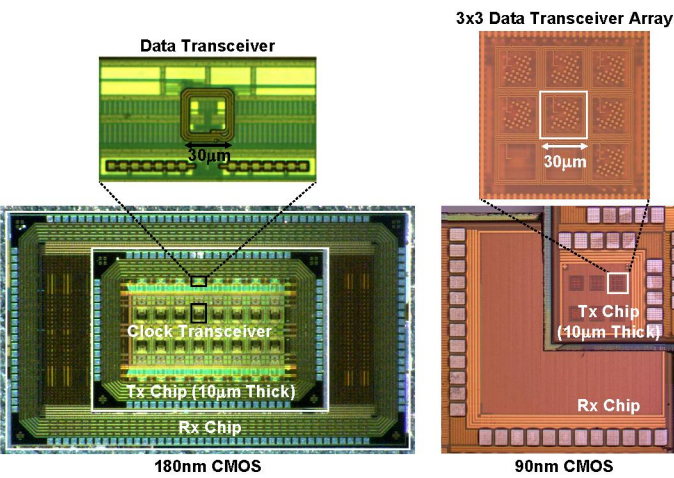

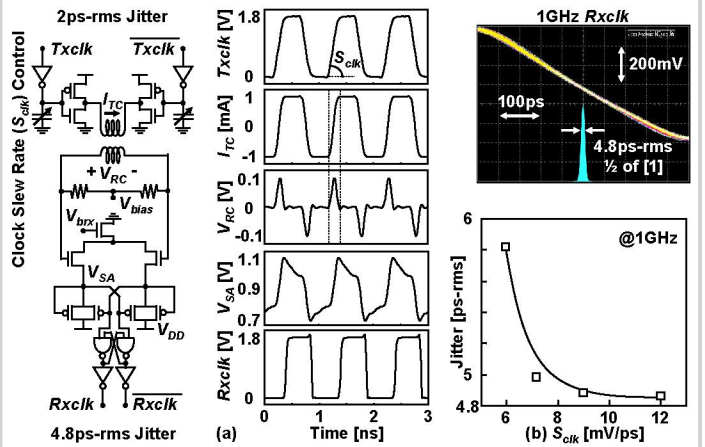Figure 20.2.3: Micrographs of stacked test chips in 180nm and 90nm CMOS.

Figure 20.2.4:(a) Inductive-coupling clock transceiver, simulated waveforms and (b) measured jitter of received clock.
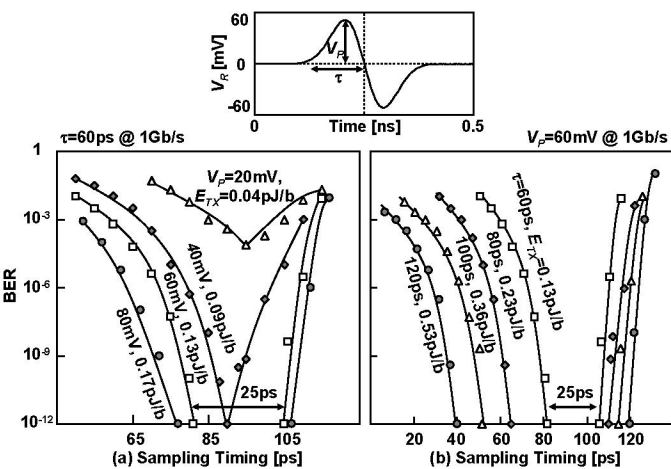

Figure 20.2.5: Measured timing bathtub curves dependence on (a) pulse amplitude and (b) pulse width.
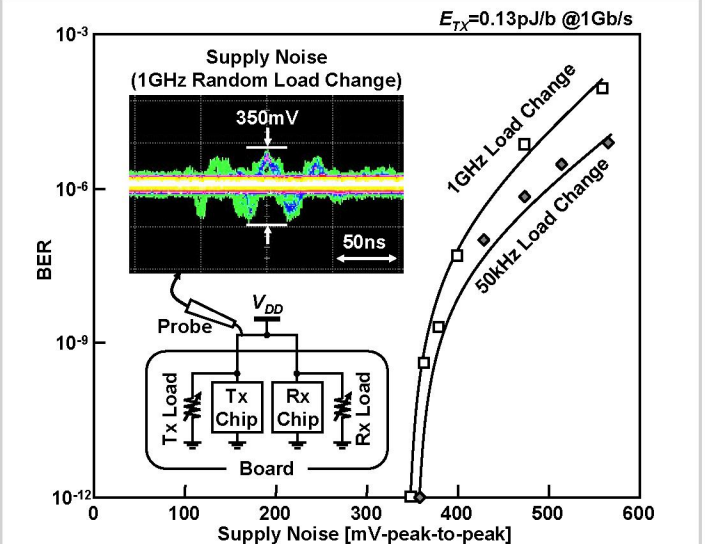

Figure 20.2.6: Measured BER dependence on supply noise.

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	This Work		[2] Previous Work
Energy Dissipation in Data Link	0.14pJ/b (Tx:0.11pJ/b, Rx:0.03pJ/b)	0.33pJ/b (Tx:0.13pJ/b, Rx:0.2pJ/b)	2.8pJ/b (Tx:2.2pJ/b, Rx:0.6pJ/b)
Energy Dissipation in Clock Link	No Data	3.5pJ/b (Tx:1.5pJ/b, Rx:2pJ/b)	12.5pJ/b (Tx:6.5pJ/b, Rx:6pJ/b)
Jitter in Clock Link	No Data	4.8ps-rms	9.5ps-rms
Process	90nm CMOS (V_{DD}=1V)	180nm CMOS (V_{DD}=1.8V)	
Data Rate	1Gb/s		
Bit Error Rate	$<10^{-12}$		
Clock Rate	1GHz		
Channel Area	30μm x 30μm		
Distance	15μm (Chip Thickness:10μm, Adhesive Thickness:5μm)		

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Figure 20.2.7: Performance summary.