28.6 A ±50mV Linear-Input-Range VCO-Based Neural-Recording Front-End with Digital Nonlinearity Correction

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Neural signal recordings have been an essential tool for understanding the brain and driving the progress in neuroscience research and therapy. The local field potential (LFP) signals, which span from 3Hz to about 200Hz, serve as indicators of various neurological behaviors and disorders. Prior integrated LFP recording front-ends are designed for a small-signal input of a few mV, limiting the dynamic range to <60 dB [1-3]. For closed-loop neuromodulation, featuring *simultaneous* neural recording and stimulation, it is important to observe and understand brain dynamics *during* stimulation. Stimulation artifacts can range between 10 and 100mV and last for several milliseconds. The stimulation patterns result in significant artifact power inside the LFP band that cannot be filtered using conventional techniques. To adaptively reject stimulation artifacts in the digital domain, it is desired to capture the neural signal combined with the artifact with a high linearity. This requirement pushes the front-end dynamic range requirement to about 80dB for ±50mV input range, 20dB beyond the capabilities of current integrated recording front-ends.

For such a high dynamic range requirement, traditional design of an instrumentation amplifier (IA) followed by an ADC faces several design challenges. The IA needs to limit the gain to 20dB to avoid saturation, which would increase the input-referred noise. The ADC also needs >14b resolution to achieve the required 80dB dynamic range, which typically leads to high power consumption unacceptable for integrated biomedical implants. On the other hand, a VCO-based front-end avoids the tradeoff between gain and input range by relying on voltage-to-phase conversion for digitizing the input [4]. The VCO-ADC has a high voltage-to-phase gain but does not saturate because there is no physical bound on the maximum phase that a signal can have. In addition, the inherent anti-aliasing that the VCO-ADC offers allows us to directly digitize the input signal.

Despite these advantages, the dynamic range of the VCO-based front-end is limited by the VCO nonlinearity. Several approaches have been reported to overcome this limitation. For instance, the VCO can be embedded in a higher-order delta-sigma loop [5] requiring an active integrator. This approach, however, has a high power consumption due to power consumed by the integrator. Alternately, the VCO could be used as a fine quantizer in a two-stage ADC [6]. The kT/C noise from the sampling operation in such an ADC calls for 1nF of capacitance to meet the noise requirements. In contrast, a digital calibration/correction implementation for VCO nonlinearity is attractive as it does not add to front-end structure complexity. It is also amenable for the implanted neural recording application since the front-end works under a well-regulated voltage and slow and limited temperature variation, rendering the VCO nonlinearity time-invariant and input-independent.

This work presents an integrated VCO-based LFP recording front-end (Fig. 28.6.1) that achieves a linear input range of ±50mV. The input neural signal is first sensed by a VCO, and then the corresponding phase/frequency information is captured in the digital quantizer. To suppress the distortions due to VCO nonlinearity, the quantized signal is finally processed by a NLC block.

The VCO (Fig. 28.6.2) consists of a differential pair to convert the input voltage to a differential current and the diff-pair branches are connected to two 29-stage ring oscillators. In order to be able to correct the nonlinearity, the diff-pair needs to remain unclipped under large input. Thus it is designed with an overdrive voltage of ~80mV. It is also important to reduce the flicker noise as it is the dominant noise contributor for this application. Flicker noise reduction is achieved by sizing up the differential pair devices, increasing the number of stages in the ring, and by sizing the inverters for symmetric rise and fall times. To further reduce flicker noise and mismatch due to the oscillators, a chopping scheme is used in which a commutating switch between the diff-pair and the oscillator runs at the sampling frequency, resulting in two phases Sp and Sn in one sampling period. The digital quantizer then subtracts the phase information recorded in these two phases to remove the oscillator-induced flicker noise.

To remove the DC offset a high-pass filter (HPF) is inserted between the electrode inputs and the diff pair. For capturing low-theta neural oscillations, the corner frequency needs to be <1Hz. A passive HPF with such a low corner requires a GΩ resistor and an nF capacitor, which requires a large silicon area. Such filters have been built with pseudo resistors in literature. However, pseudo resistors are susceptible to voltage drops due to leakage currents and are not well controlled. Our HPF uses a high-density MOM cap and a duty-cycled passive resistor. The switch connecting the duty-cycled resistor R to a bias voltage is controlled by a clock (swclk) with a low duty cycle (D). The charge / discharge transient via the resistor is thus duty-cycled, resulting in a higher average resistance R_{eq}=R/D. The switching clock frequency is higher than twice the LFP band to avoid aliasing inherent in the switching circuit, and low enough so that the parasitic capacitor of the switch and the resistor do not degrade the filter corner. The noise of the switching-resistor HPF is equal to that of a passive filter with the same capacitor and resistor R_{eq}. Thus the HPF noise, rolling off at 20dB/dec beyond the corner, is small at frequencies of interest.

The digital quantizer needs to record both the VCO cycle number and phase information for the high dynamic range requirement. This is accomplished by the phase decoder and the counter. The CountEn signal latches the VCO phase information at its rising/falling edges as InitialPh/FinalPh. To avoid an MSB error at the counter side due to metastability, the InitialPh information at the phase decoder output is used in a multiplexer to choose one out of the 29-stage VCO outputs as the counter input. The enable signal CountEn_MSB of the counter is a delayed version of the CountEn signal to account for the phase-decoder and multiplexer delay. The phase and cycle information are combined and then sampled by SampleClk for each chopping phase. The samples at two phases are then subtracted to invert the chopping discussed earlier.

The NLC block takes the quantizer output clocked by the PISOEn signal and implements a feedforward polynomial fitting algorithm to invert the VCO nonlinearity. After matching, the VCO nonlinearity is limited by the 3rd- and 5th-order terms, which demands a 5th-order polynomial fitting. The Horner's method for iterative polynomial computation is used because it requires only one single-precision multiply-accumulate (MAC) unit. When the quantizer output is ready, the input enable signal is asserted to feed the quantizer output to the NLC engine. After six iterations, each requiring 99 sysclk cycles, the output valid signal is asserted and the output data is retrieved.

The VCO-based LFP front-end is fabricated in a 40nm CMOS technology. The chip (Fig. 28.6.7) has 4 VCO cores each occupying a 0.1mm^2 area. The NLC, the VCO controller, and the SPI interface for the 4 cores are placed and routed in a much larger area than needed to simplify interfacing with the VCO cores. The effective DSP area is <0.13mm^2. The in-vitro recorded LFP signal is shown in Fig. 28.6.3. The SFDR of the front-end is >80dB for low-frequency input and 79dB for high-frequency input. The output spectra (Fig. 28.6.4) for an interferer of ±50mV and a signal of ±10mV demonstrate that the NLC suppresses the intermodulation terms to <1μV. The SNDR, DNL and INL are plotted in Fig. 28.6.5. The integrated noise from 3 to 200Hz (LFP band of interest) is 6μV_{rms}. Each VCO front-end takes 3μW from a 1.2V analog supply, and 4μW switching power from the digital supply. The leakage power is excessive as the chip is fabricated in the GP process, it is estimated ~1μW in the LP process. As shown in Fig. 28.6.6, the front-end delivers a 10× higher input range and a 20dB better dynamic range than prior art with comparable noise and power performance.

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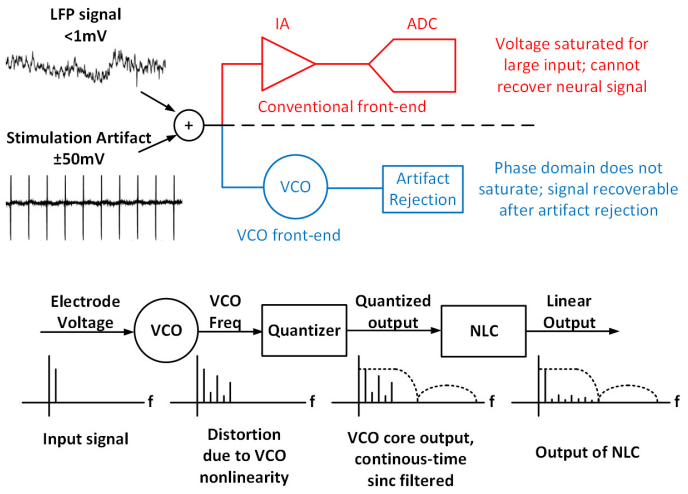

Figure 28.6.1: VCO-based front-end does not saturate with stimulation artifact (top) and the linearity can be restored by nonlinearity correction (bottom).

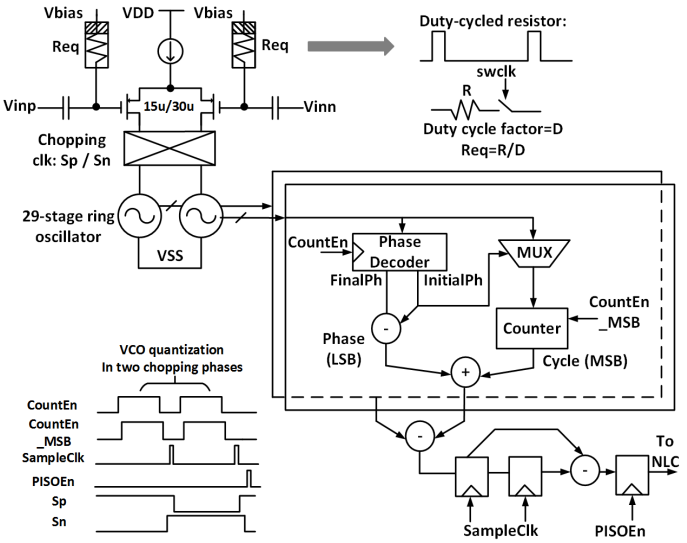

Figure 28.6.2: VCO core schematic and control timing diagram.

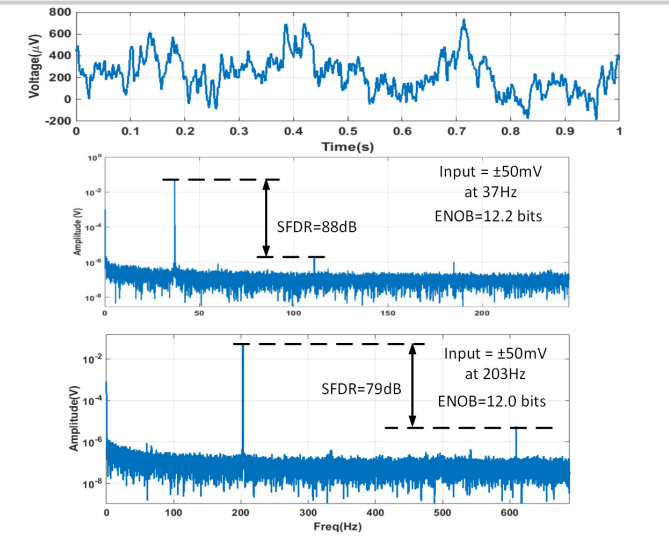

Figure 28.6.3: In-vitro recorded LFP signal (top) and front-end linearity measurement results (bottom two).

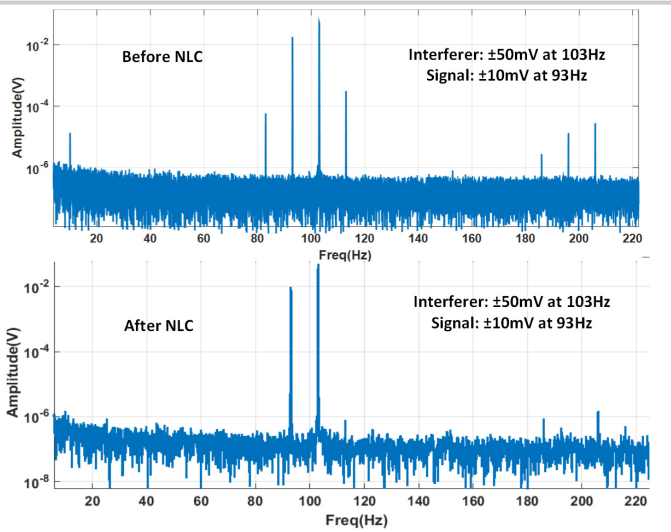

Figure 28.6.4: VCO front-end output with a large interferer and a signal, without NLC (top) and with NLC (bottom).

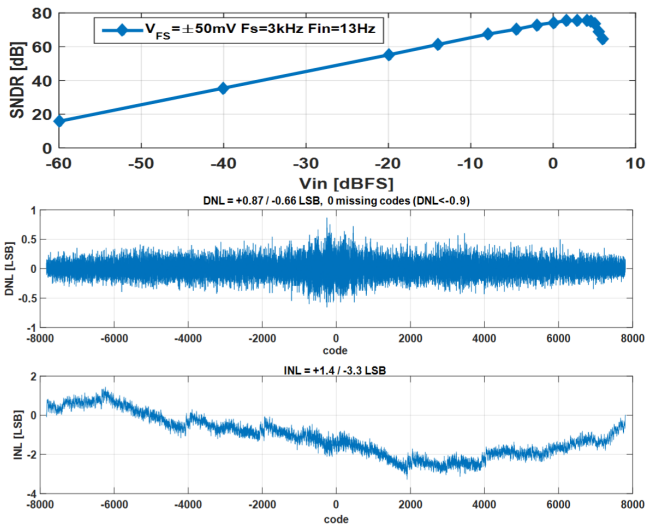

Figure 28.6.5: SNDR, DNL and INL plot of VCO Front-end. VCO Front-end 17b raw outputs truncate 3b LSB to 14b for DNL/INL plot.

	[1] JSSC 2007	[2] JSSC 2012	[3] ISSCC 2014	This work
Topology	CCIA (no ADC)	Diff Amp + ADC	Chopper Amplifier + ADC	Direct digitization of VCO with nonlinearity correction
Power/ch	2uW	5.04uW	2.3uW	3uW(Analog) 4uW(Digital switching)
Supply	1.8V	0.5V	0.5V	1.2V(Analog) 0.45V (Digital)
Signals	LFP	Spike/LFP	LFP	LFP
Peak Input	5mVp	3.5mV	±0.5mV	±50mV
Input-referred Noise	1uV	4.3uV	1.3uV	6uV
SFDR	60dB	40dB	52dB	79dB
Zin	8MΩ	∞	28MΩ	∞
Area/ch	1.7 mm²	0.013 mm²	0.025 mm²	0.135 mm²
Technology	0.8um	65nm	65nm	40nm

Figure 28.6.6: Performance comparison with prior art.

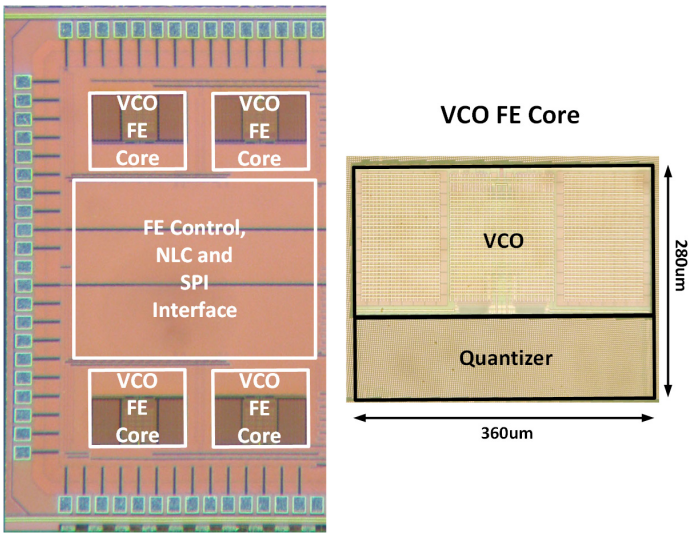

Figure 28.6.7: Die photo of the front-end.

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