Modeling and Simulation of Transistor and Circuit Variability and Reliability

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Abstract- **Statistical variability associated with discreteness of charge and granularity of matter is one of limiting factors for CMOS scaling and integration. The major MOSFET statistical variability sources and corresponding physical simulations are discussed in detail. Direct statistical parameter extraction approach is presented and the scalability of 6T and 8T SRAM of bulk CMOS technology is investigated. The standard statistical parameter generation approaches are benchmarked and newly developed parameter generation approach based on nonlinear power method is outlined.**

I. Introduction

The years of 'happy scaling' are over and the fundamental challenges that the semiconductor industry faces at technology and device level will deeply affect the design of the next generations of integrated circuits and systems. The progressive scaling of CMOS transistors to achieve faster devices and higher circuit density has fuelled the phenomenal success of the semiconductor industry – captured by Moore's famous law [1]. Silicon technology has entered the nano CMOS era with 35 nm gate length MOSFETs in mass production in the 45 nm technology generation. However, it is widely recognized that the increasing statistical variability in the device characteristics is among the major challenges to scaling and integration for the present and next generation of nano CMOS transistors and circuits [2], [3]. Variability of transistor characteristics already critically affects SRAM scaling [4], and introduces leakage and timing issues in digital logic circuits [5]. The variability is the main factor restricting the scaling of the supply voltage, which for the last four technology generations has remained virtually constant, adding to the looming power crisis.

Compact Model is a key component of interface between technology and design. The first step towards variability aware design is to develop statistical compact modeling approaches that can reliably capture statistical variability information, which will enable designer to confidently take full advantage of advanced technologies can offer. Historically, the importance of device matching property in analogue domain drove the statistical compact modeling efforts [6]. For a semiconductor technology that can have economic sense in analog domain, the device should have well controlled variance behaviors and as a result most of statistical compact model approaches developed for analog domain were rest upon the assumption for normal, uncorrelated distributions of the compact model parameters [7]. However, in digital domain, from the static functionality aspect, the CMOS logic circuit is very resistant to device variation [8]. Although statistical variation of device can cause major concerns in timing and power dissipation aspects of CMOS digital design, it still can tolerate relatively large SV compared with analog counterpart. Consequently, statistical compact modeling in digital domain needs to deal with large magnitude of SV inherent to devices at nanometer scale.

In this paper, we examine in detail how this statistical variability influences the device technology, scaling, circuit performance and compact modeling practices. In section II we review the major sources of statistical variability and corresponding physical simulation in nano CMOS transistors focusing at the 45nm technology generation and beyond. A direct statistical compact modeling strategy that can accurately transfer device variability information into industry standard compact models is outlined and its application on SRAM simulation is presented in section III. In section IV, commonly used statistical compact modeling approaches are benchmarked against direct extraction results discussed in section III. A newly developed parameter generation method that can maintain both the high moments of parameter distribution and the correlations between parameters is proposed in section V and the final conclusions are drawn in section VI.

II. Statistical Variation And Its Physical Simulation

A. Sources of Statistical Variability

The statistical variability in modern CMOS transistors is introduced by the inevitable discreteness of charge and matter, the atomic scale non-uniformity of the interfaces and the granularity of the materials used in the fabrication of integrated circuits. The granularity introduces significant variability when the characteristic size of the grains and irregularities become comparable to the transistor dimensions. For conventional bulk MOSFETs that are still the workhorse of the CMOS technology Random Discrete Dopants (RDD) are the main source of statistical variability [9]. RDD are introduced predominantly by ion implantation and redistribution during high temperature annealing. Fig.1 illustrates the dopant distribution obtained by the atomistic process simulator DADOS by Synopsys. Apart from special correlation in the dopant distribution imposed by the silicon crystal lattice, there may be also correlations introduced by the Coulomb interactions during the diffusion process. Line Edge Roughness (LER) illustrated in Fig. 2 stems from the molecular structure of the photoresist and the corpuscular nature of light. The polymer chemistry of the 193nm lithography used now for few technology generations mainly determines the current LER limit of approx 5 nm [10]. In transistors with poly-silicon gate, Poly Gate Granularity (PGG) illustrated in Fig. 3 is another important source of variability. PGG is associated with the surface potential pinning at the grain boundaries complimented by doping non-uniformity due to rapid diffusion along the grain boundaries [11]

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The introduction of high-k/metal gate technology improves the RDD induced variability, which is inversely proportional to the equivalent oxide thickness (EOT). The metal gate also eliminates the PGG induced variability. However, it introduces high-k granularity illustrated in Fig.4, and variability due to work-function variation associated with the metal gate granularity illustrated in Fig.5 [12]. In extremely scaled transistors atomic scale channel interface roughness illustrated in Fig.6 [13] and corresponding oxide thickness and body thickness variations can become important source of statistical variability.

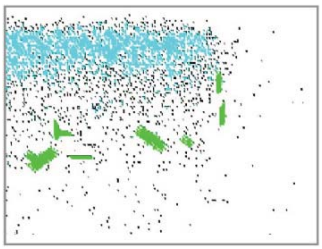

Fig. 1 KMC simulation of RDD (DADOS, Synopsys)

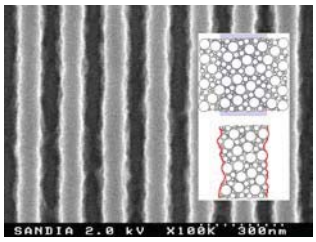

Fig. 2 Typical LER in photoresist (Sandia Labds.)

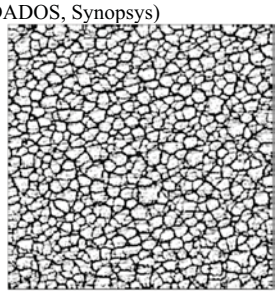

Fig. 3 SEM micrograph of typical PGG patterns.

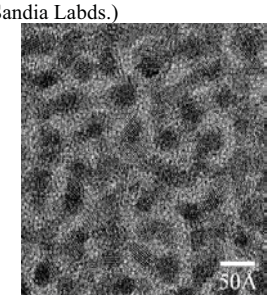

Fig. 4 Granularity in HfON high-k dielectrics (Sematech).

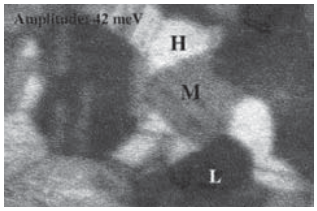

Fig. 5 Metal granularity causing gate work-function variation.

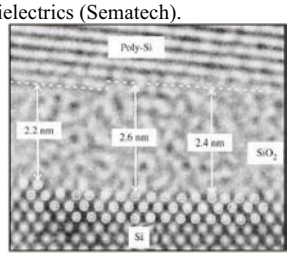

Fig. 6 Interface roughness (IBM).

On top of above-mentioned static statistical variability, problems related to statistical aspects of reliability are looming that can reduce the life-span of contemporary circuits from tens of years to 1-2 years, or less in the near future. In combination with RDD, which are the dominant source of statistical variability in bulk MOSFETs, the statistical nature of discrete trapped charges on defect states at the interface or in the gate oxide associated with hot electron degradation, negative / positive bias temperature instability (NBTI/PBTI) and hot carrier injection (HCI) result in relatively rare but anomalously large transistor parameter changes, leading to loss of performance or circuit failure [14]. In small devices, both the number of trapped charges and their positions varies from device to device. For example in a 35 nm p-channel SRAM transistor corresponding to the 45 nm technology generation a $1x10^{11}$ cm^2 NBTI trapped hole density results in average of 2 trapped holes per transistor. However, the number of trapped holes follows a Poisson distribution and in reality varies from 0 to 10.

B. Physical Simulation of Statistical Variability

The simulation results presented in this paper were obtained using the Glasgow statistical 3D device simulator, which solves the carrier transport equations in the drift-diffusion approximation with Density Gradient (DG) quantum corrections [15]. In the simulations, the RDD are generated from continuous doping profile by placing dopant atoms on silicon lattice sites within the device S/D and channel regions with a probability determined by the local ratio between dopant and silicon atom concentration. Since the basis of the silicon lattice is 0.543nm a fine mesh of 0.5nm is used to ensure a high resolution of dopant atoms. However, without considering quantum mechanical confinement in the potential well, in classical simulation, such fine mesh leads to carrier trapping at the sharply resolved Coulomb potential wells generated by the ionised discrete random dopants. In order to remove this artifact, the DG approach is employed as a quantum correction technology for both electrons and holes

The LER illustrated in Fig. 2 is introduced through 1D Fourier synthesis. Random gate edges are generated from a power spectrum corresponding to a Gaussian autocorrelation function [10], with typical correlation length Λ=30nm and root-mean-square amplitude Δ=1.3 nm, which is the level that is achieved with current lithography systems. The quoted in the literature values of LER are equal to 3Δ. The procedure used for simulating PGG involves the random generation of poly-grains for the whole gate region: a large atomic force microscope image of polycrystalline silicon grains illustrated at the top of Fig. 3 has been used as a template and the image is scaled according to the average grain diameter experimentally observed through X-Ray-diffraction measurements made both in θ-2θ and θ scan modes [16] (the average grain diameter is 65nm). Then the simulator imports a random section of the grain template image that corresponds to the gate dimension of the simulated device, and along grain boundaries, the applied gate potential in the polysilicon is modified in a way that the Fermi level remains pinned at a certain position in the silicon bandgap. In the worst case scenario the Fermi level is pinned in the middle of the silicon gap. The impact of polysilicon grain boundary variation on device characteristics is simulated through the pinning of the potential in the polysilicon gate along the grain boundaries. The individual impact of RDD, LER and PGG on the potential distribution in at typical 35 nm bulk MOSFET is illustrated in Figs. 7, 8 and 9 respectively.

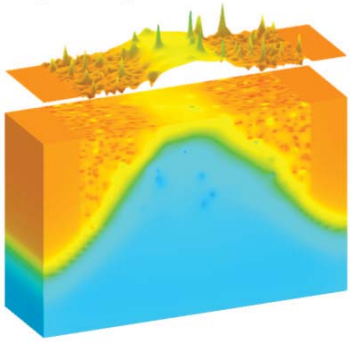

Fig. 7 Potential distribution in a 35 nm MOSFET subject to RDD.

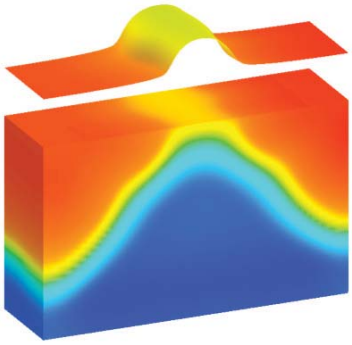

Fig. 8 Potential distribution in a 35 nm MOSFET subject to LER.

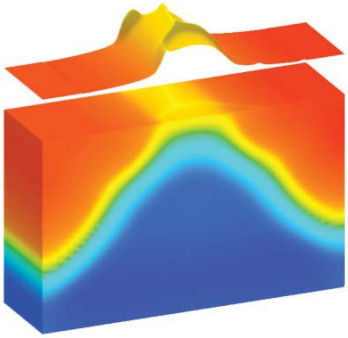

Fig. 9 Potential distribution in a 35 nm MOSFET subject to PGG.

The validation of our simulation technology is done in comparison with measured statistical variability data in 45 nm low power CMOS transistors [17]. The simulator was adjusted to match accurately the carefully calibrated TCAD device simulation results of devices without variability by adjusting the effective mass parameters involved in DG formalism, and the mobility model parameters. The calibration results are shown in Fig. 10.

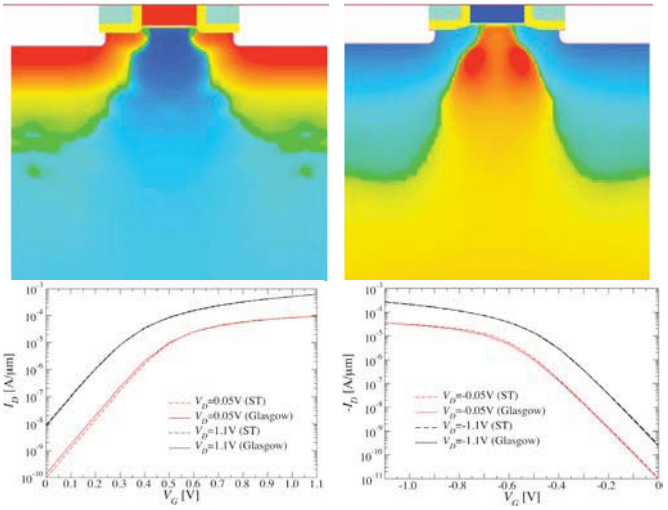

Fig. 10 Top: structure of the simulated 45 nm LP technology n(left) and p(right) channel MOSFETs; Bottom: Agreement between the commercial TCAD and the Glasgow 'atomistic' simulator results.

Statistical variability simulations are carried out, for nMOSFET, RDD, LER and PGG are considered while for pMOSFET, only RDD and LER are considered. The simulation results for the standard deviation of the threshold voltage σV_T introduced by individual and combined sources of statistical variability are compared with the measured data in Table 1. In the nMOSFET case the accurate reproduction of the experimental measurements necessitates the assumption that, in addition to RDD and LER, the PGG related variability has to be taken into account. Constant current criterion is used defining the threshold voltage as the gate voltage producing drain current of (I = 70 nA .W/L) at both low drain voltage of V_{DS}=0.05 V, and high drain voltage of V_{DS}=1.1 V. Good agreement has been obtained assuming that the Fermi level at the *n*-type poly-Si gate grain boundaries is pinned in the upper half of the band-gap at approximately 0.35eV below the conduction band of silicon. However, in the pMOSFET case the combined effect of just the RDD and LER is sufficient to reproduce accurately the experimental measurements. The reason for this is the presence of acceptor type interface states in the upper half of the band-gap which pin the Fermi level in the case of n-type poly-Si, and the absence of corresponding donor type interface states in the lower part of the bandgap which leaves the Fermi level unpinned in the case of p-type poly-Si [18].

Table 1: σV_T introduced by individual and combined source of statistical variability

	n-channel MOSFET		*p*-channel MOSFET	
	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)
RDD	50	52	51	54
LER	20	33	13	22
PSG	30	26	-	-
Combined	62	69	53	59
Experimental	62	67	54	57

Table 2: Individual and combined impact of RDD, LER on sV_T in 32 nm UTB SOI and 22 nm double gate nMOSFETs

	45nm σV_T (mV)		32nm σV_T (mV)		22nm σV_T (mV)	
	V_{ds}(50mV)	V_{ds}(1.1V)	V_{ds}(50mV)	V_{ds}(1.0V)	V_{ds}(50mV)	V_{ds}(1.0V)
RDD	50	52	5.3	6.1	6.4	8.1
LER	20	33	3.3	8.6	5.8	13
PGG	30	26	N/A	N/A	N/A	N/A
Combined	62	67	6.2	11	8.6	15
Measured	62	69	N/A	N/A	N/A	N/A

The scaling of the conventional bulk MOSFETs required continuous increase of the channel doping in order to control the short channel effects and the related leakage. This in turn keeps the RDD related variability high. Thin body silicon on insulator (SOI) transistors, due to better electrostatic integrity and short channel control, tolerate very low channel doping and therefore are resilient to the main source of statistical variability in bulk MOSFETs the RDD. Meantime very good electrostatic integrity and corresponding reduction of the threshold voltage sensitivity on channel length and drain voltage also reduces their susceptibility to LER induced variability. Table 2 presents the individual and combined impact of RDD, LER on σV_T in 32 nm UTB SOI and 22 nm double gate MOSFETs, corresponding σV_T results of the 45nm bulk technology generation nMOSFET is also presented as reference. The values of σV_T in the 32 nm UTB SOI and 22

nm double gate (DG) MOSFETs are 3-4 times smaller compared to the equivalent values in bulk MOSFETs with similar size. The results for a 22 nm double gate MOSFET are also representative for FinFET type device architectures.

The reduction of the RDD, LER variability in the UTB SOI and DG MOSFETs focuses the attention on NBTI, PBTI and HCI related variability. Also the introduction of high–k gate dielectric and the corresponding relatively high density of fixed and trapped charge (FTC) introduces unwanted variability which can neutralize the benefits from low channel doping and reduced short channel effects. Figure 11 illustrated the impact of FTC with different interface charge density on the potential distribution in 32 nm UTB SOI MOSFETS described in details elsewhere [19]. The impact of different interface trapped charge density on σV_T in 32 nm UTB SOI and 22 nm double gate MOSFETs is summarized in Table 3.

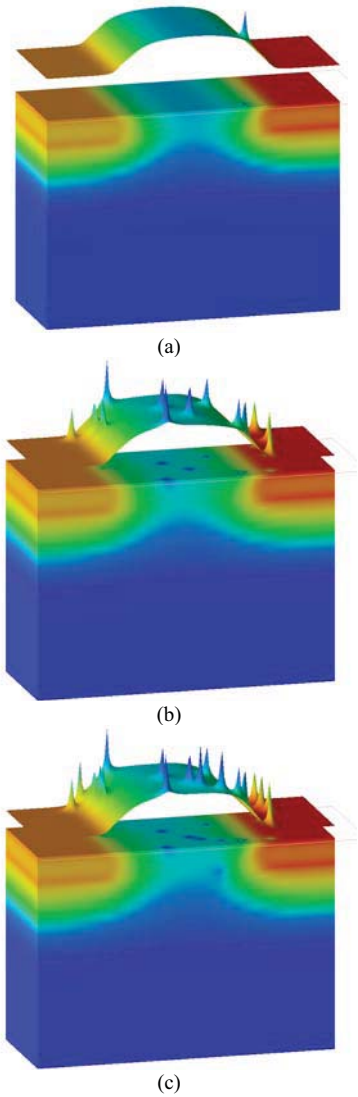

Fig. 11 Typical potential profiles corresponding to trap charge with sheet density at (a) 1e11cm^{-2}, (b) 5e11cm^{-2}, and (c) 1e12cm^{-2}

In the past the research in new gate stack materials and new device architectures has been mainly motivated by the drive to improve the device performance. Not any more. As illustrated in Fig. 12 the main driving force behind the introduction metal gate technology, fully depleted SOI and FinFET devices is the promise for reduction of the statistical variability.

Table 3: Summary of simulation results of different interface charge density

	32nm σV_T (mV)		22nm σV_T (mV)	
	V_{ds}(50mV)	V_{ds}(1.0V)	V_{ds}(50mV)	V_{ds}(1.0V)
Trap (1e11cm^{-2})	11	11	5.1	4.8
Trap (5e11cm^{-2})	18	17	13	12
Trap (1e12cm^{-2})	26	23	18	17

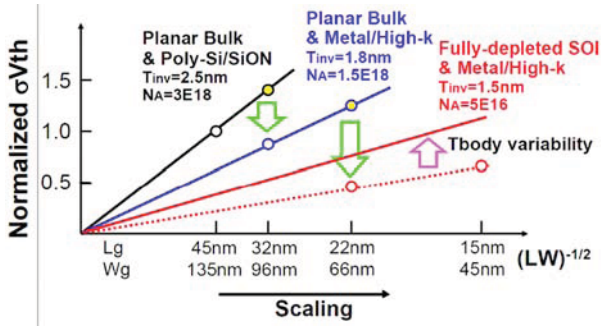

Fig. 12 Statistical variability reduction scenario. Source: 2007 ITRS Winter Public Conference.

III. Direct Statistical Compact Modeling And Its Applications

A. Direct Statistical Compact Modeling

It is very important to be able to capture the simulated or measured statistical variability in statistical compact models since this is the only way to communicate this information to designers. Unfortunately, the current industrial standard compact models do not have natural parameters designed to incorporate seamlessly the truly statistical variability associated with RDD, LER, PGG and other relevant variability sources. Fig. 13 shows the spread in I_D-V_G characteristics obtained from 'atomistic' simulator due to the combined effect of RDD, LER and PGG for a 35nm gate length device, and Fig.14 shows the corresponding probability plot of linear I_{on}, which is one of the important device figures of merits that can determine the circuit speed at nanometer regime. For a normal distribution, it should follow the straight line. It's clear from Fig.13 that the magnitude of variation introduced by statistical variability sources at nanometer regime is huge, for this particular case, the I_{off} can spread by almost 3 order of magnitude. Further more, Fig.14 demonstrates that the transistor electrical performance parameters not always follow normal distribution.

A two-stage direct statistical compact model extraction procedure [20] was developed to accurately transfer device statistical variation into compact models. At the first stage, a combination of group extraction and local optimization strategy for BSIM4, a local level parameter extraction strategy for PSP, has been applied respectively to obtain the complete set of BSIM4 and PSP parameters for uniform device. The resulting compact model card serves as the base model card for the second stage statistical extraction.

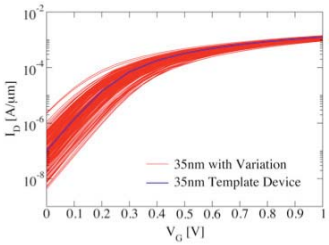

Fig. 13 Variability in the current voltage characteristics of a statistical sample of 200 microscopically different 35nm square (W=L) nMOSFETs at V_D=1 V

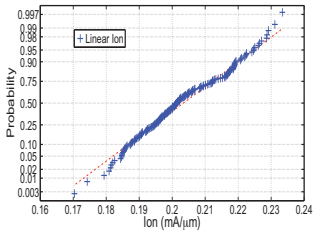

Fig. 14 Probability plot of linear *Ion* of a statistical sample of 200 microscopically different 35nm square (W=L) nMOSFETs at V_D=50mV

Based on the physical analysis of the impacts of intrinsic SV on device operation, 7 possible statistical parameters have been identified for BSIM4 and PSP respectively to capture the intrinsic SV. For BSIM4, *Vth0* is basic long channel threshold voltage parameter, and can be selected to account for traditional threshold variation introduced by SV; *U0* is low-field mobility parameter, and can be selected to account for current factor variation caused by SV; *Nfactor* and *Voff* are basic subthreshold parameters, and can be used to account for subthreshold slope and off current variation; *Minv* is moderate inversion parameter, and is selected to account for variation at moderate inversion regime; *Rdsw* is basic S/D resistance parameter, and is selected to account for dopant variation at S/D region; *Dsub* is DIBL parameter and is selected to account for DIBL variation introduced by SV. For PSP, NSUBO is the basic substrate doping parameter that physically determines the threshold voltage of device, and can be chosen to account for threshold voltage variation. Both CFL and ALPL are short channel effects parameters, and can be used to account for short channel effects variation. UO and CSO are mobility parameters, and are selected to account for transport variation introduced by SV. CTO is interface state parameter, and together with NSUBO, can be used to mimic the subthreshold behavior variation introduced by SV. RSW1 is source/drain series resistance parameter, and is selected to account for the influence of SV at S/D region.

The advantage of this approach is two fold: firstly, it does not require the variation of device electrical performance parameter follows any particular distribution; secondly, it does not need any pre-assumption of statistical compact model parameter distribution, correlation and sensitivity. As a result within the accuracy of the compact model fitting this approach will be the most accurate representation of the current voltage characteristics from the physical 3D simulations or from measurement.

The accuracy in representing each of the device characteristics and figures of merit under the influence of SV depend on the number of statistical parameters used in the second stage statistical extraction. Statistical parameters are selected in an order following their statistical significance to form the different size of parameter set. As long as the parameter set contain both low field (such as Vth0 of BSIM4, NSUBO of PSP) and high field parameters (such as Dsub of BSIM4, CFL of PSP), two sub-steps are applied during direct statistical parameter extraction: gate characteristics at low drain bias condition are selected to extract basic variation parameters at first step where high-field characteristics variation is extracted during the second sub-step. Due to the increasing importance of standby power dissipation in low power IC design, we treat *Ioff* and *Ion* equally during statistical extraction and the RMS error calculation in subthreshold region is based on linear scale as at the on current regime.

Table 4. Statistical parameter extraction errors for BSIM and PSP

Number of parameters	Average RMS fitting error(%)		Maximum RMS fitting error(%)		Standard Deviation	
	BSIM	PSP	BSIM	PSP	BSIM	PSP
1	16.8	16.5	30.1	27.8	4.3	4.23
2	10.5	11.8	22.5	24.6	3.5	3.93
3	8.5	9.1	21.5	21.9	4.1	2.96
4	3.99	5.44	9.75	13.9	1.4	2.22
5	2.85	2.59	6.75	8.2	1.15	1.25
6	1.56	1.58	3.6	5.2	0.6	0.63
7	1.16	1.32	2.8	3.6	0.45	0.59

The impacts of different size of statistical parameter set on the statistical compact modeling accuracy for BSIM4 and PSP are summarized in Table. 4, the device under investigation is a 35nm gate length MOSFET. Although surface potential based PSP is more device physics oriented comparing to threshold voltage based BSIM4, both models do not have natural structure to describe the intrinsic SV. As a result, the overall accuracy of the direct extraction results is similar for BSIM4 and PSP. The average RMS errors for both BSIM4 and PSP are around 16% at 1-parameter set, and reduce to around 1% at full 7-parameter set. The common practice is to use threshold voltage and current factor to describe variation in compact models, if the threshold voltage and the mobility parameter are used as a 2-parameter SV set in BSIM4, the average RMS statistical compact modeling error is 10% and for each individual device, the RMS error can be scattered in the range form 5% to 25%. On the other hand, it's worth mentioning that the device area is a determinant factor in statistical variation of device characteristics and the use of small statistical parameter set would be helpful for development of general statistical compact modeling strategy that can cover a wide range of device geometries. In this paper, we focus on the statistical parameter extraction results based on the 7-parameter set.

The detailed direct extraction results are presented in Fig. 15. BSIM4 has a slight edge with the mean RMS error of 1.16% compared to 1.32% for PSP. This may be due to the more empirical nature of BSIM4 perhaps provides some subtle flexibility to capture SV in a direct extraction approach, or caused by different parameter identification procedures between BSIM4 and PSP. Fig. 15 also demonstrates that although threshold voltage variation is a good indicator for subthreshold leakage current variation due to the very strong correlation between them, for a given threshold voltage value, Ion value can scatter more than ±10% around its' mean. This indicates that just considering threshold voltage variation in SV study cannot provide a full SV picture particularly when timing variability is of a major concern.

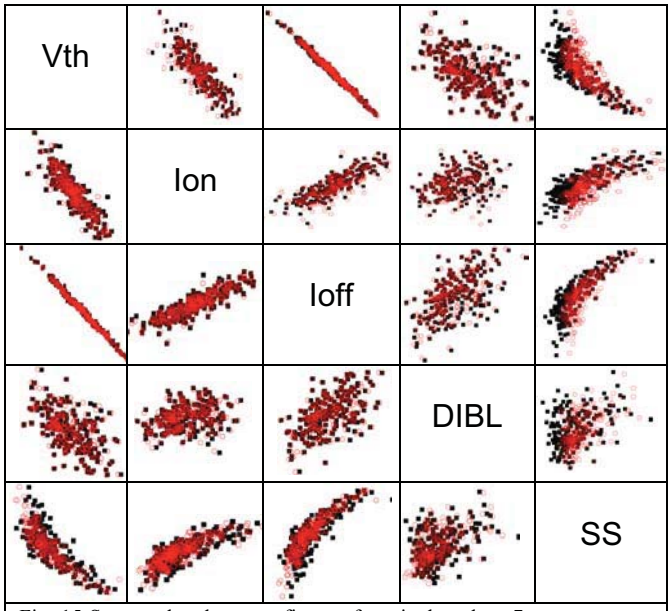

Fig. 15 Scatter plots between figure of merits based on 7-parameter set. Black square: physical statistical device simulation; Red circle: direct statistical compact modelling. Down-left: BSIM4, Up-right: PSP.

B. Statistical Circuit Simulations

Based on the statistical compact model libraries built from direct statistical compact modeling results, we have investigated the impact of RDD on 6T and 8T SRAM stability for the next three generations of bulk CMOS technology [21]. In the following discussions, we use 25 nm, 18 nm and 13 nm gate length transistors described in details in [15].

The functionality of SRAM is determined by both static noise margin (SNM) and the write noise margin (WNM). By using "write assist" technology [22], WNM can be dramatically improved; hence we focus our discussion on SNM aspect of SRAM scaling. The bias configurations associated with the SNM for 6T and 8T SRAM cells is shown in Fig.16 (a) and (b) respectively.

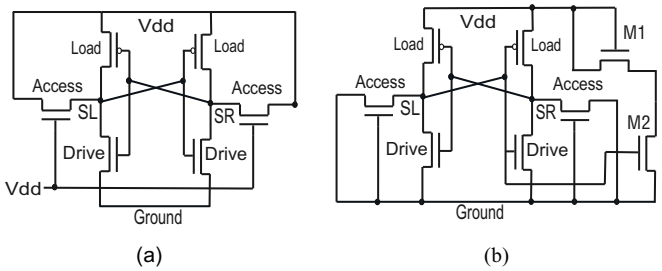

Fig. 16 Bias configuration for SNM for (a) 6T SRAM cell (b) 8T SRAM

The results of the distribution of SNM for 6T and 8T SRAM cells with a cell ratio of 2 are shown in Fig.17. The supply voltages for the 25nm, 18nm and 13nm generations are taken as 1.0, 1.0 and 0.9 V respectively. For 6T SRAM cells at the 13 nm generation, around 2% are not readable even under ideal conditions. No generation can meet the 'μ-6σ' yield criterion [23] without resorting to bias control approaches. However, employing an 8T cell structure dramatically improves SNM performance. The mean μ of SNM for each generation are well above 200mV, 150-200% higher than their 6T counterparts. The standard deviation σ has a similar value for both the 25nm and 18nm generations, and is 30% less at the 13 nm generation. From a SNM point of view, all three generations of 8T cells can pass the 'μ-6σ' yield test with a considerable margin.

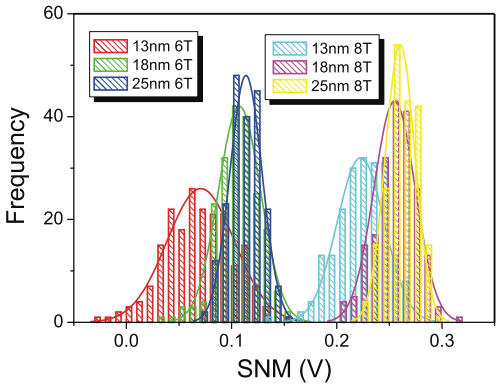

Fig. 17 Distribution of SNM over ensembles of 200 6T and of 200 8T SRAM cells for the 25, 18 and 13 nm generations respectively.

One of the fundamental limitations on future ULSI system integration is power dissipation. However, supply voltage scaling has been historically, and will continue to be much less aggressive than device scaling, with yield being one of the major reasons behind this. Since 8T SRAM can provide significantly improved SNM figure, this in turn will open a window for bolder power supply scaling. Fig. 4 shows the yield criterion for 8T SRAM cells with a cell ratio of 2 against supply voltage. For the 25 nm and 18 nm generations, as far as SNM is concerned, reasonable yield can be expected even when the supply voltage drops to 0.5 V. For the 13 nm generation, although the normalized standard deviation of the on-current can be 20% of the mean due to RDD, the minimum workable supply voltage can still remain at 0.7 V. Since the minimum supply voltage of a ULSI system is usually limited by its SRAM component [24], employing an 8T cell structure will provide greater flexibility with respect to power budget issues in system design.

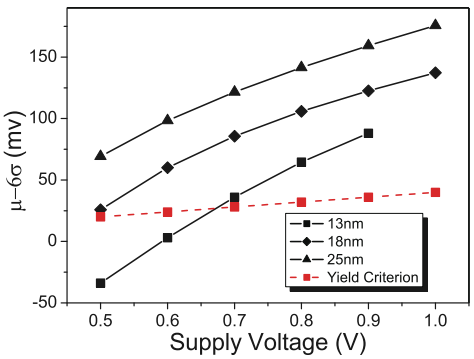

Fig. 18 Six sigma yield performance of 8T SRAM cell against supply voltage.

IV. Benchmarking Of Commonly Used Statistical Parameter Generation Approaches

One of the major disadvantages of the direct statistical parameter extraction approach is that the device sample size is pre-determined by size of compact model library. Common practice in Monte Carlo circuit simulation is to generate

statistical parameter values on the fly. Two typical statistical parameter generation approaches are investigated in comparison to the direct statistical extraction results: The first approach is to generate statistical compact model parameters assuming independent normal distribution for each extracted parameter, which is a standard approach in most of spice simulators, and will be called "naïve approach" in this paper. The second approach is based on Principal Component Analysis (PCA) taking care of the correlations between the extracted parameters, and will be called "PCA approach" in this paper. The PCA itself does not require that the original multi-dimension data follow a particular distribution. However, the reconstruction of the original data from statistical independent principal components is simpler under the assumption that the original data closely approximate normal distributions. Therefore in the PCA approach, we assume that parameters follow normal distribution.

The capability of the naïve and the PCA approaches to reproduce key device figure of merit – Ion, are illustrated in Fig.19, which clearly demonstrate the deviations in the tail due to the shared assumption between the two approaches for Normal distribution of the extracted parameters. Although both approaches can preserve the mean of the distribution, only PCA approach can generally regenerate the Ion distribution trend, and the naïve approach produces a considerable error in whole distribution region. When comparing BSIM4 and PSP, both the naïve and the PCA approaches in PSP can better reproduce the distributions of the physical device parameters, with an error in standard deviation σ, of 3% for the PCA approach, an error of 30% in σ for the naïve approach, while the corresponding errors for BSIM4 are 18% and 51% respectively.

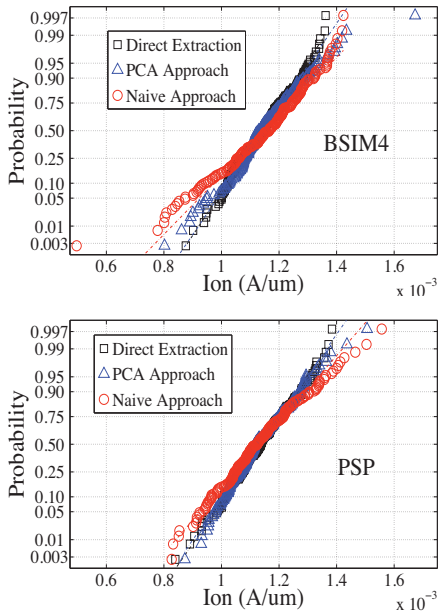

Fig. 19 Probability plot of Ion generated by different statistical approaches

V. Statistical Parameter Generation Based On Nonlinear Power Method

In order to improve the accuracy of statistical parameter generation in the tail regions, a newly developed Nonlinear Power Method (NPM) is employed to not only maintain the correlations between statistical compact model parameters, but also to preserve the high moments of the parameter distributions. NPM is based on moment matching technique to determine first four central moments of non-normal random variable Y_i representing *ith* statistical compact model parameter. The non-normal random variable Y_i can be generated using the polynomial transformation of normal random variable $Z \sim N(0, 1)$ as follows

$$Y_i = \sum_{k=1}^{s} c_{k-1} Z^{k-1} \tag{1}$$

where setting $s = 4$ controls up to the fourth moment, and this requires to knowing the even central moments of Z up to the 12^{th} order. It is not necessary to calculate the odd central moments of Z since all of these values are zeros. Substituting the values of central moments of Z into the formulas of Y_i moments leads to a nonlinear system, and its solution provides an exact solution of constants c_k. In order to maintain the parameter correlations, the intermediate correlations matrix between Y_i variables is calculated following the procedure described in [25]. Finally, multivariate non-normal distribution of random variables Y_i is generated using a combination of singular value decomposition of intermediate correlations matrix and NPM approach.

As an example, NPM based approach is applied for random generation of PSP statistical parameter set. Fig. 20 clearly demonstrates that at tail regions of statistical parameter distribution, NPM approach can preserve the original direct extraction result, while PCA approach fail to achieve this due to the normal distribution assumption. As a result, the statistical property of device electrical performance parameters can be better reproduced.

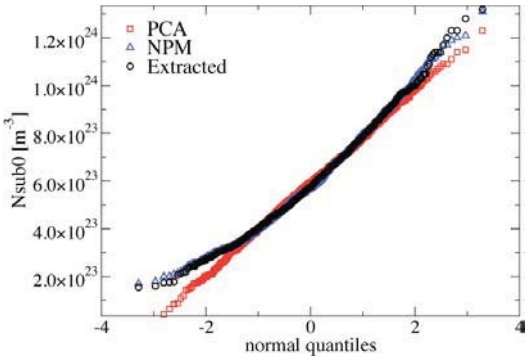

Fig. 20 Probability plot of key PSP parameter generated by different statistical approaches

Monte Carlo circuit simulation of a propagation delay in a simple inverter was carried out to assess the impact of parameter generation approaches on accuracy of statistical circuit simulation. The results of Monte Carlo circuit simulation are presented in Fig. 21. The delay distribution based on NPM approach shows very close agreement with the distribution obtained using the directly extracted statistical compact model library, while PCA method produces the significant error in the lower tail of the delay distribution.

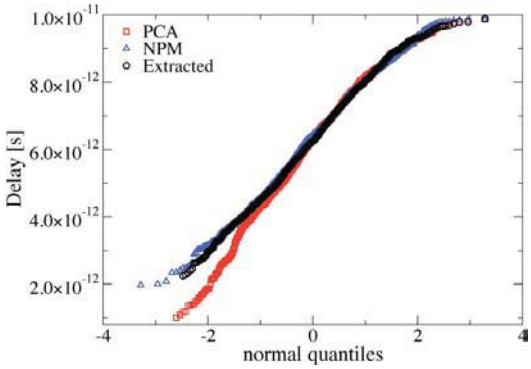

Fig. 21 Probability plot of inverter delay based on different statistical approaches

VI. Conclusion

The statistical variability introduced by discreteness of charge and matter has become one of the major concerns for the semiconductor industry. More and more the strategic technology decisions that the industry will be making in the future will be motivated by the desire to reduce statistical variability. SRAM is the most sensitive IC component in respect of statistical variability and needs special care and creative design solution in order to take full advantage from scaling in present and future technology generations. Statistical compact modeling plays a vital role in variability aware design. Although direct parameter extraction approach gives best accuracy, NPM is a step forward for development of general statistical compact modeling approach.

Acknowledgments

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