15.3 A 1V 77dB-DR 72dB-SNDR 10MHz-BW 2-1 MASH CT ΔΣM

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ΔΣM performance can be improved by using MASH or SMASH structures to obtain higher-order noise shaping [1]. They have better stability than single-loop structures. The power dissipation of ΔΣMs can be reduced by using simpler amplifiers such as single-stage or inverter-based amplifiers [2]. Selecting a passive or active-passive ΔΣM architecture, where the processing gain of comparator is used in the feedback loop of the ΔΣM's filter [3], allows a reduction in the number of amplifiers and their gain. This solution is very appealing for deep-nanometer CMOS technologies, because a comparator can achieve large gain through positive feedback, which improves with faster transistors. This paper presents a passive-active CT 2-1 MASH ΔΣM using RC integrators, low-gain stages (~20dB) and simplified digital cancellation logic (DCL). The ΔΣM, clocked at 1GHz, achieves DR/SNR/SNDR of 77/76/72.2dB for input signal BW of 10MHz, while dissipating 1.57mW from a 1V supply.

In active ΔΣMs, loop gain is distributed among all the integrators and the comparator has a signal gain close to 1, while in passive ΔΣMs it is concentrated in the comparator. Because passive integrators can only attenuate, the signal is small at the comparator input. This means that the comparator signal gain is larger than 1 because its output amplitude is close to V_{DD}. Figure 15.3.1 depicts a linear model of a 2nd-order passive-active ΔΣM, where H_1, H_2 are the passive integrators' transfer functions (TFs), E_{TN1}, E_{TN2} are thermal noises, G_1 is an inter-stage low gain block, b_1, b_2 are feedback factors, G_C is the comparator signal gain and E_C, E_Q denote comparator and quantization noises, respectively. Since feedback b_1 is added (subtracted) to V_{in}, it defines the theoretical maximum amplitude of V_{in}. Equations from Fig. 15.3.1 describe the signal D_{OUT} in baseband, where $H_{1,2}\approx 1$. One can conclude that if $G_C>>1$ the quantization noise is considerably suppressed, that E_C and E_{TN2} are attenuated by G_1, and that E_{TN1} is added directly to V_{in}. This means that the ΔΣM's SQNR is mainly defined by G_C (because $G_C>G_1$) and the SNR is limited by thermal noise.

Figure 15.3.2 shows a block diagram of the CT 2-1 MASH ΔΣM and Fig. 15.3.3 shows its schematic. Each stage of the MASH ΔΣM consists of RC integrators, gain block and 1b quantizer (clocked comparator + DFF). Excess loop delays (ELDs) of both stages are equal to T_s and in Z domain are interpreted as a z^{-1} delays. The constant ELD value facilitates proper operation of the DCL. Each integrator is an RC circuit and the feedback path is implemented by, a switched-capacitor C_{fi} connected in parallel with the C_i during clock phase ϕ_2. C_{fi} is pre-charged in ϕ_1 to either $+\Delta V_{ref}$ or $-\Delta V_{ref}$ (depending on the output bit-stream D_i). Additional capacitors C_{CMi} are used to reduce the common-mode voltage swing at the integrator's outputs. The integrator's TF can be described in the Z domain as $H_i(z)=\alpha_i/(1-\beta_i\cdot z^{-1})$, where $\alpha_i=T_s/(2\cdot R_i\cdot(C_i+C_{fi}))$ and $\beta_i=(1-\alpha_i)$. C_i denotes an equivalent capacitance of the main capacitor C_i and two common-mode capacitors C_{CMi}. Based on [4], equivalent comparator gains are approximated, for 1st and 2nd stages, as $G_{C1}=1/(\alpha_2\cdot b_2)$ and $G_{C2}=1/(\alpha_3\cdot b_3)$, requiring $\alpha_{2,3}<<1$ to increase these gains (α_3, b_3 are coefficients of the 3rd integrator). Blocks G_1 and G_{Mid} separate adjacent integrators, preventing loading and providing gain (~20dB). They are differential pairs loaded by resistors. These R's are also part of the RC time constants of the 2nd and 3rd integrators.

The output voltage of H_1 is mainly composed by the high-frequency E_{Q1} signal and the V_{in} component is only a fraction of this voltage because the first feedback cancels a significant part of V_{in}. This implies two things. First, H_1 has to provide attenuation ($\sim G_1/b_2$) to guarantee that the G_1 output amplitude is smaller than the feedback voltage of H_2 (to avoid saturation). This requires $\alpha_1\approx 1/(G_1/b_2)<<1$. Second, the distortion added to V_{in} by G_1 (a differential pair) is reduced due to the small value of V_{in} in the output of H_1. The $b_{2,3}$ should be kept small to increase the loop gains of both stages (by increasing $G_{C1,C2}$). However, making $b_{2,3}$ too small requires higher H_1 attenuation, making its thermal noise contribution more significant. As mentioned before, the SNR is limited by the integrators' thermal noises, which are defined by values of C's. The circuit has to be designed taking into account all the mentioned constraints. In this work the design solution was obtained through an optimization process.

In the block diagram of the MASH ΔΣM (Fig. 15.3.2) signal V_{int2} is the input signal of the comparator in the first-stage ΔΣM (2nd order), that is amplified by G_{Mid} and applied to second-stage ΔΣM. The DCL combines the outputs of both stages (D_1 and D_2) to cancel E_{Q1} and shape E_{Q2} by NTF_{Q1}. Since NTF and STF have denominators with poles located outside the signal band, only the DC gain factor of these denominators needs to be used in the DCL. This is done by evaluating the denominators of NTF_{Q1} and STF_2 at z=1 and using these values to scale the D_1 and D_2. Therefore the DCL becomes a FIR that can be implemented as a 6b look-up table with inputs $D_1[n]$, $D_1[n-1]$, $D_1[n-2]$, $D_2[n]$, $D_2[n-1]$, $D_2[n-2]$, which is built as a decoder using 270 logic gates and 4 DFFs. This simplification leads to a reduction in power and in the number of components (avoiding multipliers and adders). The DCL coefficients are calculated during the design phase and do not require adjustment or calibration during the circuit operation.

In a MASH architecture, the mismatch between analog (the ΔΣM stages) and digital (the DCL) TFs can degrade performance. This is addressed by a design methodology (based on [5]) that uses an optimization procedure to maximize the SNDR. The optimization takes into account ΔΣM's thermal, comparator and quantization noises. At each iteration, a Monte-Carlo (MC) analysis, where process and mismatch variations of R_i's, C_i's, C_{fi}'s, G_1 and G_{Mid} are included, is used to determine the average SNDR. These variations are only added to the analog part, while the DCL uses the nominal values to obtain a final design solution that has a low sensitivity, avoiding the need for calibration. Moreover, to reduce the distortion of the first differential pair, its input signal amplitude is also optimized to be smaller than $80mV_{pp,diff}$. After optimization, a 1000-case MC analysis (of a high-level model of the ΔΣM) assuming 3σ =16% for R_i's, 18% for C_i's, 25% for C_{fi}'s and 6% for $G_{1,Mid}$, resulted in a mean SNDR value of 72.9dB with a standard deviation of 1.3%.

The 2-1 MASH CT ΔΣM was fabricated in 65nm CMOS with a 1V supply. The external reference voltages are $V_{ref1,2}$=0.9V, V_{ref3}=0.44V. Similarly to [1], the MASH ΔΣM final outputs D_1 and D_2 are processed off-chip to produce D_{MASH}. This processing includes the DCL operation. The measured modulator's power consumption is 1.3mW, and obtained from electrical simulation the power of DCL is 270μW, giving in total 1.57mW. Figure 15.3.4 shows the FFT spectrum. Peak SNDR at -3dBFS ($1.16V_{pp,diff}$) and peak SNR at -1dBFS ($1.48V_{pp,diff}$) are 72.2/76dB, respectively. The two-tone test of IMD2/IMD3, near band-edge at -9dBFS inputs, is -78.5/-76.1dB, respectively. Figure 15.3.5 depicts measured SNDR vs. V_{in} amplitude (DR=77dB), and percentage power break-down of the MASH ΔΣM. Measurements for ±5% V_{DD} and V_{ref} variations resulted in worst-case SNDR of 70.5dB. The alias suppression (measured for various F_{in} from 980MHz to 1.02GHz) is ~51dB. Figure 15.3.6 summarizes the ΔΣM performance and compares it to the state of the art. This work achieves a Walden FOM_W of 23.6fJ/conv.-step and a Schreier FOM_S (SNDR) of 170.2dB. The combination of MASH topology and passive RC integrators with low gain blocks results in both the reduction of the power dissipation and of the chip size, as well as the lowest FOM_W for the ΔΣMs with BW from 5 to 50MHz shown in Fig. 15.3.6. Figure 15.3.7 depicts the micrograph of the test chip die with an active area of 0.027mm^2.

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References:
[1] Y. Do-Yeon et al., "An 85dB-DR 74.6dB-SNDR 50MHz-BW CT MASH ΔΣ Modulator in 28nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 272-273, Feb. 2015.
[2] S. Zeller et al., "A 0.039 mm^2 Inverter-Based 1.82 mW 68.6dB-SNDR 10 MHz-BW CT-ΣΔ-ADC in 65 nm CMOS Using Power- and Area-Efficient Design Techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1548-1560, July 2014.
[3] A. F. Yeknami et al., "Low-Power DT ΔΣ Modulators Using SC Passive Filters in 65 nm CMOS," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 2, pp. 358-370, Feb. 2014.
[4] F. Chen and B. Leung, "A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 774-782, June 1997.
[5] J. L. A. de Melo et al., "Design Methodology for Sigma-Delta Modulators based on a Genetic Algorithm Using Hybrid Cost Functions," *Proc. ISCAS*, pp. 301-304, May 2012.

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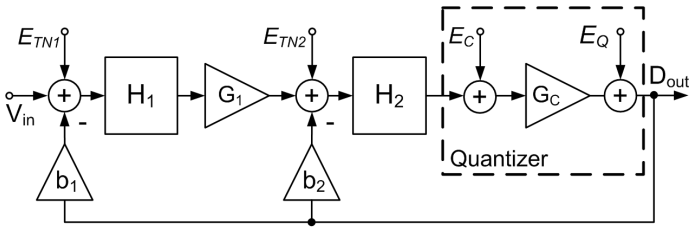

$$D_{out}=\frac{G_1\cdot G_C\cdot V_{IN}+E_{TN1}\cdot G_1\cdot G_c+E_{TN2}\cdot G_C+E_C\cdot G_C+E_Q}{1+G_C\cdot(b_2+b_1\cdot G_1)}$$

$$\approx G_C\cdot G_1\cdot\left(b_1+\frac{b_2}{G_1}\right)\approx G_C\cdot G_1\cdot b_1$$

$$D_{out}\approx\frac{V_{IN}}{b_1}+\frac{E_{TN1}}{b_1}+\frac{E_{TN2}}{b_1\cdot G_1}+\frac{E_C}{b_1\cdot G_1}+\frac{E_Q}{G_C\cdot G_1\cdot b_1}$$

Figure 15.3.1: Linear model of the first-stage 2nd order ΔΣM.

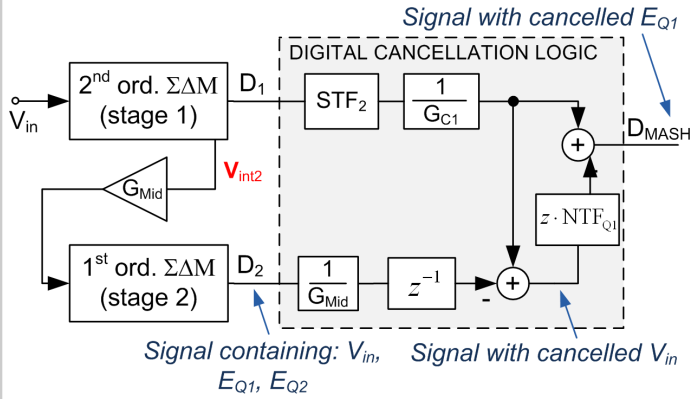

Figure 15.3.2: Block diagram of the MASH ΔΣM.

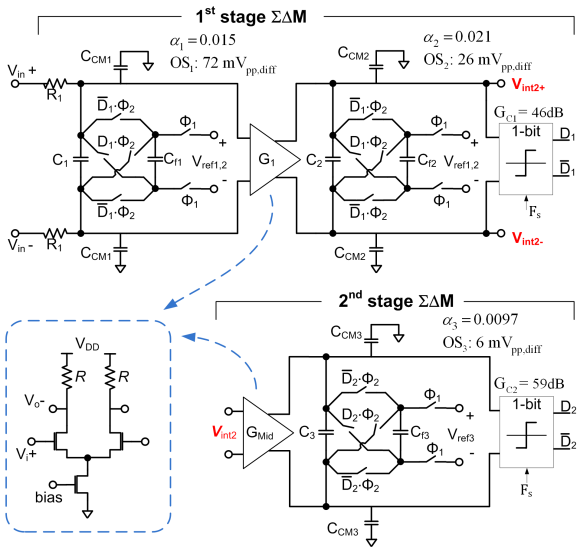

Figure 15.3.3: Schematic of the MASH ΔΣM.

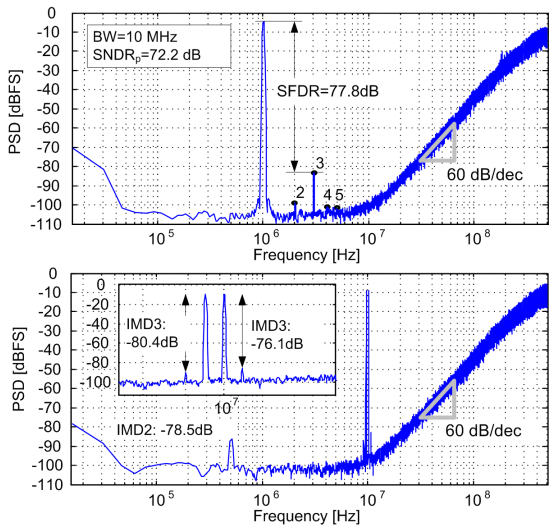

Figure 15.3.4: Measured PSD (average of eight 64k point FFTs) with F_{in}=1MHz and two input tones near the BW.

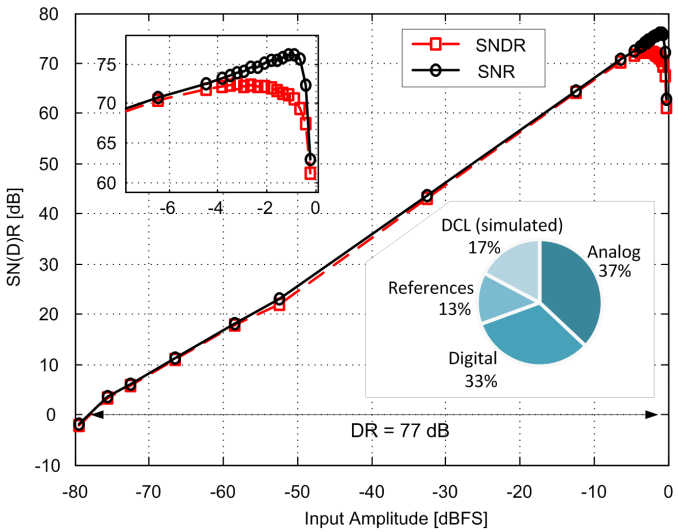

Figure 15.3.5: Measured SN(D)R as a function of V_{in} amplitude and percentage power break-down.

	This work	[1] ISSCC '15	[2] JSSC '14	Shu ISSCC '13	Loeda VLSI '15	Wei VLSI '15
Process [nm]	**65**	28	65	28	40	28
Area [mm²]	**0.027**	0.34	0.039	0.08	0.0194	0.066
Supply [V]	**1**	1.2/1.5	1.1	1.2 / 1.5	-	0.9/1.8
P [mW]	**1.57***	78	1.82	3.9	1.94	3.16
Fs [GHz]	**1**	1.8	0.65	0.64	0.6	0.432
BW [MHz]	**10**	50	10	18	10	5
DR [dB]	**77**	85	71.2	78.1	68.7	83.9
SNDR [dB]	**72.2**	74.6	68.6	73.6	67.4	80.5
FOM_W [fJ/step]	**23.6**	177.7	41.4	27.7	50.5	36.4
FOM_S [dB]	**170.2**	162.7	166	166	161.5	172.5

* Measured 1.3mW (two MASH stages) + 0.27mW (DCL - simulated)

$FOM_W=P/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$ $FOM_S=SNDR+10\cdot\log_{10}(BW/P)$

Figure 15.3.6: Performance table and comparison to prior works.

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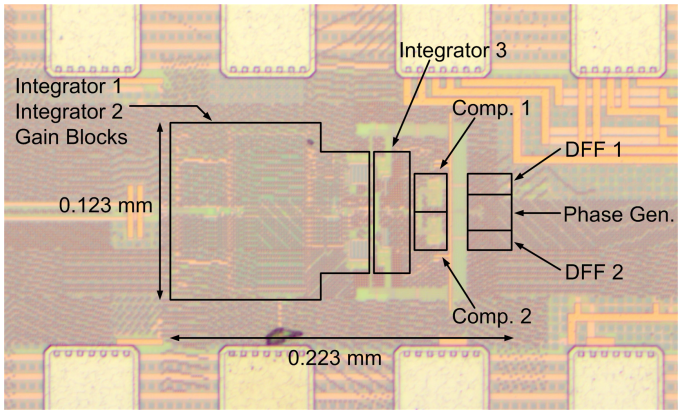

Figure 15.3.7: Micrograph of the test chip die in 65 nm CMOS.

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