A 550µW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction

Sang-Hyun Cho, Chang-Kyo Lee, Jong-Kee Kwon*, and Seung-Tak Ryu
KAIST, Daejeon, Korea
*ETRI, Daejeon, Korea
stigma@kaist.ac.kr, stryu@ee.kaist.ac.kr

***Abstract* - A speed-enhanced 10b asynchronous SAR ADC with multistep addition-only digital error correction (ADEC) is presented in this paper. Three virtually divided sub-DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC rearrange only. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. A prototype ADC was implemented in CMOS 0.13µm technology. The chip consumes 550µW and achieves a 50.6dB SNDR at 40MS/s under a 1.2V supply. The figure-of-merit (FOM) is 42fJ/conv-step.**

Keywords: SAR ADC, digital error correction

I. Introduction

Recently, many ingenious circuit techniques assisted by high-speed deep-submicron CMOS processes have made SAR ADCs a very popular type of architecture for many applications, as those advanced techniques and technologies enhance the conversion speed with excellent power efficiency. Nevertheless, many decision cycles for the Successive Approximation (SA) process remain as the fundamental speed bottleneck in SAR ADCs. As the most time-consuming process in medium-to-high resolution SAR ADCs is the DAC settling, the time for complete A/D conversion can be significantly reduced if the accuracy requirement for DAC settling can be relaxed. As reported in several papers [1-4], redundancy in code decisions makes this possible. Contrary to hardware-burdened earlier methods [1-2], recent publications [3-4] show that error correction methods based on binary DAC operations can greatly lessen the hardware overhead. However, the additional capacitors in DAC for redundancy in Liu's [3] and less systematic digital operations in Liu's [3] and Chen's [4] leave room for further improvement.

Prior to the binary DAC based techniques mentioned above, the authors reported a SAR ADC oriented digital error correction algorithm which required only the addition of a simple digital code with no DAC burden [5]. This paper presents a speed-enhanced prototype SAR ADC that builds on this idea with advanced hardware implementation.

II. Addition-Only Digital Error Correction

Fig. 1 shows an analogy of addition-only digital error correction (ADEC) algorithms in a two-step ADC and a SAR ADC using a 4b example. As with the two-step ADC, the decision procedure in the SAR ADC is virtually divided into the two steps of a 2b-coarse and a 3b-fine decision with 1b redundancy (2b-3b architecture). Both ADCs have coarse decision thresholds of ±1/4 V_{REF} which are deviated from those of a flash ADC by 0.5LSB of coarse resolution (= V_{SHIFT}) for ADEC operation. In SAR ADC, this threshold shift can be realized by starting the MSB decision with DAC level (V_{DAC}) at +1/4 V_{REF}, not the conventional center level.

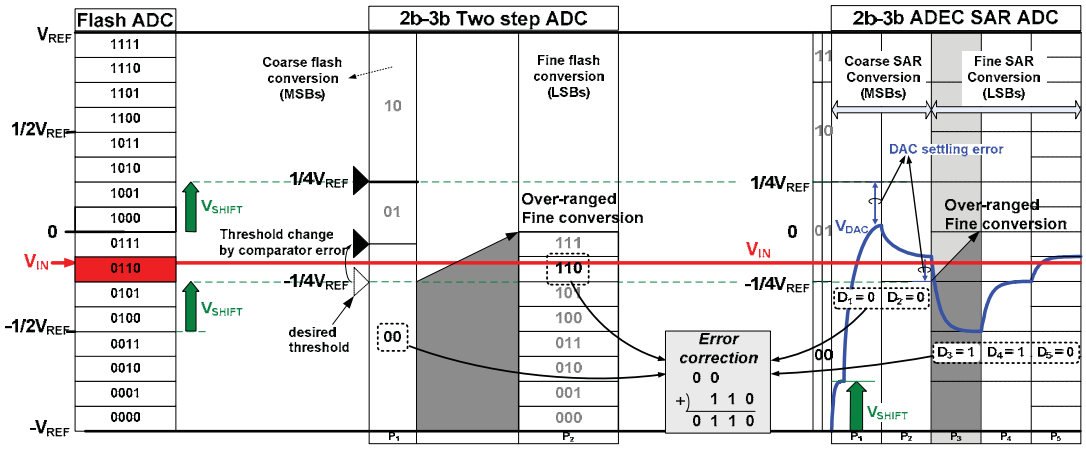

Fig. 1. Analogy of digital error correction in two-step and SAR ADCs

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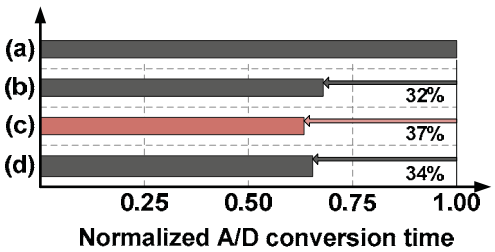

Fig. 2. Conversion time comparison for various SAR ADC architectures: (a) conventional, (b) 6b-5b, (c) 4b-4b-4b, (d) 4b-3b-3b-3b structures

There can be comparator errors in a coarse flash ADC in a two-step ADC and DAC settling errors in a SAR ADC. This is depicted in Fig. 1 by the comparator position shift (black triangle) and slow-settling V_{DAC} waveform. In the example, for a given input (V_{IN}), both ADCs generate incorrect MSBs of 00. In the following fine conversion process, the two-step ADC extends its reference range by a 0.5 LSB of coarse conversion resolution for decision redundancy. It then determines the 3b LSBs of 110 with an ideal fine flash ADC. Finally, the error-corrected full code of 0110 is achieved by adding MSBs and LSBs with one-bit overlap.

Redundancy in SAR ADC is implemented by inserting an additional decision step, P_3 in the example. The desired fine conversion range is determined by the determined MSBs, as with the two-stage ADC, and the fine conversion starts by placing the DAC level (V_{DAC}) at the center of it. Here, then, all of the threshold levels for coarse and fine decisions in the ADEC SAR are identical to those in a two-step ADC. Accordingly, as the effect of comparator error in the coarse ADC can be corrected in a two-step ADC by virtue of digital error correction, the code error during the coarse SA conversion occurring as a result of incomplete DAC settling is curable in the ADEC SAR ADC as long as the error amount is less than 0.5 LSB of the coarse resolution. This relaxed requirement of DAC settling can speed up the SAR ADC, even with an increased number of conversion cycles.

III. Speed Optimized Multi-Step ADEC SAR ADC

In the ADEC SAR ADC design, there must be a trade-off between the reduced DAC settling requirement and the time overhead due to the increased number of decision cycles. Thus, the ADEC SAR ADC can be designed with multiple redundant decision phases to optimize the conversion speed. To determine the speed-optimized architecture for the 10b ADC, the conversion speeds of several architectures have been compared with conventional designs. The total required time for 10b conversion was estimated, including all of the required times such as the input sampling time, DAC settling time, and comparator latching time. Additionally, the result was normalized to the speed of a conventional SAR ADC which has no redundancy. For this estimation, the input sampling time and average comparator decision time were assumed to be 4ns and 130ps, respectively, based on the proposed design and on the results of an earlier study [6]. Note that this work has an asynchronous SAR controller for further speed enhancement. Fig. 2 shows the comparison results with several sample architectures, showing 6b-5b with 1b redundancy, 4b-4b-4b with 2b redundancies, and 4b-3b-3b-3b with 3b redundancies. The comparison shows that the 4b-4b-4b architecture is the optimum choice among all, with a speed enhancement of 37%.

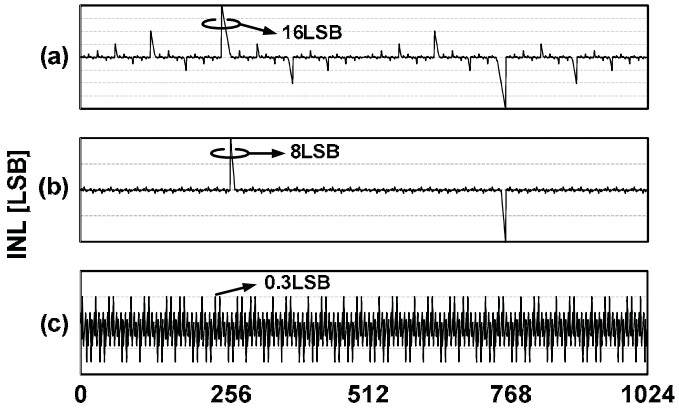

Fig. 3. INL comparison of differently configured SAR ADCs under 4b DAC settling: (a) conventional, (b) 6b-5b, (c) 4b-4b-4b structures

A behavioral simulation was conducted to compare the dynamic linearity of the architectures mentioned above under an operating speed which guarantees only 4b-accurate DAC settling in MSB decision. Fig. 3 shows the simulation result. This figure shows that the conventional and 6b-5b architectures have considerably large INL peaks, whereas the optimum choice shows less than 0.3 LSB errors. This demonstrates the effectiveness of the speed optimized 4b-4b-4b ADEC SAR ADC.

A prototype 10b SAR ADC with 4b-4b-4b architecture was implemented. A single-ended version schematic of its DAC and comparator are shown in Fig. 4(a) with its switching table (real design is in fully differential). The binary-weighted capacitor DAC was virtually segmented into 3 sub-DACs (sub-$DAC_{1\sim3}$) for ADEC operations. Here, only a 9b binary weighted DAC was designed for 10b SAR ADC by virtue of the three reference voltages, V_{REF+}, V_{CM} and V_{REF-}. The MSB is determined by connecting the bottom plates of all capacitors to the reference common level (V_{CM}) [7]. Thus, the DAC size is reduced by half, and as is the switching power consumption. Capacitors in sub-DAC_1 and sub-DAC_2 are split into two sub-capacitors (C_i = C_{i_1} and C_{i_2}, i = 4~9) to simplify the capacitor switching logic. This is explained later. This is explained later. The operation of the ADC is explained in Fig. 4 for a sample input of +27/1024 V_{REF}. DAC settling waveform (V_{DAC}) during the entire conversion process is shown in Fig. 4(b). First, V_{DAC} is shifted up by V_{SHIFT1} (= 32 LSB) by switching C_6 to V_{REF+}. At the same time, the MSB decision is conducted by connecting the rest capacitors to

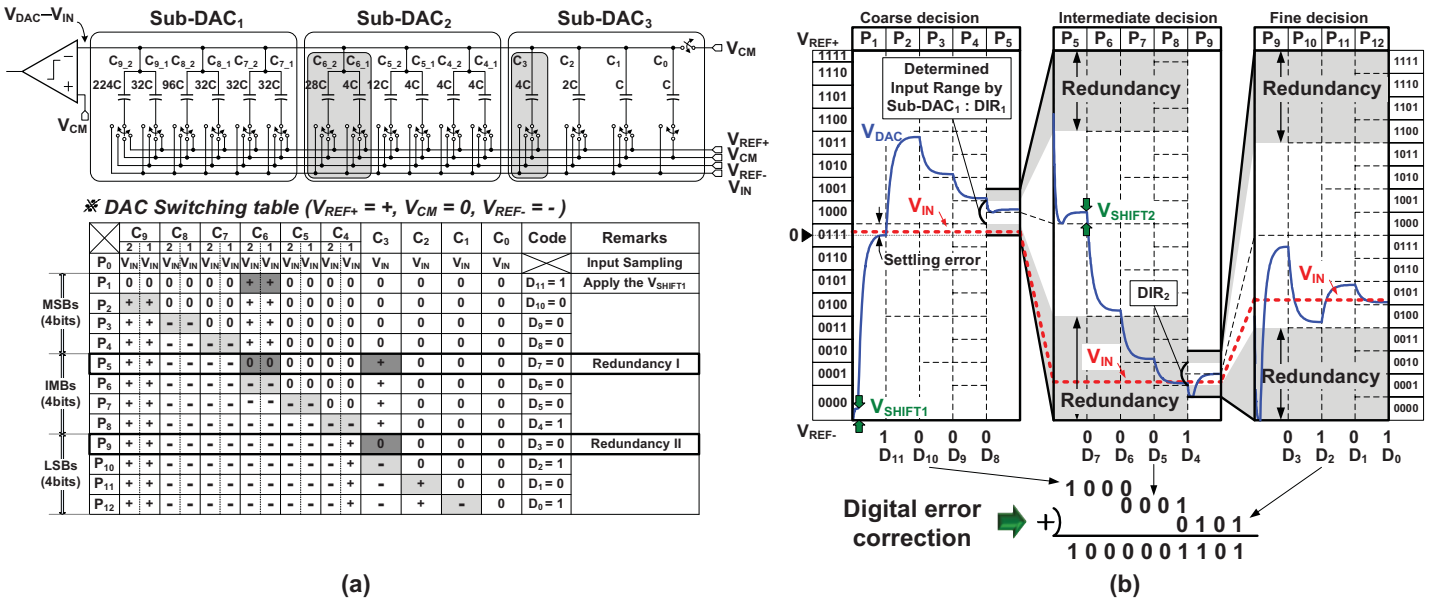

Fig. 4. (a) Virtually segmented (4b-4b-4b) 10bit ADEC SAR ADC and its switching table. (b) DAC waveform with incomplete settling

V_{CM}. Due to the incomplete settling of V_{DAC}, which is assumed to be less than 32 LSB, an incorrect decision is the result for D_{11}. The result is 1. Subsequently, SA operation continues by utilizing the capacitors in sub-DAC_1, as shown in the table, until 4 MSBs are achieved. 1000 is determined for $D_{11}D_{10}D_9D_8$ in the example. Before sub-DAC_2 is used for an intermediate code decision, the first redundant phase P_5 is inserted. In this phase, C_6 (= C_{6_1} + C_{6_2}) returns to V_{CM} to prepare for use in the sub-DAC_2 operation. As a result, V_{DAC} is automatically located at the center of the determined input range (DIR_1). At the same time, another V_{DAC} shift, V_{SHIFT2} (= 4LSB), is performed for consecutive ADEC. This is done by switching C_3 from V_{CM} to V_{REF+}. By the following SA operations with sub-DAC_2, the intermediate bits (IMBs) are obtained as '$D_7D_6D_5D_4$ = 0001'. In the second redundant phase P_9, C_3 returns to V_{CM} for the same reason C_6 does in P_5. However, in this case, V_{DAC} drops to the lower boundary of DIR_2 during this operation. Therefore, V_{DAC} must be raised by 8 LSBs to correct the subsequent operations. This can be performed by additional capacitor switching. As the capacitors in sub-DAC_3 are untouchable for $D_3D_2D_1D_0$ decision purposes, sub-DAC_2 is reconfigured by selecting one 4C-valued capacitor which has been connected to V_{REF-}. It is switched to V_{REF+}. C_{4_1} (=4C) is used in this example. This is why the capacitors in sub-DAC_2 are split with 4C's and why those in sub-DAC_1 are split with 32C's. In this algorithm, capacitor rearranging is required only when the LSB from the previous stage (D_8 before sub-DAC_2 in use and D_4 before sub-DAC_1 does, in this design) is 1; thus, switch controller design for this is simple. After this operation, normal SA operations are conducted, with the $D_3D_2D_1D_0$ result of 0101. After all those sub-decisions, the three produced 4b data examples are added together with one-bit overlap, as shown in Fig. 4(b), leading to an error-corrected output of 1000001101.

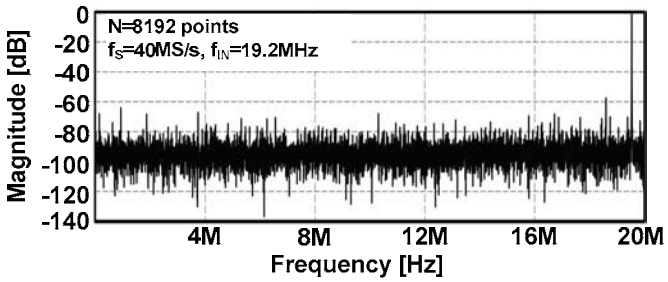

Fig. 5. Measured FFT result with 19.2MHz input at 40MS/s

IV. Experimental Results

TABLE I

Measured Performance

Process		0.13μm 1P8M CMOS
Supply		1.2V
Resolution		10b
Sampling rate		40MS/s
Power consumption	Comparator	155μW
	Digital	395μW
	Total	550μW
DNL		-0.78 ~ 0.72LSB
INL		-1.55 ~ 0.90LSB
SFDR @ 40MS/s		57.7dB @ f_{IN}=20MHz
SNDR @ 40MS/s		50.6dB @ f_{IN}=20MHz
Core area		500 x 640 μm^2
FOM		42fJ/conv.step

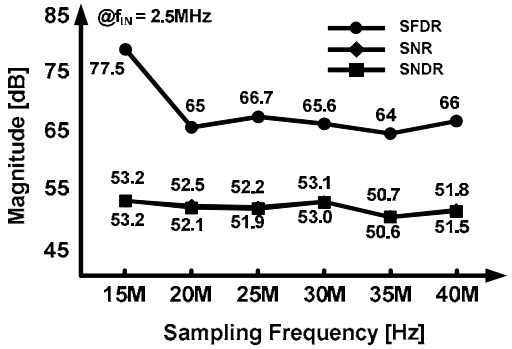

Fig. 6. Dynamic performances for various input frequencies

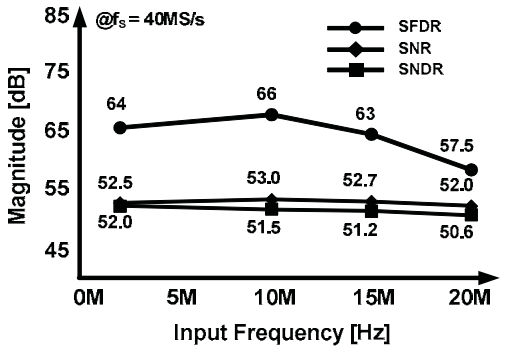

Fig. 7. Dynamic performances for various sampling rates

A prototype ADC was fabricated in a 0.13µm CMOS process with a core size of 500 × 640µm^2. The chip works under a 1.2V supply with reference voltages of 0.2V and 1.0V. Fig. 5 shows the measured FFT result for an input frequency of 19.2MHz at a sampling rate of 40MHz. Fig. 6 and Fig. 7 show the measured dynamic performance. At an input signal of 2.5MHz, the sampling frequency is swept from 15MHz to 40MHz. Except for the 15MHz case, SFDR and SNDR show stable results in ranges of 50.6 ~53.2dB and 64 ~ 66.7 dB, respectively. Dynamic performance with an input frequency sweep at 40MS/s resulted in 52dB and 50.6dB SNDR for 2.5MHz and 20MHz of input, respectively. The measured maximum DNL and INL were 0.8 and 1.5LSB, respectively. The relatively low SNDR from the measurement results from the poor DAC linearity, which itself stems from the routing parasitic capacitance. The total power consumption is 550µW and the ENOB is 8.4b. The resulting FoM is 42fJ/step.

This paper proposed a speed-optimized multi-step ADEC SAR ADC architecture capable of 37% speed enhancement but with negligible hardware overhead. The proposed systematic operational principle of the ADEC SAR ADC can be simply extended for higher resolution SAR ADC for optimization of its power and speed.

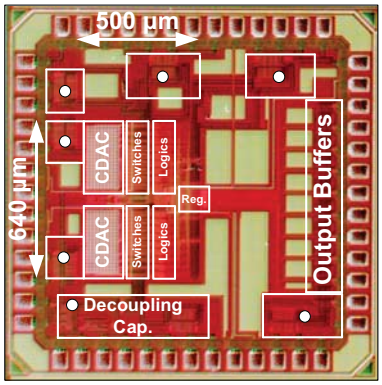

Fig. 8. Chip photograph

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