23.3 A 3-bit/2UI 27Gb/s PAM-3 Single-Ended Transceiver Using One-Tap DFE for Next-Generation Memory Interface

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Bandwidths of memory interfaces have been increased tremendously to enable high-data throughput while maintaining single-ended signaling and the supply voltage of I/O has been scaled down. Due to the increasing interface bandwidth the required area and power consumption has increased as well, resulting in higher I/O circuit design costs [3]. A high-loss channel causes ISI, which in turn limits the maximum data rate. Therefore, complex equalizers are needed for compensation, resulting in additional power dissipation and area overhead. As the data sampling rate increases, the deterministic and random noises degrade the data sampling margin and further limit the bandwidth. To lessen the negative impact of high channel loss and to reduce the forwarded clock frequency, multi-level signaling, such as PAM-4, can be used, as shown in Fig. 23.3.1 [2]. While the voltage sense margin for PAM-4 is theoretically $^1/_3$ of NRZ, in practice it is smaller due to simultaneous switching noise (SSN), crosstalk, and random noise in single-ended signaling. Eventually, the reduced voltage sense margin degrades the SNR, which causes a reduction in the BER. On the other hand, PAM-3's voltage sense margin is ½ of NRZ's. Duo-binary signaling is commonly used for PAM-3 signaling [1]. However, the pin efficiency and the forwarded clock frequency for duo-binary signaling is the same as for NRZ. In this paper, a 3b/2UI PAM-3 single-ended memory interface is proposed, with a pin efficiency of 150% and a reduced clock frequency, compared to NRZ signaling. To address PAM-3 equalizer inefficiencies a tri-level decision feedback equalizer (DFE) is implemented in the receiver (RX).

A high-level block diagram of the proposed PAM-3 single-ended transciever is shown in Fig. 23.3.1. In the TX, three 8:1 serializers convert 1.125Gb/s parallel data into 9Gb/s full-rate data (A, B, C) using an external 9GHz clock and an internal PRBS-7 pattern generator. The 3b/2UI half-rate encoder convert three data bits to the 18Gb/s up and down signals (UP/DN) to generate the 27Gb/s PAM-3 data via the N-over-N driver. The generated single-ended PAM-3 data stream is transmitted to the RX, along with the forwarded clock at $^1/_3$ of the data rate. In the RX, the single-ended-to-differential (S2D) amplifier with ground-termination for LPDDR interface converts the input data to the differential output. The 1-tap half-rate DFE compensates the post-cursor, and the three-original data are decoded by the 3b/2UI full-rate decoder. The quadrature-phase clocks, which are generated by the 4-phase generator with a duty-compensated half-rate clock, are used for the DFE and the decoder in the RX.

There are nine transition cases for the 3b/2UI PAM-3 signaling in the TX output, as shown in Fig. 23.3.2. Eight of which are mapped to express 3b for every 2UI. The remaining low-to-high transition are unassigned and used to detect the odd/even data in the RX, because there is no low-to-high transition between the odd and even data in normal operation. The generated UP/DN data are serialized by the 2:1 multiplexer and converted to singled-ended PAM-3 data by the N-over-N output driver. The output impedance of the binary-weighted driver is controlled for impedance matching with a ground-terminated 50Ω resistor in the RX. The supply voltage of the low-swing driver is 0.6V for the 308mV peak-to-peak voltage of the PAM-3 output.

In the proposed PAM-3 RX, the input stage consists of the ground terminated resistor and the S2D amplifier. A feedforward path is added to the first stage of the S2D amplifier to match the differential gain. The outputs of the S2D amplifier are fed to the 1-tap half-rate DFE for post-cursor cancellation. In the case that DFE has more than two input voltage levels, more than two current branches are used to express the different input levels. However, there is an unused case in the PAM-3 DFE which causes this inefficient in the PAM-3 DFE. In the proposed PAM-3 DFE, the unit tap of the summer is designed with only one current branch, like the DFE for NRZ signaling, while expressing three input voltage levels depending on the data as shown in Fig. 23.3.3 [3]. Comp_H and Comp_LB are applied to the tap as inputs, instead of the differential inputs for the three cases. When the gate voltages become zero, half of the tail current flows through each input MOS, and it expresses the middle level. This enables the DFE summer for the PAM-3 interface to be implemented with the same complexity as NRZ signaling. Due to the reduced number of current branches, the parasitic capacitance and the feedback delay is reduced. In the proposed DFE summer, Fig. 23.3.4, two current branches are used for half-rate operation, and the PMOS switches operate off the quadrature phase clocks (Q_{CK}, QB_{CK}). The strong-arm clocked comparators make the decision with I_{CK}, IB_{CK}, and the internal reference voltages. The outputs of the comparators are return-to-zero (RZ) signals and must be converted to non-return-to-zero (NRZ) signals for the proper operations of the DFE and the decoder. A CML-based SR-latch is commonly used for fast RZ-to-NRZ conversion; however, this consumes large power. In Fig. 23.3.4, the proposed RZ-to-NRZ converter is implemented in CMOS logic with a PMOS switch. When the clock is high, the output node of the RZ-to-NRZ converter is in high-impedance. This achieves both low-power and high-speed RZ-to-NRZ conversion without using a CML-based SR latch. The converted outputs are fed back to the DFE summer to cancel out the postcursor and to decode the data back to the three-original data (A, B, C) bits by the 3b/2UI full-rate decoder; which has the same logic depth as the encoder in the TX.

An external 9GHz clock, with an RMS jitter of 304fs, is applied to both the TX and the RX to generate and recover the data. The measured eye diagrams of the PAM-3 TX outputs are shown in Fig. 23.3.5. The 27Gb/s PAM-3 data are generated with a peak-to-peak swing of 308mV, and a sampling margin of 0.439UI for a single-channel without crosstalk. In the proposed RX, the delay of the clock, the threshold voltages of the comparators, and the coefficient of the DFE are manually controlled to achieve optimal BER. The measured eye diagrams and the bathtubs of the recovered PRBS-7 outputs are shown in Fig. 23.3.5. The bathtubs of the proposed PAM-3 interface are measured with a programmable error detector, by controlling the delay of the clocks in the RX. To prove the functionality of the proposed PAM-3 DFE, an internal eye-opening monitoring (EOM) circuit was added to the output node of the DFE summer. The eye was closed at the EOM circuit when the DFE is not used. On the other hand, with the use of the proposed PAM-3 DFE, the BER was measured at less than 10^{-12}, and an opened eye is obtained. A summary comparison with state-of-the-art memory interfaces is shown in Fig. 23.3.6. Compared to NRZ signaling, the proposed PAM-3 single-ended memory interface achieves a 150% pin efficiency, and the forwarded clock frequency is decreased by 33.3% for the same NRZ data rate. The power dissipation of the TX and the RX is 10.69mW and 17.03mW. For an 8b DQ pin case, the power efficiency will be further reduced since the forwarded clock can be shared. The power efficiency of the proposed transceiver is 1.03pJ/b at 27Gb/s due to the proposed energy-efficient PAM-3 DFE and the reduced forwarded clock frequency.

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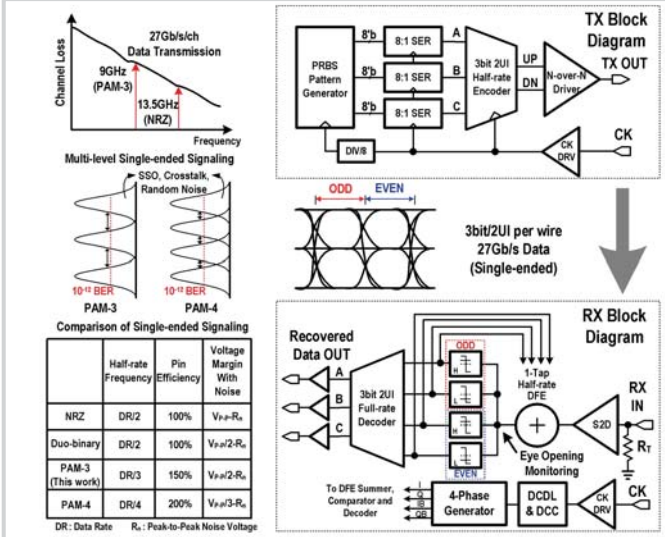
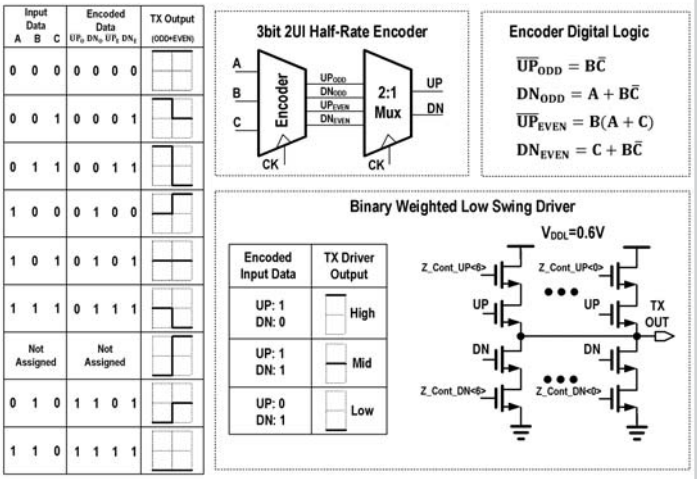


	Half-rate Frequency	Pin Efficiency	Voltage Margin With Noise
NRZ	DR/2	100%	V_{P-P}-R_n
Duo-binary	DR/2	100%	V_{P-P}/2-R_n
PAM-3 (This work)	DR/3	150%	V_{P-P}/2-R_n
PAM-4	DR/4	200%	V_{P-P}/3-R_n

DR: Data Rate R_n: Peak-to-Peak Noise Voltage

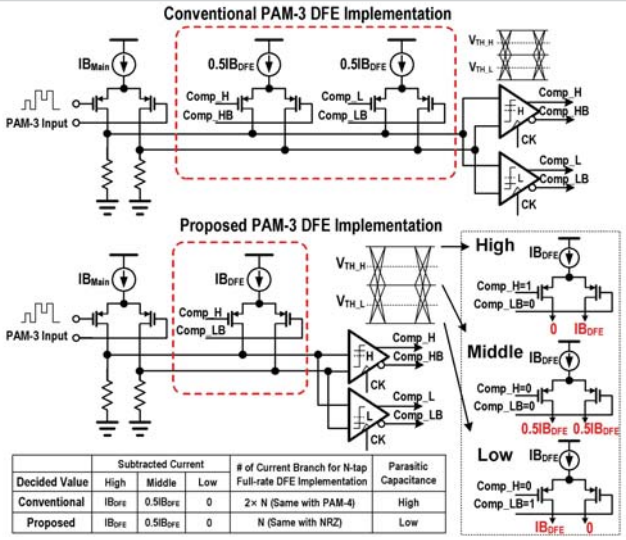
Figure 23.3.1: Top block diagram of the proposed PAM-3 single-ended transceiver.



Input Data A B C	Encoded Data $\overline{UP}_E$ DN_O $\overline{UP}_O$ DN_E	TX Output (ODD+EVEN)
0 0 0	0 0 0 0	
0 0 1	0 0 0 1	
0 1 0	0 0 1 1	
1 0 0	0 1 0 0	
1 0 1	0 1 0 1	
1 1 1	0 1 1 1	
Not Assigned	Not Assigned	
0 1 0	1 1 0 1	
1 1 0	1 1 1 1	

Encoded Input Data	TX Driver Output
UP: 1 DN: 0	High
UP: 1 DN: 1	Mid
UP: 0 DN: 1	Low

Figure 23.3.2: Proposed 3bit/2UI encoding and low-swing driver for PAM-3 modulation.



	Subtracted Current			# of Current Branch for N-tap Full-rate DFE Implementation	Parasitic Capacitance
Decided Value	High	Middle	Low		
Conventional	IB_{DFE}	$0.5IB_{DFE}$	0	2× N (Same with PAM-4)	High
Proposed	IB_{DFE}	$0.5IB_{DFE}$	0	N (Same with NRZ)	Low

Figure 23.3.3: Operation of the conventional and proposed PAM-3 DFE with 3 different cases.

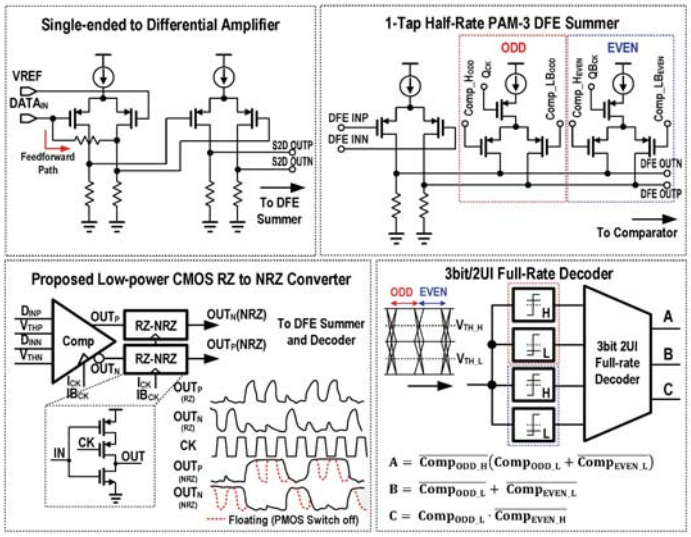


Figure 23.3.4: Implementations of the proposed PAM-3 receiver and 3bit/2UI decoding.

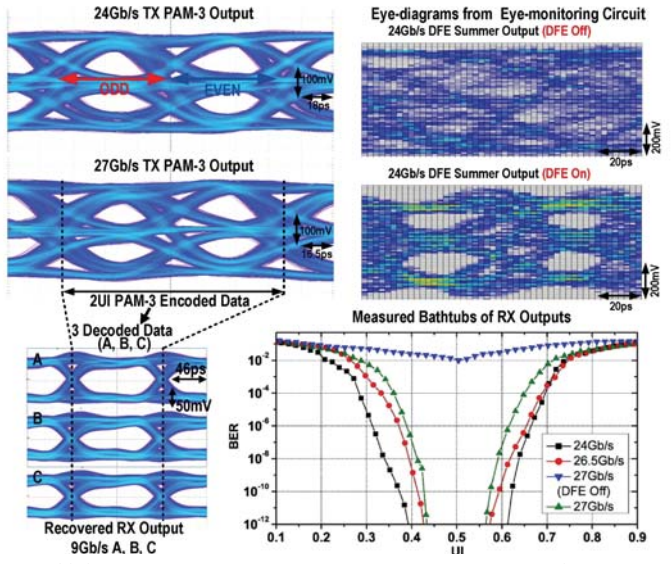
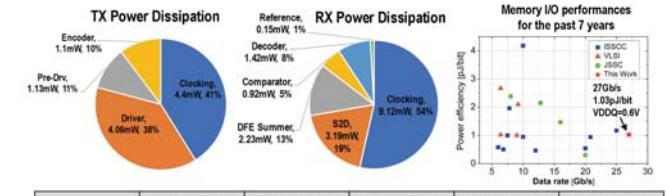


Figure 23.3.5: Measured eye-diagrams and bathtubs of the PAM-3 TRX.



	JSSC 2014 [1]	ISSCC 2015 [3]	ISSCC 2016 [4]	ISSCC 2018 [5]	This Work
Signaling Style	Duo-binary	NRZ	CNRZ-5	NRZ	PAM-3
Data Rate per Pin	7Gb/s	10Gb/s	20.83Gb/s	25Gb/s	**27Gb/s**
Forwarded Clock Frequency	3.5GHz (1/2 rate)	5GHz (1/2 rate)	3.125GHz (RX PLL)	12.5GHz (1/2 rate)	9GHz **(1/3 rate)**
Pin Efficiency	100% (1bit/1UI·1pin)	100% (1bit/1UI·1pin)	83% (5bit/1UI·6pin)	100% (1bit/1UI·1pin)	**150% (3bit/2UI·1pin)**
Power Efficiency	0.56pJ/bit	4.18pJ/bit	0.94pJ/bit*	1.17pJ/bit#	1.03pJ/bit
VDDQ	1.05V	1V	0.925V	0.7V§	**0.6V**
Equalization	Duo-binary	FFE+IIR+DFE	T-Coil+CTLE	T-Coil+CTLE	**PAM-3 DFE**
Reach	15mm	100mm	12mm	80mm	20mm
Area	0.0333mm²	0.0091mm²	0.629mm²	0.3875mm²	0.0135mm²
CMOS Technology	65nm	65nm	28nm	16nm	28nm

* 6 Data & 1 Clock (PLL Clock)
\# 8 Data & 1 Clock
§ V_{DDQ} is equal to V_{reg_PLL}, 0.7V at T=0° in TT corner

Figure 23.3.6: Power breakdowns, memory I/O performances, and comparison table.

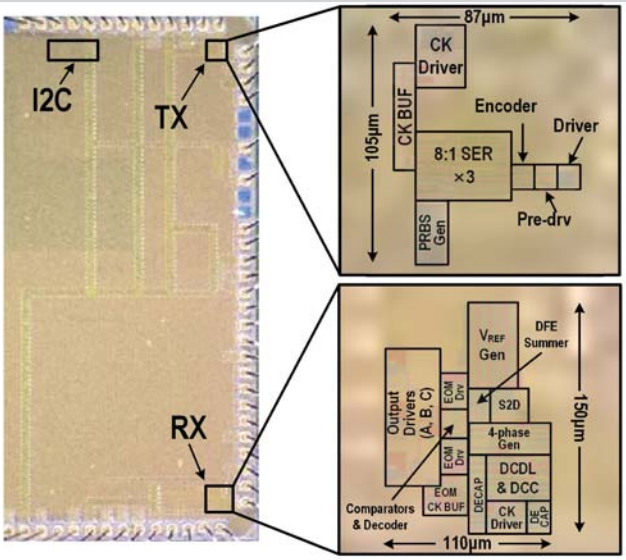


Figure 23.3.7: Microphotograph of the proposed PAM-3 TRX.

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