FP 14.2: Development of Single-Chip Multi-GB/s DRAMs

Richard Crisp, Kevin Donnelly, Alfredo Moncayo, Don Perino, Jared Zerbe

Rambus Inc., Mountain View, Ca.

Next-generation PCs and workstations will subsume much of the media processing into the CPU performing the 3D, audio, video decompression, modem and other processing intensive functions in software demanding as much as a 10x increase in processing throughput. Key to attaining the processing throughput goals is increased memory bandwidth and caches alone are not sufficient.

Bandwidth may be increased by increasing either data path width or operating frequency. Counting the necessary address, control, power and ground pins shows the typical 64b wide bus requires over 110 pins with a 128b bus needing more than 200pins. Wide buses increase cost by adding to die size, packaging, test and, use costs. Increasing bus operating frequency beyond 66MHz creates numerous problems in timing margin assurance, cost, latency, and signal integrity [1].

The density of DRAM components quadruples approximately every 3 years. As density quadruples, so must bandwidth to maintain the same fill rate (MB/s /MB). Therefore the need for bandwidth to be increased on a per-device level grows each generation. With 64Mb and 256Mb devices nearing volume shipments, the need is arising for multi-gigabyte per second DRAMs.

The major issues to be addressed in development of multi-gigabyte per second DRAMs are core and device organization, clocking/clock recovery, I/O timing, modular expansion, and power dissipation. Due to the length and time constraints of this forum, the core issues will not be covered in this paper.

Previously reported high bandwidth DRAMs use different external interfaces [2, 3, 4, 5]. Nitta's 1.6GB/s device used a 64b interface at 200MHz. Saeki relies on a 32b interface operating at 250MHz. Kushiyama and Yoo both report a 500Mb/s data rate per pin, Kushiyama reports a byte-wide interface and Yoo reports a 2-byte-wide interface. Kushiyama and Yoo use signaling on both edges of a system clock or strobe to double bandwidth. Kushiyama's device employs an on-chip PLL for precise clocking while Yoo relies on source synchronous clocking with a frequency-doubled data strobe for a data timing reference [6].

The incident wave switched bus similar to the one used by this device is described by Kushiyama. Open-drain current source drivers drive a single-ended parallel-terminated bus. Bus voltage swing is determined by the sink current of the drivers. The high dynamic output impedance of the current source drivers prevents reflected waves from reflecting off of an enabled output buffer.

For signaling rates beyond 600Mb/s/pin data-valid windows on the external bus are less than 1ns. Clock skew and clock jitter must be tightly controlled both at the system and component level. System level clock skew is topologically controlled by busing all signals so each has the same fanout, loading and path length. This requirement is incompatible with today's industry standard SDRAMs and modules which dictate a matrix interconnection topology (Figure 1).

Input buffers/receivers used at high data rates should exhibit small setup and hold time requirements, be tolerant of a wide common mode input range, and have low latency. The circuit shown in Figure 2, currently in use, meets these requirements, needs no bias currents, and integrates input signal latching.

The module approach used for such a bused arrangement of DRAMs is production-proven at 500Mb/s/pin in a high-volume consumer application [7]. With an increase of the number of signals to permit a 32b wide connection, the same electrical characteristics can be maintained for modules based on the new device. The connector system is fundamentally high-bandwidth due to the small impedance discontinuity it presents to the circuit.

Minimization of system jitter is critical to successful operation beyond 500Mb/s/pin rates. A system-level jitter budget must be established and take into account the expected system configuration extremes. The jitter budget must be apportioned over the system clock, the clock input amplifier/DLL path, and the on-chip clock distribution network (including clock buffers) and the data output drivers and data input receivers.

Current 600Mb/s/pin DRAMs use a system clock with approximately 150ps jitter (peak-peak). The clock must be brought onto the DRAM and controller chips with minimal delay and without adding significant jitter. Reported DLLs operate with 200ps jitter when used on a DRAM [8]. Under nominal conditions a device using this circuit in 0.38μm CMOS is demonstrated at 1.0GB/s over an 8b wide bus (Figure 3). Further scaling of device operating frequency requires reducing the system jitter. Circuits with significant jitter are external clock, on-chip DLL, on-chip clock routing, buffering, and I/O.

The clock input receiver on the DRAM uses a delay-locked loop to eliminate the input buffer delay. A key deficiency of the previously reported DLL, circuit implemenation-dependent bimodal jitter, is eliminated by use of a full frequency quadrature generator/phase interpolator rather than the half-frequency circuit of the predecessor (Figures 4, 5, 6).

The DLL also provides duty cycle correction to produce a 50% duty cycle clock on-chip. A 50% duty cycle on-chip clock is key to permit reliable signaling on both clock edges at high clock rates.

Variations in output current of an activated open-drain driver introduce jitter in the data output timing due to difference in the timing of the signal crossing the switching threshold. The devices reported in Reference 9 both employ output current regulation to minimize this effect.

Electrical properties of the packaging have a significant effect on DRAM performance. In particular, pin-pin matching is important. A detailed model of the package using electromagnetic modeling tools is used extensively in the bus simulations.

Current 16Mb DRAMs with 600MB/s throughput dissipate up to 1W when powered from a 3.3V power supply. Scaling the device to 2.5V operation is expected to reduce the power dissipation by approximately 30%. Due to the greater operating frequency and the wider organization of the device under development, it is expected to dissipate approximately 3.0W, approximately 40% consumed by the external interface.

Combination of the techniques described above is expected to result in approximately 30% improvement of current device jitter budget. A DRAM incorporating these improvements is expected to operate with 1.3Gb/s/pin signaling rate (650MHz clock rate) delivering 5.2GB/s from a 32b interface. Such a 64Mb density DRAM will exhibit a fill rate of 650times/s. Compared to an industry-standard 64M SDRAM operating at 66MHz with its 33times/s fill rate in a 2Mx32 organization, the ratio is 19.7:1.

0-7803-3721-2 / 97 / $5.00 / © IEEE

References: **See page 461.**

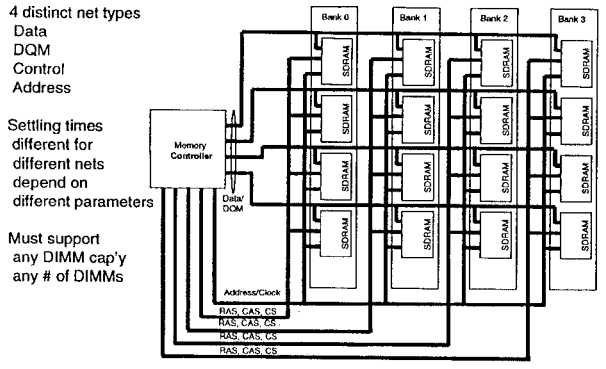

Figure 1: Typical SDRAM system topology.

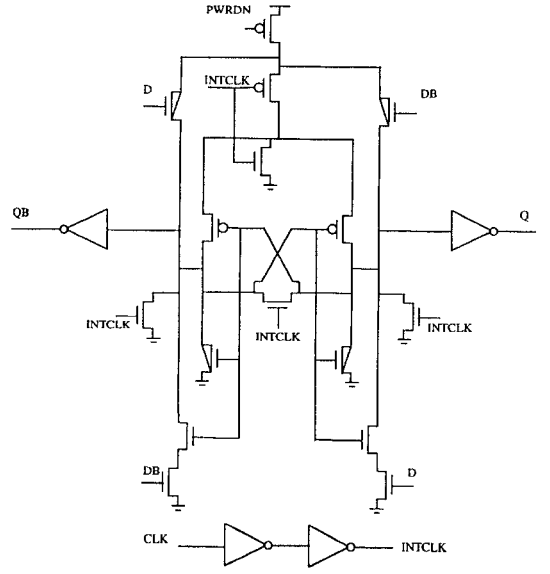

Figure 2: Input receiver.

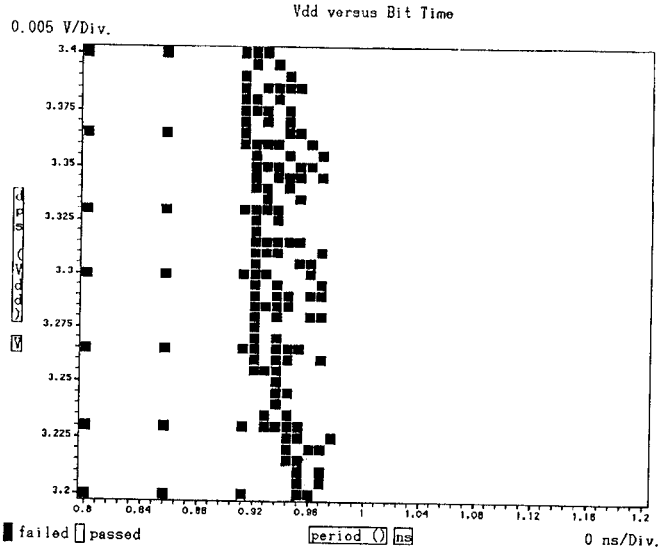

Figure 3: Shmoo showing 1GHz operation.

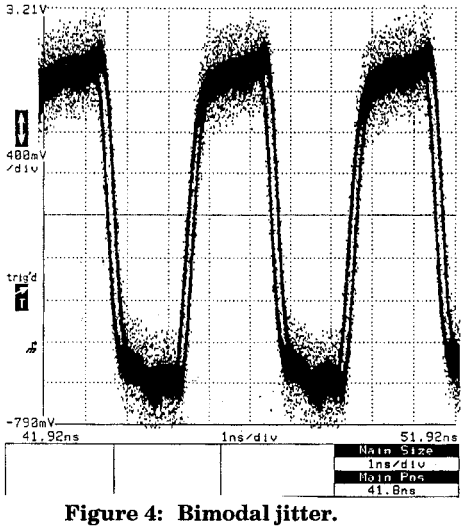

Figure 4: Bimodal jitter.

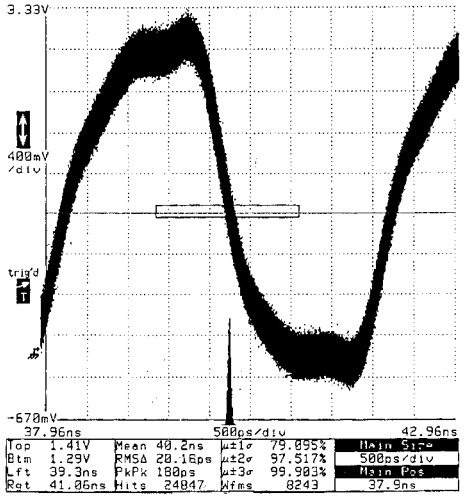

Figure 5: Eliminated bimodal jitter.

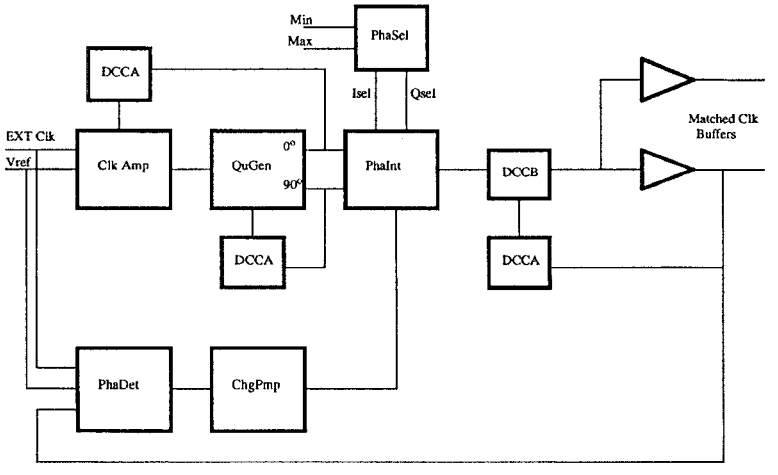

Figure 6: Improved DLL block diagram.

(Continued from page 221)

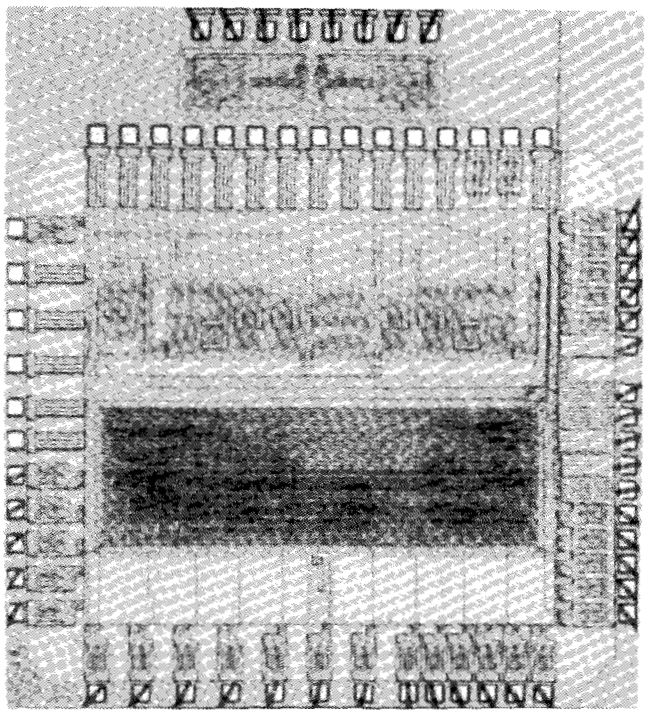

Figure 7: Test chip micrograph.

	AD1	AD2
Signal bandwidth	20-20000Hz	20-20000Hz
Sampling frequency	5.6448MHz	5.6448MHz
Oversampling ratio	128	128
Supply voltage	3.3V	3.3V
Max. input level	1Vrms	2Vrms
Dynamic range	96dB	101dB
THD (1kHz)	-104dB	-110dB
In-band tones	< -113dB	< -108dB
Power consumption	2.3mW	6.6mW
Aliasing	< -100dB	< -100dB
Chip area	0.4mm²	0.9mm²
Process	0.5µm, 2PS, 3AL, CMOS	

Table 1: Measured performance of two ΣΔ modulator versions.

FP 14.2: Development of Single-Chip Multi-GB/s DRAMs

(Continued from page 227)

References:

[1] Crisp, R., "Factors Limiting High Frequency SDRAM System Operation," Tutorial Overview, Rambus Inc. 1996.

[2] Kushiyama, N., et al., "A 500Mbytes/sec Data-Rate 4.5Mbit DRAM," IEEE Journal of Solid-State Circuits, vol. 28, no. 4, pp. 490-498, April, 1993.

[3] Yoo, J., et al., "A 32-Bank 1Gb DRAM with 1GB/s Bandwidth," ISSCC Digest of Technical Papers, pp. 378-379, Feb., 1996.

[4] Saeki, T., et al., "A 2.5ns Clock Access 250MHz 256Mb SDRAM with Synchronous Mirror Delay," ISSCC Digest of Technical Papers, pp. 374-375, Feb., 1996.

[5] Nitta, Y., et al., "A 1.6GB/s 1Gb SDRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture," ISSCC Digest of Technical Papers, pp. 376-377, Feb., 1996.

[6] Horowitz, M., et al., "PLL Design for a 500MB/s Interface," ISSCC Digest of Technical Papers, pp. 160-161, Feb., 1993.

[7] Nintendo 64 game console uses memory modules as described in the text.

[8] Lee, T., et al, "A 2.5V DLL for an 18Mb, 500MB/s DRAM," ISSCC Digest of Technical Papers, pp. 300-301, Feb., 1994.

[9] Donnelly, K., et al., "A 660MB/s Portable Interface Megacell in 0.3µm-0.7µm CMOS ASIC," ISSCC Digest of Technical Papers, pp. 290-291, Feb.,