11.5 A Time-Correlated Single-Photon-Counting Sensor with 14GS/s Histogramming Time-to-Digital Converter

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Time-correlated single photon counting (TCSPC) is a photon-efficient technique to record ultra-fast optical waveforms found in numerous applications such as time-of-flight (ToF) range measurement (LIDAR) [1], ToF 3D imaging [2], scanning optical microscopy [3], diffuse optical tomography (DOT) and Raman sensing [4]. Typical instrumentation consists of a pulsed laser source, a discrete detector such as an avalanche photodiode (APD) or photomultiplier tube (PMT), time-to-digital converter (TDC) card and a FPGA or PC to assemble and compute histograms of photon time stamps. Cost and size restrict the number of channels of TCSPC hardware. Having few detection and conversion channels, the technique is limited to processing optical waveforms with low intensity, with less than one returned photon per laser pulse, to avoid pile-up distortion [4]. However, many ultra-fast optical waveforms exhibit high dynamic range in the number of photons emitted per laser pulse. Examples are signals observed at close range in ToF with multiple reflections, diffuse reflected photons in DOT or local variations in fluorescent dye concentration in microscopy. This paper provides a single integrated chip that reduces conventional TCSPC pile-up mechanisms by an order of magnitude through ultra-parallel realizations of both photon detection and time-resolving hardware. A TDC architecture is presented which combines the two step iterated TCSPC process of time-code generation, followed by memory lookup, increment and write, into one parallel direct-to-histogram conversion. The sensor achieves 71.4ps resolution, over 18.85ns dynamic range, with 14GS/s throughput. The sensor can process 1.7Gphoton/s and generate 21k histograms/s (with 4.6µs readout time), each capturing a total of 1.7kphotons in a 1µs exposure.

Figure 11.5.1 provides a system overview consisting of a 32×32 single photon avalanche diode (SPAD) array, 1024-to-1 channel XOR timing combiner and histogramming TDC. The schematic of a SPAD pixel is shown consisting of a passively quenched SPAD, an 8T input buffer, a 17T toggle flip flop (TFF) and a 6T SRAM (not shown). The pixel with NIR-enhanced DNW to P- substrate SPAD is 21×21µm^2 pitch at 43% fill factor. The sensor region of interest (RoI) is programmed by writing to each pixel SRAM allowing high dark-noise pixels to be disconnected from the TDC input. Each SPAD event triggers the TFF encoding timing information on both edges of the pixel output using an asynchronous dual data-rate (DDR) approach. The output of each SPAD pixel in the array is combined into a single output through a timing-balanced cascaded XOR H-tree, consisting of a column-wise 5-stage cascaded XOR-tree using 8T single-ended XORs arranged between pixels in a vertically flattened tree with centrally tapped output. A single-ended to differential buffer is placed on each column output connecting into a fully differential horizontally flattened 5-stage XOR tree. The full 10-stage XOR tree is designed to have balanced timing from each pixel to the TDC input. The last XOR-tree output is toggled when any pixel in the array flips its state from a SPAD event.

Figure 11.5.2 illustrates the histogramming TDC consisting of 33-phase PLL, folded flash TDC front end, 8-stage data pipeline and 8 ripple counters per TDC phase which build the histogram. Each clock phase of the pseudo-differential VCO is coupled to a front end differential D-type Flip-Flop (DFF) in the TDC. The output of each front end DFF is logically XORed with its neighbour recording if a logical transition of the toggled output of the SPAD array occurs during the sampling window created by the temporal difference of the two clock phases. The input of the XOR in the last stage of the TDC front end is folded from the first, permitting continuous operation with no conversion dead zone and no converter dead time. The TDC conversion rate is the reciprocal of the time difference between successive clock phases. An 8-stage shift register is attached to each TDC front end output. Each shift register flip-flop represents a recorded timing event from 1 to 8 prior clock cycles. These are loaded out in parallel every 8 clock cycles to the synchronous first stage of the 16b ripple counters, each counter forming one bin of the time-domain histogram. The pipeline extends the converter dynamic range from 33 to 264 histogram bins. Each front-end 1b time quantizer, 8b shift register and 8 ripple counters are synchronous to their own clock, and independent of the other clock domains except for the links to and from the neighbouring XORs. The VCO is designed with an odd number of stages ensuring the converter is duty cycle insensitive using only positive clock edges. The PLL loop 8× divider matches the 1 to 8 duty cycle of the TDC synchronizing the laser output with the first histogram bin.

The PLL has a locking range of 44.3 to 53MHz corresponding to a bin width of 85.2 to 71.4ps. The measured integrated periodic RMS jitter of the PLL divider (laser synchronization output) in this range is 153.7 to 69.2ps respectively. For characterization, a PicoQuant FDL500 425nm pulsed laser was used as an optical source triggered by the sensor. An optical ToF sweep was performed to assess the TDC measurement range and the result is shown in Fig. 11.5.3. No conversion dead zone is observed. The timing mismatch of each pixel to the TDC front end is calculated at 280.8ps RMS, whilst the worst cases outliers are +938.2/-851.2ps. The converter linearity across the 33-phase front end was measured using the statistical code density test, activating SPADs under background light to create an uncorrelated input. The worst-case measured DNL is +0.75/-0.61 LSB and the maximum INL is +0.65/-0.2LSB (Fig. 11.5.3). The maximum mean operating frequency of the XOR tree was measured, under constant illumination recorded using the TDC, at 1.7Gphoton/s saturation by incrementally activating SPAD pixels. Figure 11.5.4 demonstrates this as the recorded mean number of SPAD events in a single shot capture or one laser repetition. To capture behavior showing no dead-time in the TDC conversion, two lasers are focused directly on the array with 1.4ns timing offset and both triggered simultaneously by the sensor. Figure 11.5.5 illustrates an example output from the sensor capturing two laser pulses against ambient light background. These two pulses separated by a short time interval mimic the fast dynamics in optical waveforms from scintillators, scattered light in time-domain spectroscopy or burst integrated fluorescence. This demonstrates that no distortion is present due to pile-up in the TDC, where a traditional TCSPC setup or TDC with converter dead-time would distort or not capture the second pulse profile. The power consumption of the XOR tree is optical intensity-dependent and the measured worst case was 16.1mW, the TDC front-end at 14.1mW and the PLL at 1.6mW.

Figure 11.5.6 presents this work in a comparative performance table against state-of-the-art TDC architectures, achieving the greatest conversion rate at the expense of power consumption. Although [6] is an oversampling TDC, it is included as it has the previously highest published single-channel conversion rate. Increasing the dynamic range of this architecture requires lengthening the shift registers and the addition of a counter per bin. The 2.4×1.7mm^2 device is manufactured in the STMicroelectronics 0.13µm 1P4M imaging CMOS and an annotated photomicrograph is shown in Fig. 11.5.7.

References:

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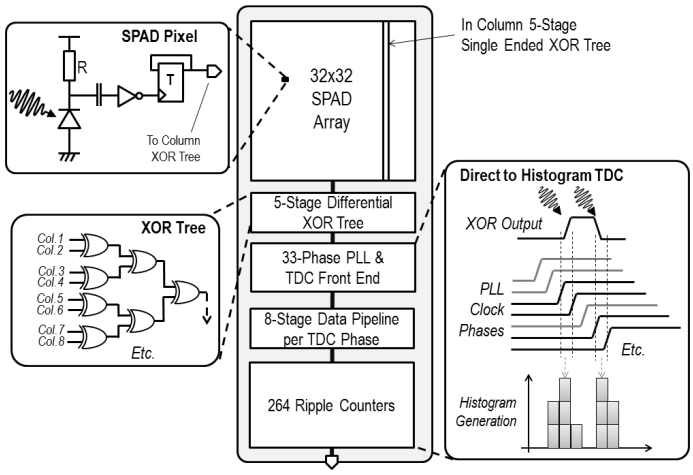

Figure 11.5.1: TCSPC sensor with histogramming TDC.

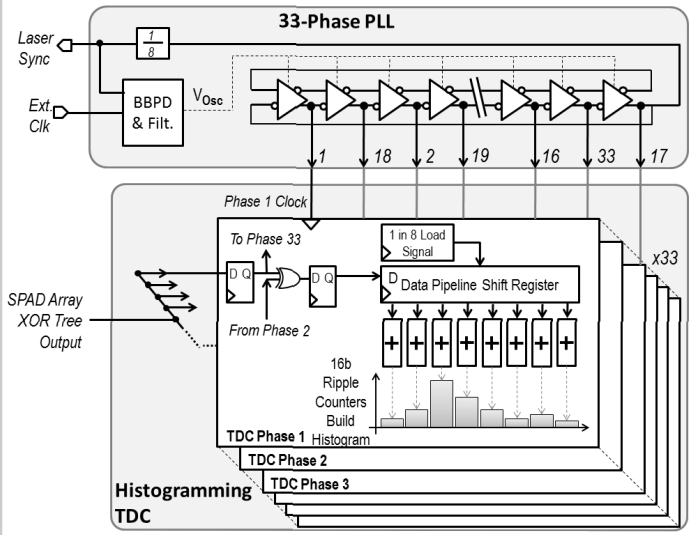

Figure 11.5.2: Block diagram of the TDC architecture.

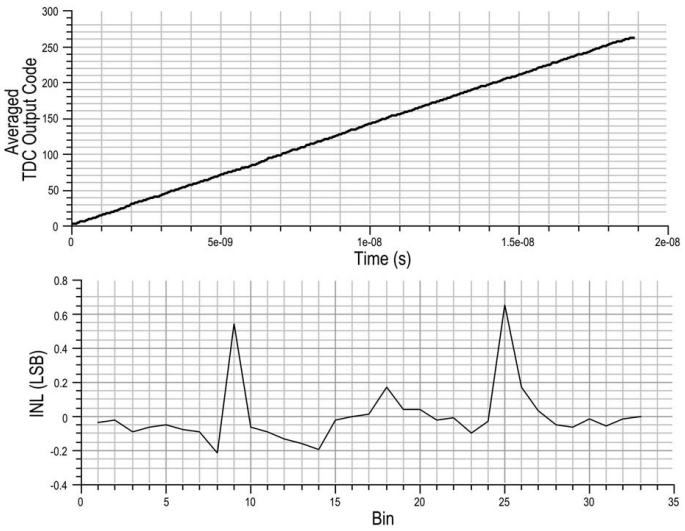

Figure 11.5.3: Optical ToF measurement showing mean TDC code versus time and INL of 33-phase TDC front end.

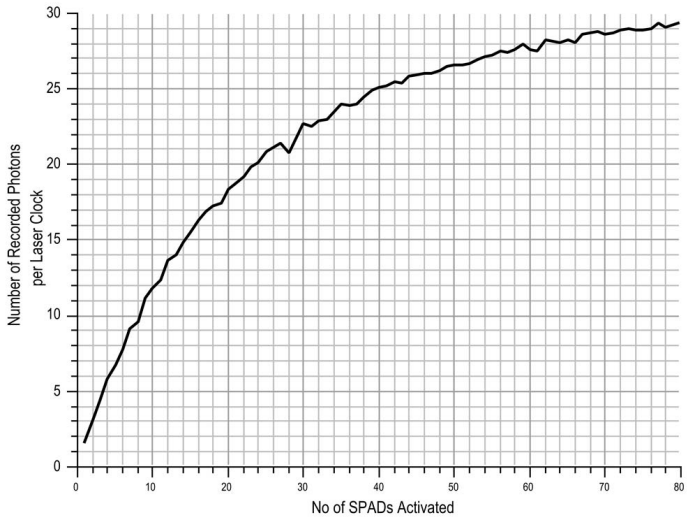

Figure 11.5.4: Recorded mean number of photons in a single shot capture (one laser repletion) versus number of SPADs enabled.

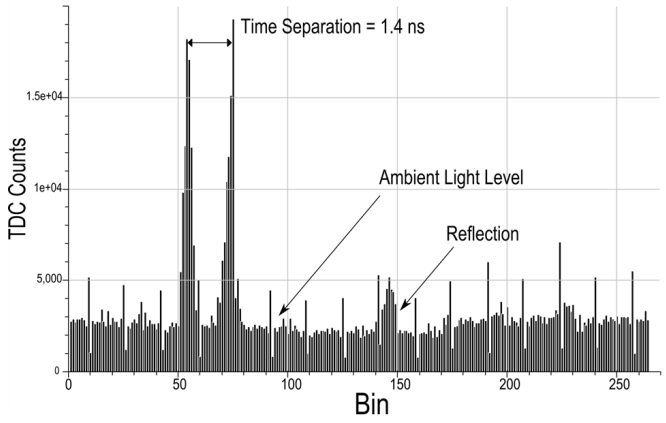

Figure 11.5.5: Histogram showing two laser pulses with 1.4ns separation. INL spikes are evident in the ambient/background level.

	This Work		[2]	[3]	[5]	[6]
Architecture	Histogramming 1ch Folded Flash TDC		Column Parallel Flash TDC	16ch Interleaved GRO-TDC	2ch Interleaved Vernier TDC	Oversampling 1ch SRO-TDC
Application	TCSPC		TCSPC	TCSPC	TCSPC	ADPLL
Tech.	130nm		180nm	130nm	130nm	90nm
Supply	1.2V		1.8V	1.2V	1.3V	1V
Conv. Rate	11.7GS/s	14GS/s	62.5MS/s	100MS/s	500MS/s	750MS/s
Delay Stage	85ps	71ps	208ps	52ps	31ps	156ps
Dyn. Range	22.5ns	18.8ns	853ns	3.6µs	2ns	2 to 840ns
Bit Width	8b		12b	16b	6b	13b
External Cal.	No		No	Yes	Yes	No
TDC Power	14.1 mW		***	1.8mW	1mW	2mW
TDC Area	0.03mm²*		0.02mm²**	0.04mm²	0.15mm²	0.02mm²

*Area of TDC Front End and Data Pipeline, **Estimated as Not Reported, *** Not Reported

Figure 11.5.6: TDC comparative performance summary table.

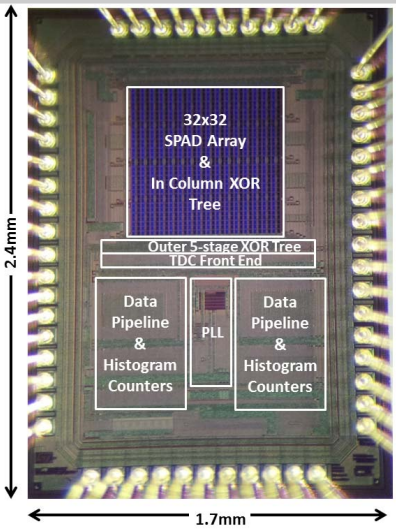

Figure 11.5.7: Annotated photomicrograph of the TCSPC sensor die in CPGA68 package.

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