A 0.7-3GHz Envelope ΔΣ Modulator Using Phase Modulated Carrier Clock for Multi-mode/band Switching Amplifiers

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***Abstract* — A 1-bit RF modulator using phase-modulated-carrier-clocking envelope ΔΣ modulation for a multi-mode/band transmitter is presented. The prototype IC designed in 90 nm CMOS process covers 2.4 GHz ISM and 3GPP frequency bands up to 3 GHz in conformity with IEEE 802.11g, W-CDMA and LTE in 5MHz-mode. The IC dissipates 8 mW for 1.95 GHz WCDMA and occupies 0.044 mm^2.**

***Index Terms* — CMOS, Delta-sigma modulation, switching amplifier, land mobile radio equipment, wireless LAN, radio transmitters.**

I. Introduction

A transmitter architecture using a class-D power amplifier (CDPA), which operates like a 1-bit digital-to-analog converter, is a promising candidate for fabricating multi-mode/band transceivers because it is highly blessed with the flexibility owing to the digital signal processing. In this architecture, a 1-bit pulse train that includes the desired RF signal is amplified to a specific level at the CDPA [1], [2]. A ΔΣ modulator is preferably used to generate a 1-bit signal from the multiple-bit baseband signal with a high signal-to-noise ratio (SNR) at the targeted band. The previous report [3] has described a 1-bit modulator for W-CDMA mobile terminals in which the quadrature baseband signal is ΔΣ-modulated with a sampling rate of 2 GHz for a carrier frequency of 1 GHz. However this architecture cannot cover the major 3GPP frequency bands with the sufficient bandwidth, e.g. 60 MHz for the 1.95 GHz band, because it uses the image band. To achieve the sufficient bandwidth, the ΔΣ modulator must operate at further higher sampling rates (typically 3.9 GHz for the 1.95 GHz band), which is extremely difficult to manage with the standard CMOS technology. Moreover, such a high-speed modulator must be designed using dynamic logic circuits, resulting in a significant amount of power consumption (more than 120 mW).

To fabricate a 1-bit modulator that covers the 2.4 GHz ISM and major 3GPP frequency bands with reasonable power consumption, we propose a transmitter architecture in which the 1-bit pulse train is generated by ΔΣ-modulating the envelope using the phase-modulated carrier (PM-carrier) clock. The sampling rate needed for ΔΣ-modulation becomes much lower in the proposed architecture, leading to further band extension and lower power consumption. In addition, the proposed architecture has the potential to significantly reduce switching losses at the following CDPA due to the zero-current switching (ZCS), the low average switching rate, and the low voltage operation owing to the high coding efficiency.

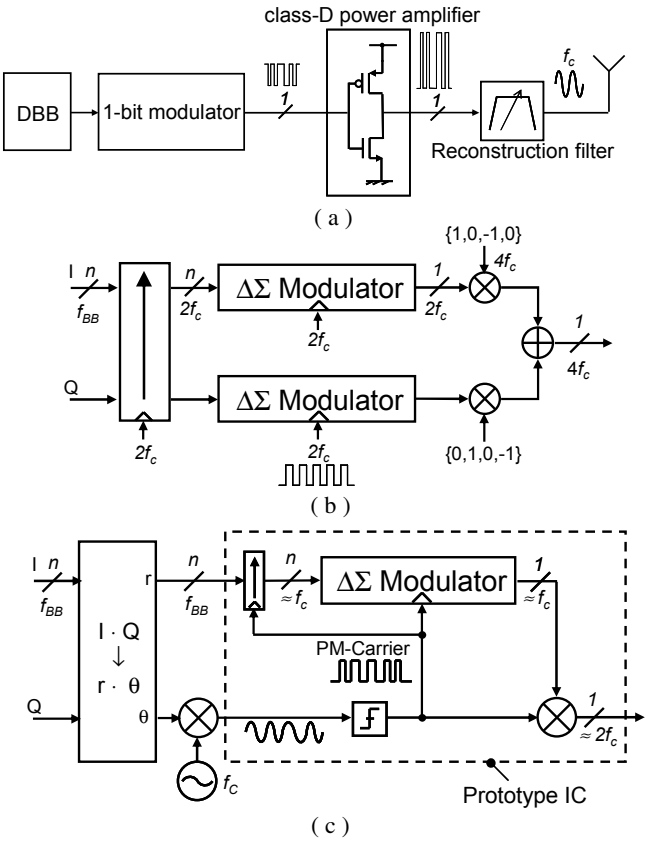

Fig.1 Block diagrams of the 1-bit transmitter (a) and constituent 1-bit modulators in the conventional (b) and proposed (c) architecture

II. Architecture

Figure 1 shows the block diagrams of the 1-bit transmitter (a) and the constituent 1-bit modulators using

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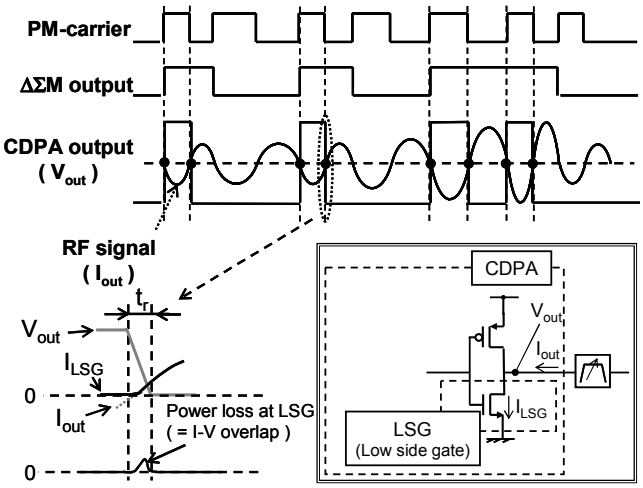
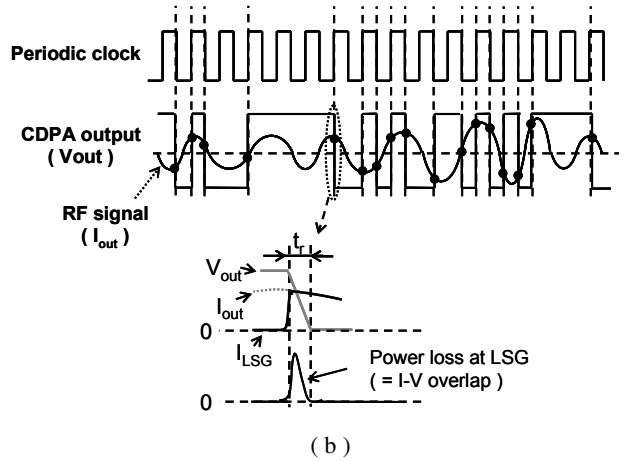
the conventional quadrature ΔΣ modulation (QDSM) (b) and the proposed envelope-ΔΣ-modulation using phase-modulated carrier clock (PMC-EDSM) (c). While the PMC-EDSM architecture is similar to the envelope ΔΣ-modulation (EDSM) architecture [4], the PMC-EDSM architecture primarily features the envelope ΔΣ-modulation clocked by the PM-carrier. In the PMC-EDSM architecture, the phase information is represented by the pulse positions in the 1-bit pulse train, which is generated by synchronously multiplying the ΔΣ-modulated envelope and the PM-carrier. Thus, the PMC-EDSM architecture realizes the higher SNR because the phase information preserves as a pure analog signal with no quantization noise.

Though the power loss at the CDPA following the modulator is ideally zero, in practice it is not so small due to the effect of parasitic elements attached to the switching devices in the CDPA. One of the primary origins of the power loss comes from the overlap of voltage and current waveforms (I-V overlap) across the switching devices during the transition. The ZCS means that the I-V overlap is significantly reduced. Figure 2(a) shows the mechanism of the ZCS at the following CDPA in PMC-EDSM with the voltage and current waveforms at the CDPA output node. The PMC-EDSM architecture ensures that the rising/falling edges in the 1-bit pulse train occur only when the phase of the PM-carrier is zero/π, respectively. This indicates that the output current of the CDPA is always nearly zero during the transition. On the other hand, this is not always satisfied in the QDSM architecture as shown in Fig. 2(b).



(a)



(b)

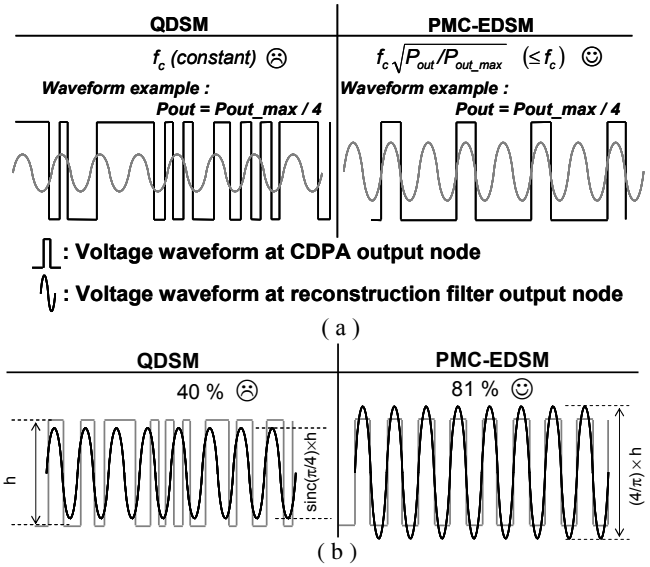
Fig.2 Waveforms at CDPA output node for the PMC-EDSM architecture (a) and the QDSM architecture (b)

Another origin of the power loss at the CDPA is the charge/discharge cycle process onto the parasitic output capacitor in which the power loss is proportional to the switching rate. Figure 3(a) shows the average switching rate with the voltage waveforms at CDPA and filter output nodes. In the PMC-EDSM architecture, the average switching rate, f_r, is decreased with the smaller output power, P_{out}, on the basis of the equation

$$f_r = f_c \sqrt{P_{out} / P_{out\_max}} \quad (1)$$

where f_c, and P_{out_max} are respectively the carrier frequency and the maximum output power. On the other hand, it is always equal to the carrier frequency in the QDSM architecture regardless of power levels.

The coding efficiency (η_C) is defined as the reconstructed signal power ratio to the total power of the pulse train [5]. When the η_C is higher, the required pulse train power can be lower for the same power level. Considering that the supply voltage of the CDPA is

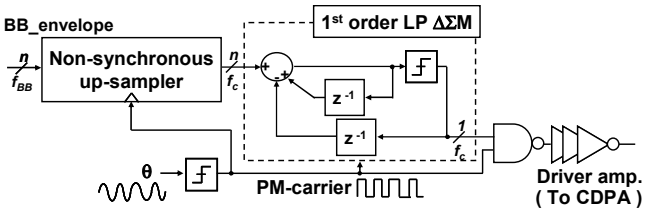


(a)

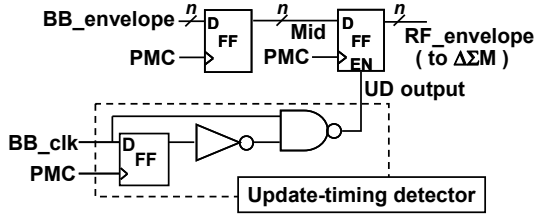
(b)

Fig.3 CDPA performance comparison for averaging switching rate (a) and coding efficiency at maximum output power (b)

proportional to the square root of the pulse train power, the higher η_C enables the lower supply voltage operation of the CDPA, resulting in less switching loss onto the parasitic capacitors. Figure 3(b) shows the η_C at the maximum output power in the both architectures. In the PMC-EDSM architecture, the pulse train is identical to the PM-carrier and thereby the envelope is $4/\pi$ times larger than half the pulse height, corresponding to η_C of 81 %. In the QDSM architecture, the envelope cannot exceed the pulse height since the pulse signal is not synchronous with the reconstructed signal, which is seen as the filter output signal in Fig. 3(b). In addition, sinc filtering due to aperture effect at the CDPA further decreases the coding efficiency, resulting in maximum η_C of 40 %.



(a)



(b)

Fig.4 Circuit diagrams of prototype IC (a) and constituent non-synchronous up-sampler (b)

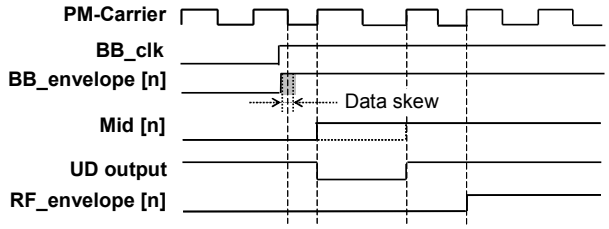


Fig.5 Timing chart for non-synchronous up-sampler

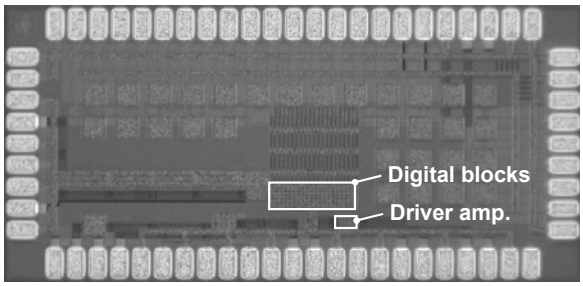
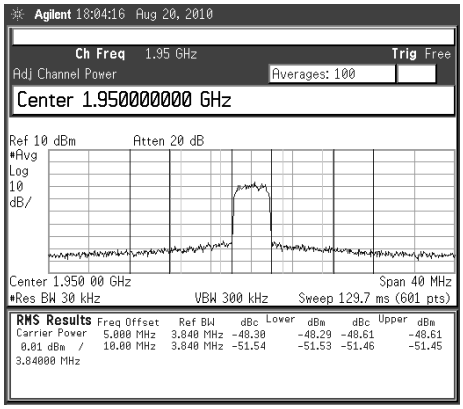


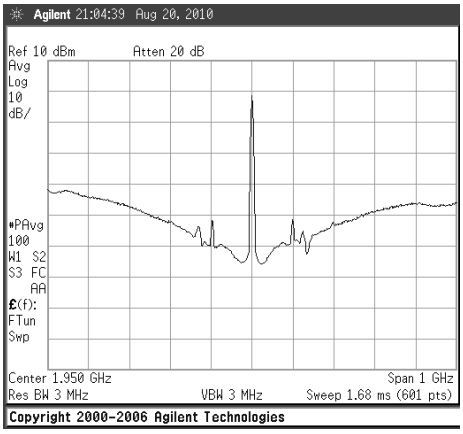
Fig.6 Microphotograph of the prototype IC die

III. Circuit Design

To evaluate the 1-bit modulator in the PMC-EDSM architecture, we designed a prototype IC that includes the blocks outlined by the dotted line in Fig. 1(c). The detailed block diagram is shown in Fig. 4(a). The multiple-bit digital envelope is up-sampled from the baseband clock rate to the PM-carrier at the non-synchronous up-sampler and then fed to the ΔΣ modulator with the two-level (1/0)



(a)



(b)

Fig.7 Measured output spectra for 1.95 GHz W-CDMA in a close-in view (a) and an expanded view (b)

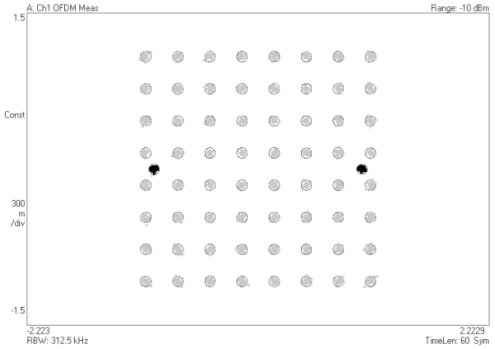


Fig.8 Measured constellation for 2.4 GHz WLAN 64-QAM/OFDM

TABLE I
PERFORMANCE SUMMARY

Mode	WLAN (802.11g)	WCDMA uplink					LTE uplink (Ch. BW = 5MHz)				
$f_{carrier}$ (GHz)	2.4	0.7	0.835	1.95	2.57	3	0.7	0.835	1.95	2.57	3
ACLR (dB) at 5MHz offset	-	44.6	41.9	48.3	47.4	45.6	36.7	37.5	43.4	40.6	35.8
ACLR (dB) at 10MHz offset	-	47.5	49.7	51.5	51.0	50.2	43.3	42.8	49.1	48.0	39.6
EVM (%) including residual errors	2.5	1.1	1.5	1.0	0.84	(Not Measured)					
Supply voltage of DSM (V)	1.0	1.0	1.0	1.0	1.2	1.3	1.0	1.0	1.0	1.2	1.3
Power of DSM (mW)	9.5	3.2	3.7	8.0	14	19	3.0	3.5	7.8	14.4	21
Drain eff. (%) of the final stage	7.8	28.0	27.0	24.8	14.3	12.5	18.8	16.5	18.4	10.0	7.4

quantization. The NAND is used to multiply the ΔΣ-modulated envelope and the PM-carrier. The driver amplifier consisting of cascaded inverters, which can also be regarded as the class-D amplifier, was designed to drive the following CDPA. The non-synchronous up-sampler as shown in Fig. 4(b) consists of an update-timing detector (UD) and two cascaded delayed flip-flops (DFF). When a rising edge of the baseband clock arrives, the UD forces the second DFF to postpone the update timing for a clock period, as shown in the timing chart of Fig. 5. This means that transmission errors due to data skew are completely avoided. Thanks to the PMC-architecture, the 1st-order ΔΣ modulator can be used to meet the specification for the 3GPP standards. For gigahertz operation, the borrow-save redundant arithmetic is applied to the adder for carry-free operation and sign determination using only the upper four bits is applied to the quantizer to lower the carry propagation delay [3]. Figure 6 shows a die photograph of the prototype IC fabricated in 90 nm CMOS process. The occupied area for the digital blocks is as small as 0.044 mm^2.

IV. Measurement

The measured output spectra for the W-CDMA HPSK signal in the 1.95GHz band are shown in Fig. 7. The adjacent channel leakage ratios (ACLR) at 5 and 10 MHz-offset for the WCDMA signal were respectively more than 48.3 and 51.5 dB without any linearization techniques as shown in (a), which are better than those of other work using multi-bit ΔΣ modulation [6]. The bandwidth in which the noise floor is less than -50 dBc is over 100 MHz as shown in (b). The power consumption is as small as 8.0 mW under the supply voltage of 1V. The drain efficiency of the final stage in the driver amplifier is 24.8 %. The measured constellation for the WLAN 802.11g OFDM/64-QAM signal in the 2.4 GHz band is shown in Fig. 8. The EVM including residual errors for WLAN was 2.5 %. The performance of the 2.4GHz ISM and the 3GPP frequency bands is summarized in Table I. The prototype IC can cover the 2.4 GHz ISM and the 3GPP frequency bands up to 3 GHz in conformity with IEEE 802.11g, W-CDMA and LTE in 5MHz-mode.

V. Conclusion

The proposed architecture proves able to provide a 1-bit sequence for the switching amplifier, covering the 3GPP bands up to 3 GHz and the 2.4 GHz ISM band in conformity with IEEE 802.11g, W-CDMA and LTE in 5MHz-mode. The prototype modulator has the power consumption of 8 mW for 1.95 GHz WCDMA and die area of 0.044 mm^2. In addition, the proposed architecture has the potential to significantly reduce switching losses at the following CDPA due to the zero-current switching, the low average switching rate, and the low voltage operation owing to the high coding efficiency.

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