Reliability Challenges for the 10nm Node and Beyond

James H. Stathis[1,a], M. Wang[1,b], R.G. Southwick[1,b], E.Y. Wu[2,c], B.P Linder[1,a], E.G. Liniger[1,a], G. Bonilla[1,a], H. Kothari[3,b]

[1]IBM Research, [2]IBM Microelectronics, & [3]STMicroelectronics
[a]Yorktown Heights, NY, [b]Albany Nanotechnology Center Albany, NY, and [c]Essex Junction, VT

Abstract

Technology elements for the 10nm node and beyond include FINFETs on bulk or SOI, replacement gate process, multi-workfunction gate stacks, self-aligned contacts, and alternative channel materials. This paper describes current trends and how improved physics understanding and models can enable us to anticipate the effects of scaling on reliability even in early stages of development.

Introduction

New device structures and materials, coupled with aggressive gate and metallization pitch scaling for integration density, give rise to significant new challenges in reliability characterization and modeling. Technology elements for the 10nm node and beyond include FINFETs formed on either bulk or SOI [1], replacement gate process flow, multi-workfunction (WF) gate stacks, self-aligned contacts (SAC), and potentially alternative channel materials such as III-V and SiGe [2,3].

Voltage and Tinv Scaling

Electrical thickness (T_{inv}) scaling for improving performance will require reduced operation voltage in order to maintain equivalent reliability. Using the observed voltage and thickness dependence, Fig. 1 shows the voltage reduction requirement for interfacial layer (IL) scaling [4]. The 2013 ITRS roadmap anticipates sufficient voltage reduction to contain the expected impact on nFet T_{inv} scaling, but NBTI

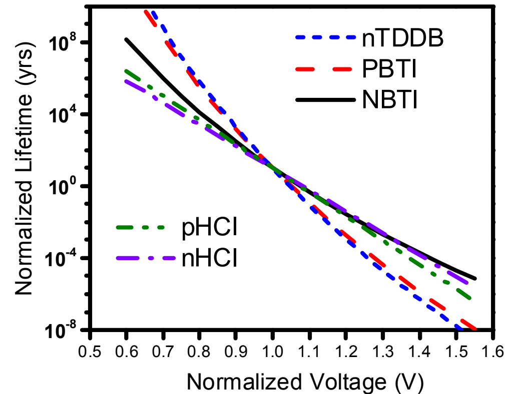


Fig. 2. Voltage dependent normalized lifetime for transistor FEOL reliability modes.

will limit pFet scaling unless new materials such SiGe channel devices are adopted [5]. The voltage dependence of hot carrier injection (HCI) lifetime for mid-Vg stress condition (i.e, Vg=½Vd+Vt) is weaker than for other mechanisms (TDDB or BTI) as shown in Fig. 2. Thus, as Vdd is reduced, the lifetime associated with HCI will increase by a lesser amount and HCI could become a larger contribution to the total degradation at end of life.

Pitch Scaling

Density is now one of the main drivers of scaling, and the spacing between the gate and the self-aligned S/D contact

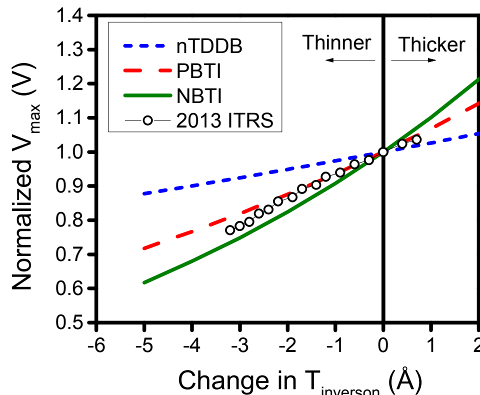


Fig. 1. Trend of maximum operation voltage V_{max} for constant reliability for the three major gate dielectric failure modes, and ITRS roadmap trend for Vdd and EOT scaling from 10nm node.

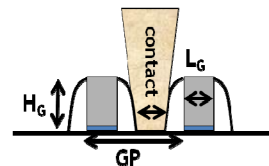


Fig. 3. Schematic of gate and contact geometry scaling.

TABLE I
GATE AND CONTACT GEOMETRY SCALING

Node	Gate Pitch	Gate Length	Contact	Best case Spacer
32	120-130	30-35	30-40	25-30
22-14	80-100	25-30	20	18-25
10	65-75	20-23	20	12-16
7	45-55	12-18	15	9-12
5	35-45	9-16	12	7-9
3?	25-35	7-12	<12?	3-6?

All dimensions in nm. Best case spacer dimension (GP-LG-Contact)/2 reflects ideal case without contact taper.

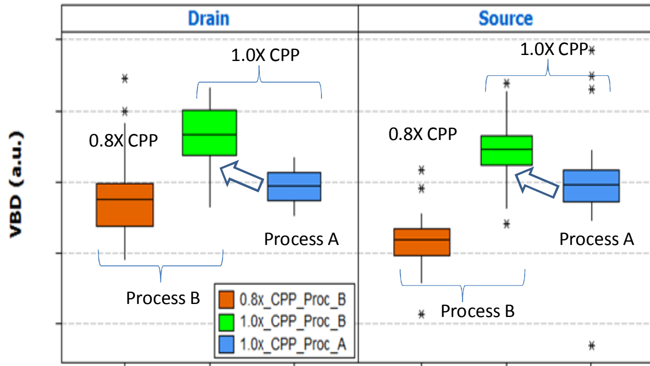


Fig. 4 . Breakdown voltage between gate metal and self-aligned S/D contact with scaled gate pitch at L_{gate}=20nm.

will become less than 10nm (Fig. 3 and Table I) which is comparable to the gate dielectric thickness in early CMOS technology. Thus, the intrinsic as well as extrinsic reliability of the gate sidewall spacer will become increasingly important. Fig. 4 shows that good gate-to-contact breakdown voltage can be achieved in scaled pitch structures. Adoption of low-k (compared to Si_3N_4) spacer material is needed to maintain low contact capacitance. Voltage acceleration [6] and Weibull slope (Fig. 5) of low-k spacer material are comparable to Si_3N_4. Intrinsic max Vdd exceeds 1V for

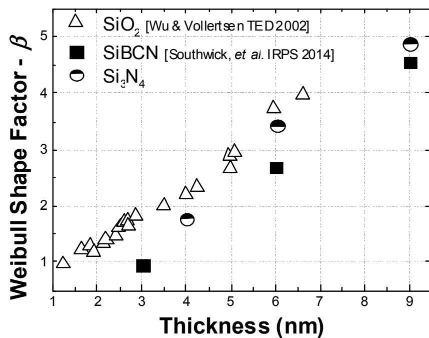


Fig. 5. Weibull slope as a function of thickness for SiO_2 and various sidewall spacer materials.

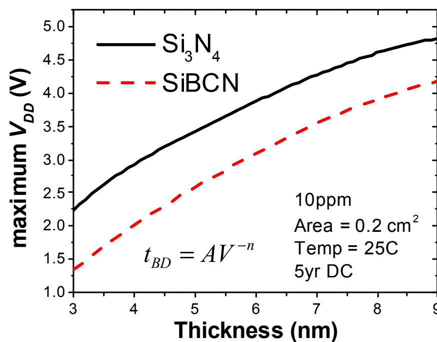


Fig. 6. Projected intrinsic Vdd_max for sidewall materials, using power law voltage acceleration.

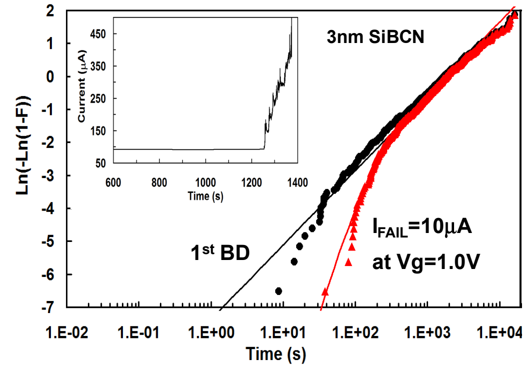


Fig. 7. First breakdown distribution and failure distribution (I_{Fail}=10μA) including progressive breakdown in SiBCN. Inset: Example of progressive BD in SiBCN.

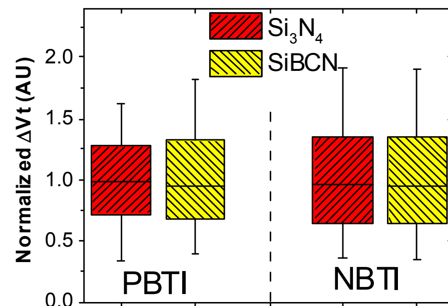


Fig. 8. Measured NBTI and PBTI are unaffected by spacer material in RMG FinFET.

anticipated thickness, and using power law voltage model gives more margin compared to $\sqrt{E}$ model (Fig. 6). As shown in Fig. 7, additional margin is obtained from progressive breakdown similar to gate dielectrics. Fig. 8 shows that the change from Si_3N_4 to SiBCN spacer material does not impact transistor BTI reliability.

Fin Geometry

The use of fully-depleted FinFETs has given rise to several new reliability considerations, including [110] interface orientation, increased self-heating during accelerated stress [7], and new solutions for Vt tuning and junction optimization [1]. At matched Vt (by metal workfunction tuning), undoped fins offer significant PBTI advantage over doped planar FET, as shown in Fig. 9 [8]. Multi-Vt devices with equivalent reliability can be obtained by process optimization as shown in Fig. 10 [1]. The sidewall (110) orientation reduces the FinFET advantage for pFET NBTI, and also for HCI damage. Reducing the fin thickness also increases HCI due to increased carrier capture cross section [7].

Without channel doping and with reduced thermal budget, control of the junction profile becomes more difficult and

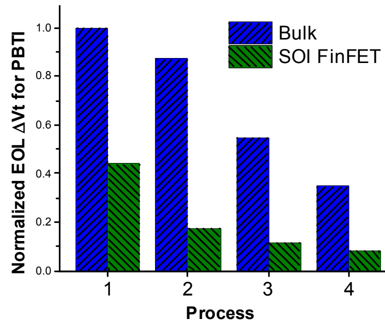


Fig. 9. Measured PBTI is up to 4x lower in SOI FinFET compared to bulk device at constant overdrive (Vg- Vt) for various dielectric stacks. After Wang *et al.*, EDL 2013.

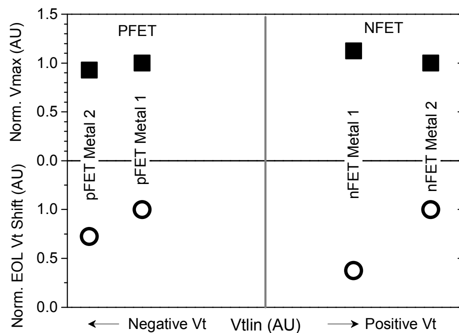


Fig. 10. Comparable TDDB (top) and BTI (bottom) reliability is achieved with multi-Vt stacks.

underlapped devices become more sensitive to HCI degradation (Fig. 11a), with HCI degradation more localized at the drain for underlapped devices (Fig. 11b). As shown in Fig. 12, the Id degradation sensed at high Vg overdrive with linear drain bias, i.e. ΔIdlin with Vg=Vdd and Vd=0.05V (and corresponding to ΔVt_idlin) is more sensitive to resistance or mobility degradation, including Rsd increase from defects generated in the spacer region, compared to Vt shift sensed at Vg near threshold (ΔVtlin). As gate stress voltage increases, from just above Vt toward Vd, the

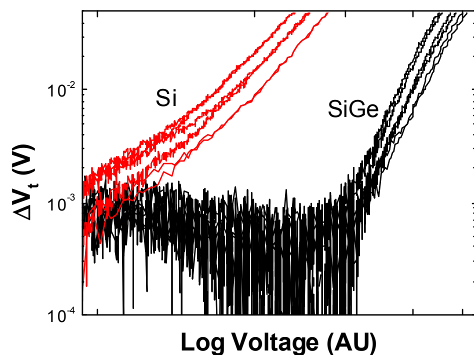
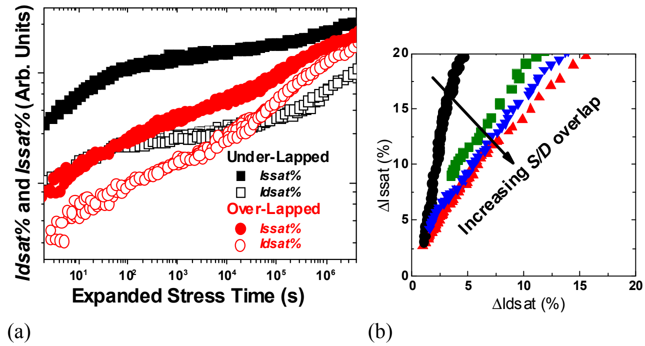


Fig. 13. Ramp BTI data for SiGe pFET compared to Si pFET.



(a) (b)

Fig. 11. (a) Forward (Id) and reverse (Is) current degradation by HCI. (b) Underlapped devices show larger ratio of reverse/forward degradation implying more localized damage close to drain.

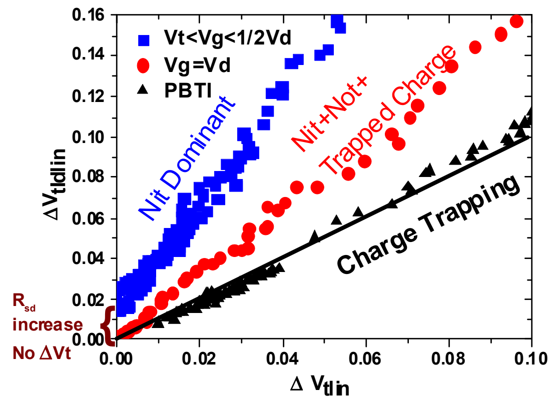


Fig. 12. ΔVt_idlin is the shift extracted by constant current method from Idlin measured near Vg=Vdd with Vd=0.05V. For charge trapping (no Rsd increase or mobility decrease), ΔVt_idlin = ΔVtlin. Dit (mobility degradation) leads to increased ΔVt_idlin. Rsd increase alone causes ΔVt_idlin without Vtlin change.

degradation mode changes from Nit dominant (mobility degradation) to trapped charge dominant (Vt shift).

New substrate materials

The search for higher performance in addition to density scaling is driving exploratory work on Si replacements. SiGe pFET channel was first introduced as a Vt adjustment element and was found to have greatly improved NBTI [5], as demonstrated in Fig. 13. Higher Ge content and/or III-V materials may be used in future for higher performance, with IL optimization key to realizing the full potential of the alternate channel material.

Variability

As dimension scaling and process complexity increase, variability inevitably becomes worse. Vt and BTI variability are well known issues, but the impact of variability on breakdown is not as well appreciated. Process non-uniformity

makes the measured breakdown distributions broader, leading to overly conservative lifetime projection, and fundamentally invalidates the assumption of Poisson statistics that underlies the usual area-scaling relation for failure rate, $F_2=1-(1-F_1)^{(A2/A1)}$. Local variation can be separated from cross-wafer variation by extensive cross-wafer and within die measurements [9], and non-Poisson area scaling can be efficiently modeled using a defect clustering model [10] as shown in Fig. 14. With this approach, the low percentile failure times can be obtained even in the presence of multiple unknown sources of random variation.

Interconnect

The introduction of ultra-low k materials to reduce capacitance, and the selection of barrier materials, metal alloys, and metal capping layers required to meet resistance targets at finer pitches (<50nm) in scaled interconnect structures entail a significant increase in integration complexity and reliability challenges, due to degraded thermo-mechanical properties and lower dielectric breakdown strength. This drives a need to evaluate failure mechanisms in these heterogeneous structures at lower voltages, closer to operating conditions. Long-term studies (Fig. 15) show that the canonical $\sqrt{E}$ acceleration model is overly conservative for predicting TDDB lifetime [11]. Dense wiring in SRAM cells is a potential vulnerable location for BEOL breakdown. Typical cell layouts have wordlines (WL) passing over Vdd, closely spaced metal lines between bitlines (BL) and ground, and sometimes bitlines crossing over the internal node connection. Breakdowns at these locations (Fig. 16) affect the cell differently than transistor gate breakdown within the cell. Sensitivity to breakdown-induced leakage between WL and Vdd, or BL and Gnd, will depend on sense amp design. Careful attention to voltage acceleration and progressive breakdown is required to model the impact of BEOL breakdown.

Acknowledgements: We thank Terry Hook, Geordie Braceras, and Ed Cartier for insights. This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

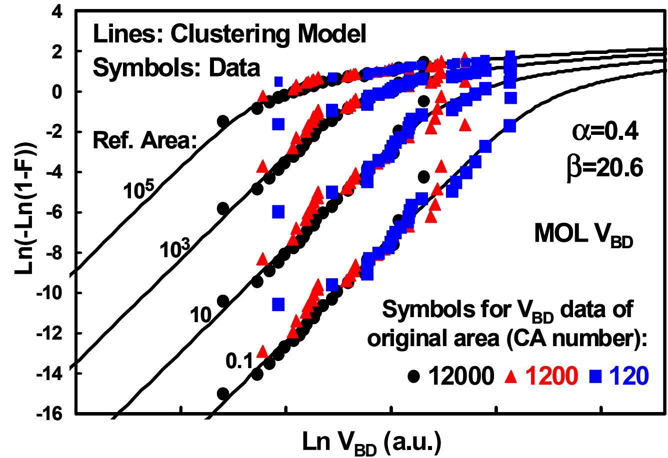


Fig. 14. Breakdown voltage data for gate-to-contact (PC-CA) showing non-Poisson area scaling and excellent agreement with clustering model at various reference areas. After E.Wu *et al.*, IRPS 2014.

References

[1] K.-I. Seo *et al.*, VLSI-Technology 2014.
[2] P. Hashemi *et al.*, VLSI-Technology 2013, p. T18-T19.
[3] Y. Sun *et al.*, IEDM 2013, p. 48; R.T.P. Lee *et al.*, IEDM 2013, p. 44.
[4] B.P. Linder *et al.*, VLSI-DAT 2013.
[5] J. Franco *et al.*, IEDM 2011, p.445; S. Krishnan *et al.*, IEDM 2011, p. 634.
[6] R.G. Southwick *et al.*, IRPS 2014.
[7] S. Ramey *et al.*, IRPS 2013, 4C.5.1-4C.5.5.
[8] M.Wang *et al.*, Electron Dev. Lett. 34, p. 837-839, 2013.
[9] F. Chen *et al.*, IRPS 2014.
[10] E. Wu *et al.*, Appl. Phys. Lett 103, 152907, 2013, IEDM 2013, p. 401; R. Achanta *et al.*, IITC 2014; E.Wu *et al.*, IRPS 2014; E.Wu *et al.*, IEDM 2014.
[11] E. Liniger *et al.*, IRPS 2014.

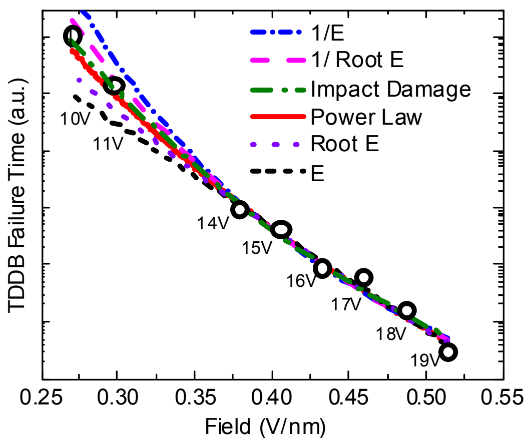


Fig. 16. Voltage dependence of BEOL dielectric breakdown (after Liniger IRPS 2014). Data lie between E and 1/E models.

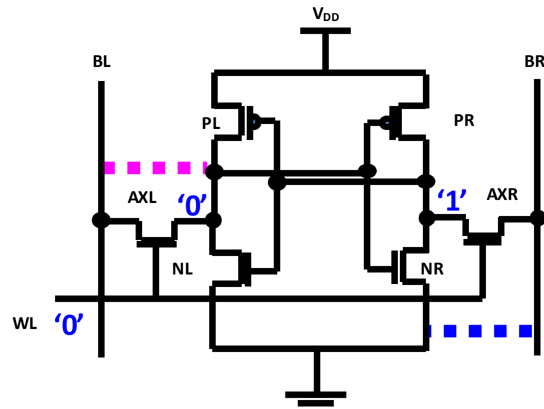


Fig. 16. Inter- and intra-metal level vulnerabilities in typical SRAM cell layout include bitline to node or to gnd, and Vdd to wordline (not shown).