An Integrated 33.5dBm Linear 2.4GHz Power Amplifier in 65nm CMOS for WLAN Applications

Ali Afsahi[1,2], Lawrence E. Larson[1]

[1]Center for Wireless Communications, University of California, San Diego, La Jolla, CA 92093

[2]Broadcom Corp., San Diego, CA 92127

Abstract **— *An* integrated linear 2.4GHz CMOS power amplifier is presented. With a 3.3v supply, the PA produces a saturated output power of 33.5dBm with peak drain and power-added efficiencies of 44.2% and 37.6%, respectively and has 40dB small-signal gain. By utilizing gm-linearization and digital pre-distortion, an EVM of -25dB is achieved at 26.4dBm with 22% PAE while transmitting 54Mbs OFDM. The chip is fabricated in standard 65nm CMOS and packaged in a 40-pin QFN package. The PA occupies 2.2mm^2 active area.**

Index Terms **-- CMOS, Power Amplifier, WLAN, OFDM, Linearization, Power Combiner**

I. INTRODUCTION

Silicon-based approaches for linear RF power amplifiers are becoming increasingly common. These designs usually rely on advanced circuit techniques to overcome some of the intrinsic limitations of silicon technology. Both linearity enhancement [1-2] and efficiency enhancement techniques [3] are needed in order to meet the demanding performance requirements of the modern wireless environment. In particular, the recent trend in the 802.11 OFDM environments is towards complete System-on-Chip (SOC) approaches, where multiple power amplifiers are placed on a single die to address multiple frequency bands and MIMO applications. This paper describes some improved design techniques to realize high power, high efficiency and linear power amplifiers in a standard 65nm CMOS technology for 802.11 OFDM applications.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows a simplified schematic of a class AB CMOS power amplifier using a cascode structure. Typically, the thick gate oxide transistor is used as a cascode device to increase the reliability of the PA and to use a higher supply voltage. The 3.3v supply limit makes the design of watt-level PAs very challenging in CMOS. For example, in Fig. 1, in order to deliver 32dBm saturated power to the antenna, we need to transfer the 50Ω load to ~3Ω. But this approach has three major drawbacks. First, the loss of any finite-Q matching network increases as a function of impedance transformation ratio [4]. Second, the loss of the matching network is more sensitive to layout parasitics. For example, if there is a 1Ω parasitic resistor in series with *C* in Fig. 2(a), the loss increases from 0.4dB to 1.7dB when the R_L reduces from 10Ω to 3Ω. And third, the PA input device needs to be very large to provide the required current to such a small load. A larger device results in a larger device parasitic capacitance, which makes the design of the PA driver very difficult and inefficient. For instance, simulation results of the circuit of Fig. 1 show the input and output capacitances excluding the layout parasitics are, 9pF (C_{par1}) and 13pF (C_{par2}), respectively for a 3Ω load impedance. The output capacitance is larger due to use of the thick gate oxide cascode device.

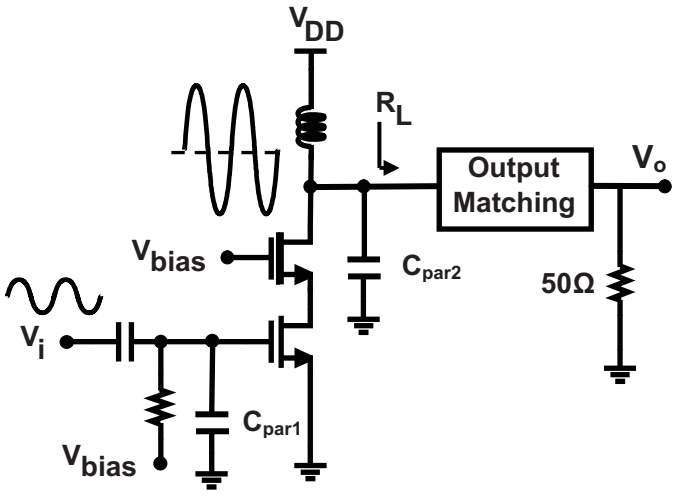

Fig. 1. Simplified schematic of typical class AB power amplifier.

One possible solution is to combine the output power of multiple smaller PAs, where each PA is presented with a higher impedance and can then have a more efficient, higher gain driver. In this solution the power combining network needs to be low loss. Recently, there has been a significant effort to use different power combining architectures to generate high output power in CMOS [4-7]. Fig. 2 shows the resonant LC and transformer matching networks, which can be used for narrow-band power amplifiers. In both cases, the 50Ω load is transformed to 50/k^{2}Ω. It can be shown that the transformers store less energy in the inductance for a given transformation ratio compared to an *LC* matching network, which results in lower loss for a given *Q* [4].

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

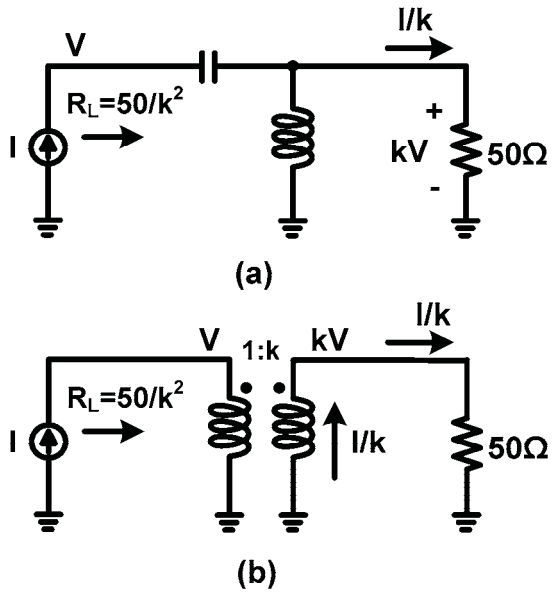

Fig. 2. (a) LC matching network. (b) Transformer matching network.

In [4-6], the authors have used a voltage-mode transformer-based power combiner (Fig. 3), where the secondary (antenna side) coils of *n* transformers are connected in series and their primaries are driven by separate amplifiers; the AC voltages add on the secondary side, generating higher output power. The advantage is that the impedance that each PA sees is *n* times larger, which relaxes the design of the driver and also reduces the sensitivity to layout parasitics. In this approach, depending on the implementation, all the primary ports may not be symmetric with respect to the secondary ports which can introduce amplitude and phase mismatch, which worsens at higher frequency. This mismatch can reduce the maximum output power and efficiency of the power amplifier [5-6].

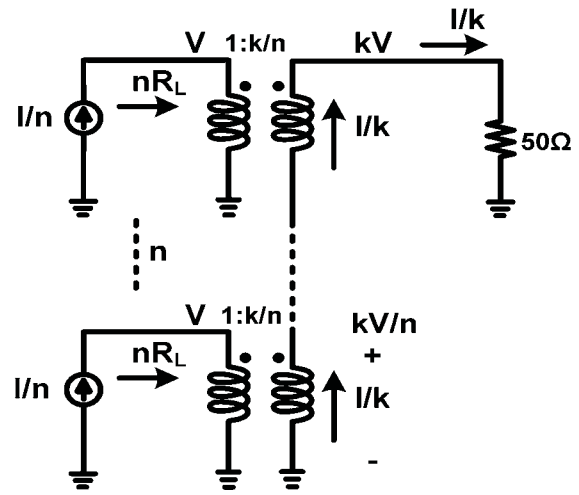

Fig. 3. Voltage-mode transformer-based power combiner.

In [7], a distributed LC combiner (Fig. 4), is used which transfers 50Ω to a lower impedance at the output of each PA. The problem with this approach is that the layout routing parasitic resistances are at the side where the impedance is low, and this can increase the overall loss of the combiner. It can be shown that (Fig. 2(a)) if the parasitic resistance moves to the side where the impedance is 50Ω, the loss reduces from 1.7dB to 0.2dB for the case of 1Ω parasitic resistance and R_L=3Ω.

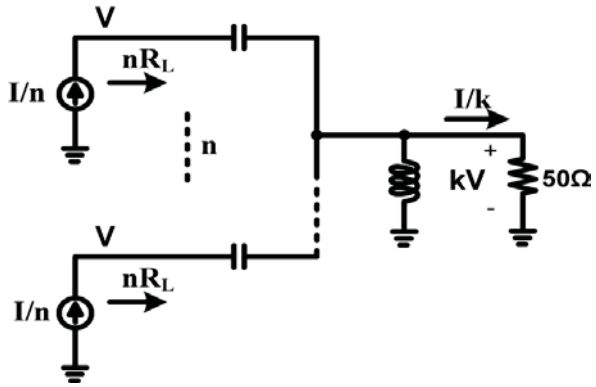

Fig. 4. LC power combiner.

In order to address these issues, we employ a current-mode transformer-based combiner shown in Fig. 5. All the PAs are symmetric with respect to the output and most of the layout routing parasitic resistances are at the 50Ω side. The other advantage of this architecture is smaller loss in the secondary. Assume the resistive part of the secondary side of each transformer in Fig. 5 is *r* and the current is *I/(kn)*, therefore, the total resistive power loss in the secondary would be roughly $rI^2/(nk^2)$. However, in Fig. 3 the resistive part of secondary is *r/n* (assuming it is proportional to the turns ratio) and the current is *I/k,* so the total secondary loss would be rI^2/k^2 which is *n* times larger. The disadvantage of this approach compared to Fig. 3, is that the number of turns is larger on the secondary side, increasing the area and lowering the self-resonance frequency.

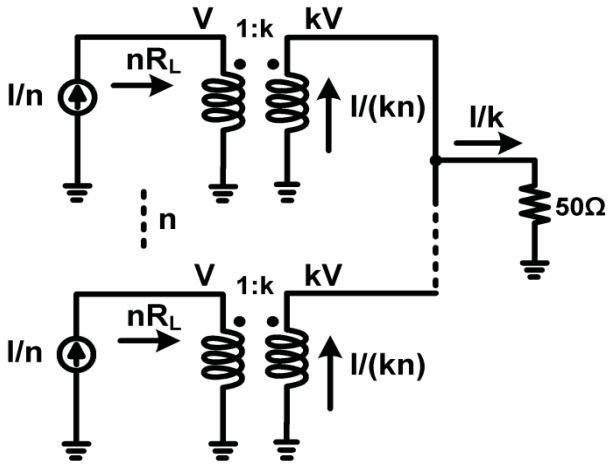

Fig. 5. Current-mode transformer-based power combiner.

The high-level block diagram of the PA is shown in Fig. 6. It has three differential stages with the introduced power

combiner at the output, which combines the powers and also converts the differential signal to single-ended, which eliminates the need for an off-chip balun. The first stage is a 1.2v pseudo-differential cascode amplifier with inductive load tuned to 2.45GHz. The second stage is a 3.3v cascode amplifier with a thick oxide cascode device to improve the reliability. Its output is transformer-coupled to the input of the final stage to increase the common-mode stability.

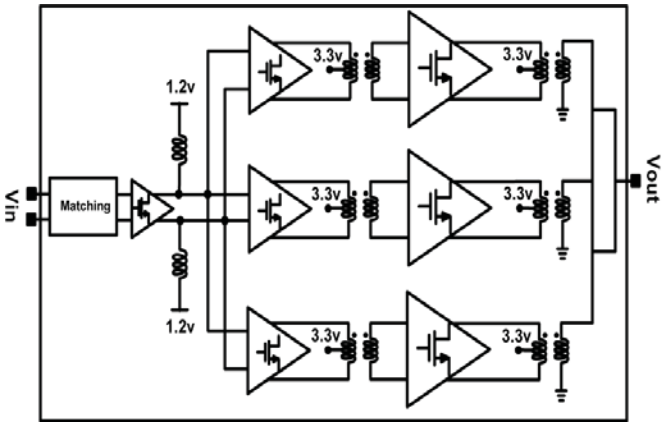

Fig.6. Block diagram of PA.

Fig. 7 shows the simplified schematic of the last stage. It also utilizes a cascode structure with a transformer as the load. The cascode gate bias is carefully set to make sure the Vds of the gm-stage is in the proper and reliable range. To improve the linearity of the PA, an auxiliary stage is used. The main and auxiliary devices are biased with an offset level to linearize the effective transconductance over a wide range of input voltages [2,7]. By utilizing this analog gm-linearization scheme, the P_{1dB} of the transmitter is enhanced to be closer to P_{sat}. In order to improve the linearity further, an open-loop digital pre-distortion technique is used.

III MEASUREMENT RESULTS

The chip is fabricated in a standard 65nm CMOS technology (Fig. 8) and packaged in a 40-pin QFN package. The PA occupies 2.2mm^2 active area. Fig. 9 shows the measured S-parameters. The PA achieves 40dB small-signal gain at 2.45GHz and better than -10dB input match from 1.7GHz to 3.7GHz. Fig. 10 shows the measured output power, PAE and drain efficiency for a 2.45GHz single tone. At a supply of 3.3v the measured P_{sat} is 33.5dBm with a peak PAE and drain efficiency of 37.6% and 44.2% respectively. The measurements show that the PA can deliver more than 30dBm saturated power from 1.6GHz to 3.6GHz.

The measured AM-AM and AM-PM distortion are plotted in Fig. 11. By using the gm-linearization technique, a P_{1dB} of 30.5dBm is achieved. The phase distortion at P_{1dB} is approximately 14 degrees, which can be mostly compensated by digital pre-distortion. One can reduce the phase distortion by reducing the offset voltage between the main and auxiliary

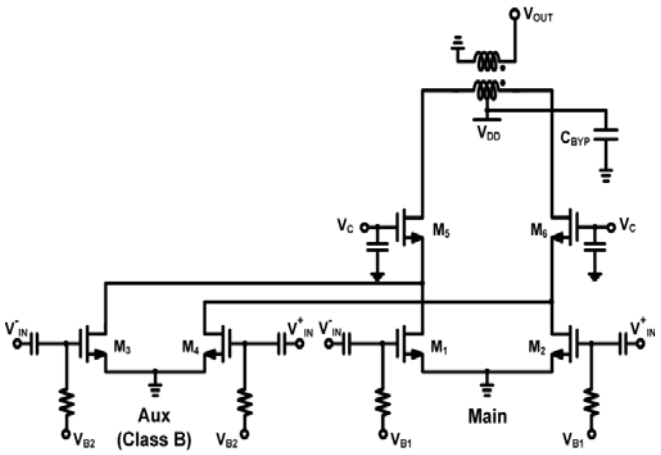

Fig. 7. Simplified schematic of output stage.

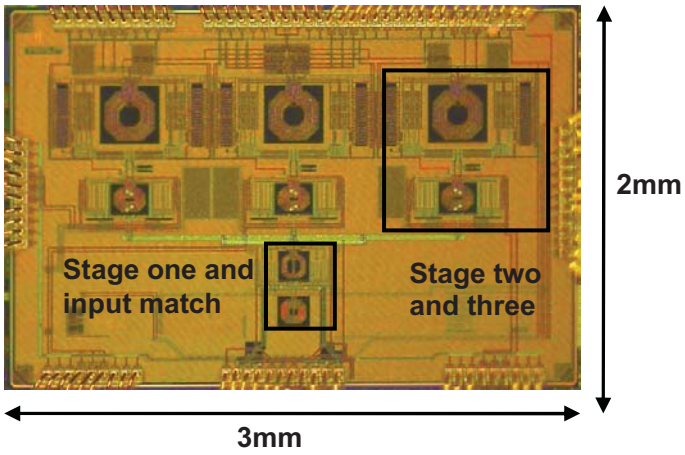

Fig. 8. Die microphotograph.

devices at the input of the final stage, at the expense of lower P_{1dB}.

The measured EVM for a 54Mb/s OFDM signal with and without digital pre-distortion (DPD) is shown in Fig. 12. Without DPD, the measured average power for -25dB EVM is 23.9dBm with 14% PAE and after applying DPD, an output power of 26.4dBm with 22% PAE and -25dB EVM is achieved. The output spectrum meets the 802.11g mask at

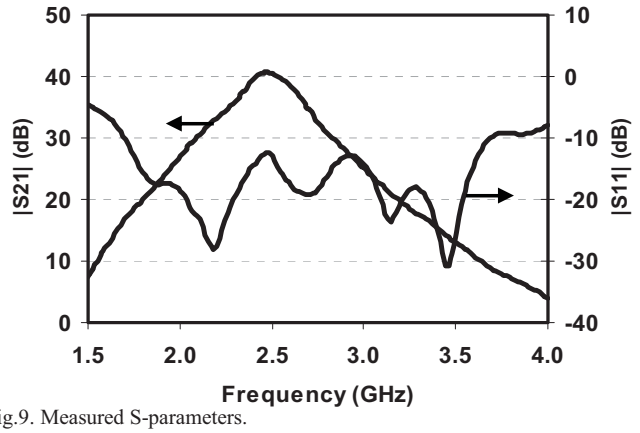

Fig.9. Measured S-parameters.

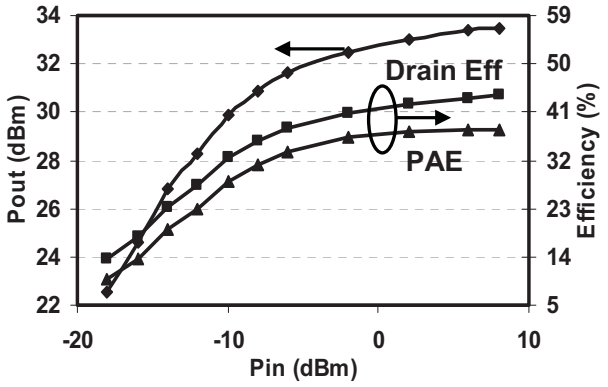

Fig. 10. Measured output power, PAE and Drain efficiency.

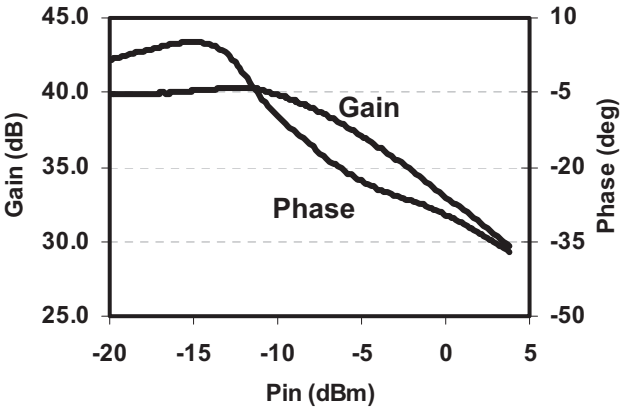

Fig. 11. Measured AM-AM and AM-PM distortion.

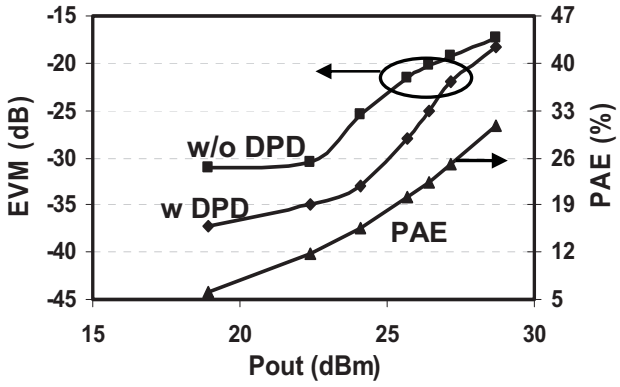

Fig. 12. Measured EVM and PAE for an OFDM 54Mb/s signal.

27dBm output power. In Table I, the measured results are compared with previously reported results in this category.

IV. CONCLUSION

In this paper, we demonstrated a fully integrated power amplifier using a current-mode transformer-based power combiner in a 65nm CMOS process. A saturated power of greater than 2W with the drain efficiency more than 40% is achieved. With a gm-linearization technique and DPD, the PA can deliver 26.4dBm average linear power with -25dB EVM and 22% efficiency, which makes it suitable for high power WLAN and WiMAX applications.

TABLE I. COMPARISON OF 2.4GHz OFDM CMOS PAs

	ref[6]	ref[7]	This work
Psat	30.1dBm	31.5dBm	33.5dBm
Small Signal Gain	28dB	32dB	40dB
Peak PAE	33%	25%	37.6%
Power at -25dB EVM	22.7dBm	25.5dBm	26.4dBm
PAE at -25dB EVM	12.4%	16%	22%
Power at -28dB EVM	N/A	24.5dBm	25.7dBm
PAE at -25dB EVM	N/A	14%	20%
Supply	3.3v	3.3v	3.3v
Technology	90nm CMOS	65nm CMOS	65nm CMOS

ACKNOWLEDGMENT

The authors would like to thank A. Behzad for his valuable support and technical advice. The authors would also like to acknowledge the contribution of A. Sarfaraz for designing the passive components and D. Kwon to DPD as well as the contribution of Broadcom WLAN RF layout team. The authors would also like to acknowledge valuable discussions with Professors P. Asbeck, J. Buckwalter and D. Kimball of UCSD.

I. REFERENCES

[1] C. Wang, M. Vaidyanathan, L. E. Larson, "A capacitive-compensation technique for improved linearity in CMOS Class-AB power amplifiers" *IEEE J. Solid-State Circuits*, Vol 39, Issue 11, pp. 1927-1037, Nov. 2004.

[2] A. Afsahi, A. Behzad, V. Magoon, L. E. Larson, "Linearized dual-band power amplifiers with integrated baluns in 65nm CMOS for a 2x2 802.11n MIMO WLAN SoC," *IEEE J. Solid-State Circuits*, Vol. 45, No. 5, May 2010.

[3] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck, L. E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE J. Solid-State Circuits*, Vol. 42, pp. 1271-1281, June 2007.

[4] I. Aoki, S. Kee et. al, "A fully-integrated quad-band GSM/GPRS CMOS power amplifier," *IEEE J. Solid-State Circuits*, Vol. 43, no. 12, pp. 2747-2758, Dec. 2008.

[5] P. Haldi et al., "A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS," *IEEE J. Solid-State Circuits*, Vol. 43, Issue 5, pp. 1054-1063. May 2008.

[6] D. Chowdhury, C. D. Hull et. al, "A fully integrated dual-mode linear 2.4GHz CMOS power amplifier for 4G WiMax applications," *IEEE J. Solid-State Circuits*, Vol. 44, no. 12, pp. 3393-3402, Dec. 2009.

[7] A. Afsahi, A. Behzad, L. E. Larson, "A 65nm CMOS 2.4GHz 31.5dBm power amplifier with a distributed LC power-combining network and improved linearization for WLAN applications," *ISSCC Dig. Tech. Papers*, pp. 452-453, Feb 2010.