Demonstration of 50-mV Digital Integrated Circuits with Microelectromechanical Relays

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***Abstract*—**50-mV operation of digital integrated circuits at room temperature is demonstrated for the first time using body-biased microelectromechanical relays. An improved relay design and self-assembled molecular coating provide for lower contact adhesion to reduce hysteretic switching behavior, so that the relays operate reliably with sub-50-mV gate voltage swing to provide for ultra-low active power consumption as well as zero static power consumption.

I. Introduction

Nanometer-scale mechanical relays are of interest for ultra-low-power digital computing applications because they in principle can achieve zero OFF-state leakage current (which provides for zero static power consumption) and abrupt switching characteristics so that they can be operated with very low gate voltage swing [1-2]. To minimize dynamic power consumption, a digital integrated circuit (IC) should be operated with a very low supply voltage (V_{DD}). V_{DD} reduction for a relay-based digital IC is limited by the switching hysteresis voltage (V_H) arising from contact adhesive force (F_{AD}). Piezoelectric relays have been demonstrated to operate with very low V_H, ~10 mV [3], but have a more complex structure (*i.e.*, are more costly to manufacture and difficult to miniaturize) than electrostatic relays. In this work, a body-biased electrostatic relay design for digital logic applications is improved to reduce F_{AD}. Furthermore, V_H is reduced with self-assembled molecular coating of the relays to enable stable switching operation with sub-50-mV gate voltage swing. Room-temperature operation of relay-based digital ICs with V_{DD} as low as 50 mV is demonstrated for the first time.

II. Relay Design and Fabrication

The schematic diagrams in **Fig. 1a** illustrate the body-biased microelectromechanical (MEM) relay designs used in this work. Each comprises a movable gate electrode suspended by four folded-flexure beams over a fixed body electrode, and two sets of source/drain electrodes (*i.e.*, two electrical switches). The relay design with four contact dimples (referred to herein as the 4C design) was first introduced in [4], and uses a conductive channel layer (attached underneath the gate electrode with an intermediary insulating layer) to form a bridge between a pair of source and drain electrodes (formed from the same layer as the body electrode) in the ON state. The new relay design introduced in this work has only two contact dimples (one for each electrical switch) for smaller total contact area and hence lower F_{AD} as well as lower ON-state resistance (R_{ON}) [5]; it is referred to herein as the 2C design. A plan-view scanning electron micrograph (SEM) of a fabricated 2C relay is shown in **Fig. 1b**.

As fabricated, air gaps exist between the conductive source and drain electrodes so that no current can flow between them, *i.e.*, $I_{DS} = 0$ (**Fig. 1c**). When a voltage (V_{GB}) is applied between the gate and body, the movable structure is actuated downward by the electrostatic force; if $|V_{GB}|$ is larger than a certain threshold pull-in voltage (V_{PI}), the conductive electrodes are brought into physical contact so that current can flow between the source and drain electrodes (**Fig. 1c**). When $|V_{GB}|$ is subsequently reduced toward 0 V, the spring restoring force of the suspension beams pulls the movable structure out of contact so that I_{DS} drops abruptly to zero at a certain release voltage (V_{RL}). V_H is defined as $V_{PI} - V_{RL}$. Depending on the body bias voltage (V_B), a relay can turn on with either increasing or decreasing gate voltage (V_G) because of the ambipolar nature of electrostatic force. If V_B is negative, then the relay turns on with increasingly positive V_G, similarly as an n-channel MOSFET; in this case, it is referred to as a N-relay. If V_B is positive, then the relay turns on with increasingly negative V_G or decreasingly positive V_G, similarly as a p-channel MOSFET; in this case, it is referred to as a P-relay. Circuit symbols for N-relay and P-relay are shown in **Fig. 2**.

Fig. 3 illustrates key steps in the 2C relay fabrication process, after the patterning of the tungsten (W) layer (body and source electrodes), contact dimple regions, drain electrode via regions, drain electrode (W attached underneath the gate electrode with an intermediary insulating layer of Aluminum Oxide, Al_2O_3), and heavily doped p-type polycrystalline Silicon-Germanium ($Si_{0.4}Ge_{0.6}$) structural layer (gate electrode). (Patterning of the Al_2O_3 layer to define via/anchor regions prior to deposition of poly-$Si_{0.4}Ge_{0.6}$ is not shown since these regions lie beyond the *B-B'* cutline.) As fabricated, the relays in this work have an actuation-gap thickness (g_o) to dimple-gap thickness (g_d) ratio larger than three (*cf.*, **Fig. 3c**) so that they operate in non-pull-in mode to avoid unnecessarily large V_H [6]. To reduce V_H further, relays were coated with a hydrophobic anti-stiction self-assembled monolayer (SAM) of Perfluorooctyltriethyloxysilane (PFOTES) using a vapor-phase process [7] after the relay structures were released (by selectively removing sacrificial oxide layers) in vapor HF (*cf.*, **Fig. 3f**).

III. Results and Discussion

Measured I_{DS}-V_G characteristics for 2C relays and for 4C relays operated as N-relay or P-relay are shown in **Fig. 4** and **Fig. 5**, respectively. Immeasurably-low OFF-state leakage current and $>10^7$ ON/OFF current ratio are observed, as expected. Note that V_H values (summarized in **Fig. 6**) are much lower for coated relays due to reduced surface adhesion energy between the contacting electrode surfaces. The reduction in V_H afforded

by PFOTES coating comes with the tradeoff of increased subthreshold swing (SS), due to tunneling conduction through the PFOTES coating that is modulated by V_G. Average SS values for PFOTES-covered relays are compared for 2C and 4C relay designs in **Fig. 7**. (The full range of measured SS values across eight relays is also indicated.) SS is approximately twice as large for the 4C design as compared with the 2C design, since twice as much force is needed to compress the PFOTES in a 4C relay. (The PFOTES coating between the conducting electrodes can be mechanically modeled as a spring; springs in parallel combination—*cf.*, **Fig. 7** inset—have equivalent stiffness equal to the sum of the individual springs.)

Measured timing diagrams for a relay-based inverter circuit are shown in **Fig. 8**. (The glitches in the signals are due to noise from the power supply.) Various two-input logic functions can be implemented with only two relays (*vs.*, four transistors for CMOS implementations) as shown in **Fig. 9**. Note that pass-gate topology is employed in these circuits, as relays are functionally transmission gates. Since each relay comprises two electrical switches, it is straightforward to implement dual-polarity pass-gate logic, *i.e.*, generate complementary output signals, which eliminates the need for inversions (incurring additional mechanical delays) along the signal path. This topology minimizes the number of mechanical delays and also the number of relays per digital function [8]. (The signal propagation delay in a relay-based IC is dominated by mechanical switching delay, which is much larger than *RC* charging/discharging delay; therefore, an optimally designed relay circuit should minimize the number of mechanical delays, *i.e.*, all relays should switch simultaneously to achieve the fastest possible circuit operation.) The measured voltage waveforms in **Fig. 10** for 2C-relay-based ICs demonstrate their correct operation for NOT, AND, OR, and XOR functions for V_{DD} as low as 50 mV.

Fig. 11 shows the circuit diagram and measurement setup for a 2:1 multiplexer (MUX) implemented with two relays. The source electrode of each relay serves as an input signal line, the gates are interconnected together to form a select line, and the drain electrodes are interconnected together to form the output node. The measured voltage waveforms in **Fig. 12** confirm that this circuit functions properly for V_{DD} down to 50 mV.

In **Fig. 7**, it can be seen that there is significant variation in SS for the coated relays, which indicates that the coating process was non-uniform. For very low operating voltage, poor SS results in lower ON-state current (nA range for V_{DD} = 50 mV, *cf.*, **Fig. 4**) and hence high effective R_{ON}. In this work, the output voltage waveforms were measured using an oscilloscope probe with internal resistance of 10 MΩ (R_{OSC}), which is not much larger than R_{ON} for relays with poor SS operating at very low V_{DD}. As a result, the output voltage does not reach V_{DD} in some cases due to the resistive voltage divider effect modeled by the equivalent circuit shown in **Fig. 13**. When either the N-relay or P-relay is turned on, the voltage divider consisting of R_{ON} connected in series with R_{OSC} limits the output voltage to be less than V_{DD}; when both relays are turned on, the output voltage swing increases closer to V_{DD} since the parallel combination of two resistors provides for lower resistance. It should be noted that, since relays have nearly infinite OFF-state resistance (in contrast to the R_{OSC} of the oscilloscope) due to zero OFF-state leakage, high effective R_{ON} should not prevent proper operation of relay-based ICs. Nevertheless, improvement in the uniformity of the SAM coating process is expected to provide for uniformly low SS (and thereby low R_{ON}) in the future.

It should be noted that body biasing is used for all of the relays in this work in order to minimize V_{DD}. This is necessary to minimize the switching energy of a relay across a range of values of mechanical switching delay [9]. **Fig. 14** shows how the mechanical turn-ON delay (τ_{ON}) of the 2C relay can be improved by increasing V_{DD}, albeit at a tradeoff of higher dynamic power consumption.

IV. Conclusion

A new body-biased relay design is introduced to reduce the number of contacts and thereby reduce the switching hysteresis voltage (V_H) to enable lower gate voltage operation. A self-assembled monolayer coating of PFOTES is effective for further reducing V_H, with a tradeoff of degraded subthreshold swing. Together, these improvements enable relay-based digital ICs to operate reliably with a supply voltage of 50 mV at room temperature. These results show the promise of nanoelectromechanical switches for ultra-low-power computing at the edge of the cloud.

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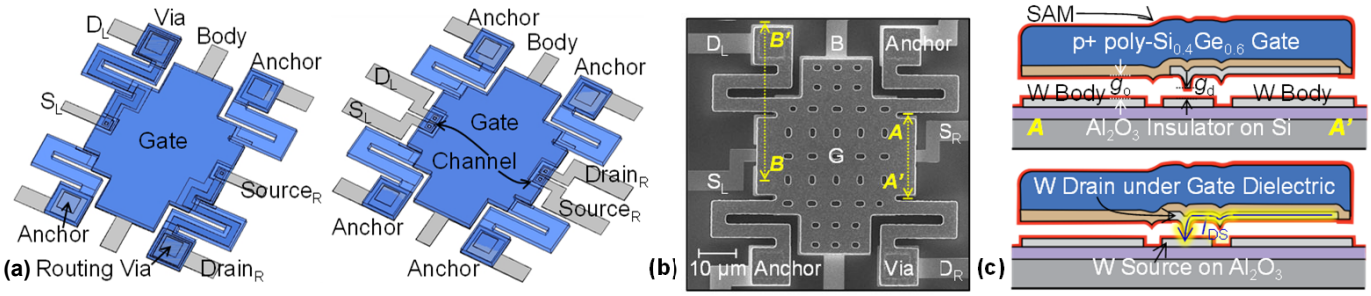


Fig. 1. (a) Isometric schematic views of the new two-contact (left) and old four-contact (right) relay designs. (b) Plan-view SEM of two-contact relay. (c) Cross-sectional views (along the *A-A'* cutline in Fig. 1b) in the off-state (top) and on-state (bottom). As fabricated g_o = 220 nm and g_d = 60 nm.

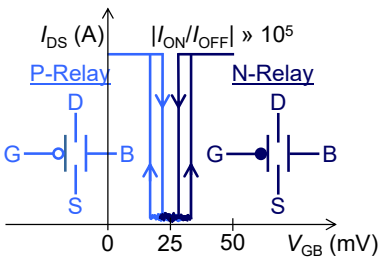


Fig. 2. Circuit symbols and ideal I_{DS}-V_{GB} characteristics. N- or P-relay behavior is determined by the body bias voltage (V_B).

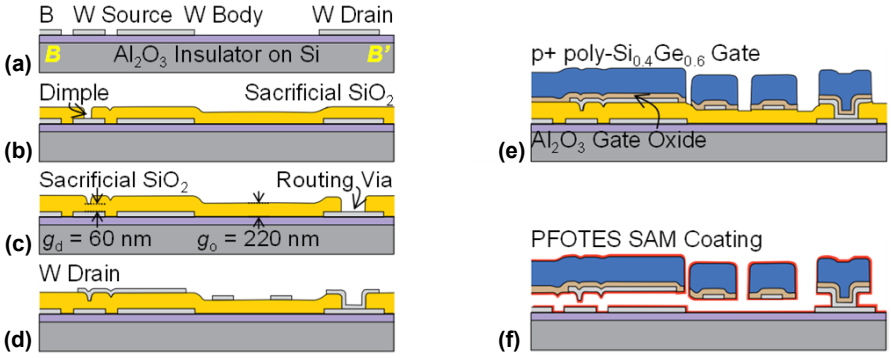


Fig. 3. *B-B'* (*cf.*, **Fig. 1b**) cross-sections illustrating key steps of the 2C relay fabrication process: (a) 60 nm W source and body electrodes formed on 80 nm Al_2O_3 insulating layer. (b) 160 nm 1st sacrificial SiO_2 layer deposition followed by contact dimple definition. (c) 60 nm 2nd sacrificial SiO_2 layer deposition followed by routing via definition. (d) 60 nm W drain electrode formation. (e) 55 nm Al_2O_3 gate insulator deposition followed by anchor region definition (not shown) and 1.9 μm p+ poly-$Si_{0.4}Ge_{0.6}$ gate formation. (f) Release in HF vapor followed by SAM coating.

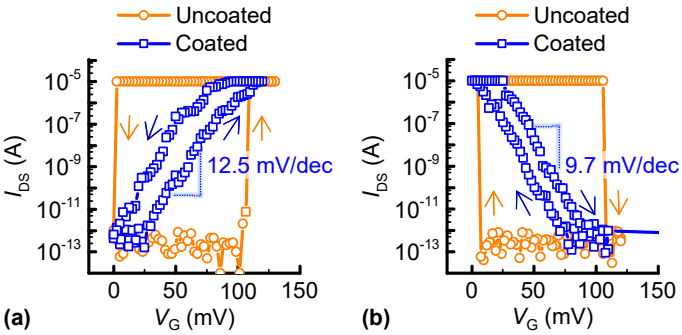


Fig. 4. I_{DS}-V_G curves for 2C (a) N-relay and (b) P-relay, with and without PFOTES coating, measured at 23 ˚C and 10 μTorr. V_{DS} = 200 mV. $|V_B|$ = ~15 V. The current compliance is set to limit I_{DS} to 10 μA.

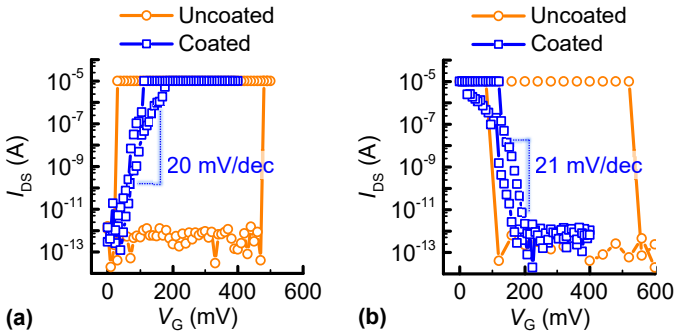


Fig. 5. I_{DS} *vs.* V_G curves for 4C (a) N-relay (b) P-relay, with and without PFOTES coating, measured at 23 ˚C and 10 μTorr. V_{DS} = 200 mV. $|V_B|$ = ~15 V. The current compliance is set to 10 μA.

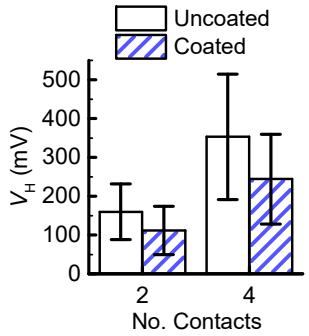


Fig. 6. Average V_H values for 2C and 4C relays, with and without PFOTES coating, measured at 23 ˚C and 10 μTorr. V_{DS} = 200 mV. $|V_B|$ = ~15 V.

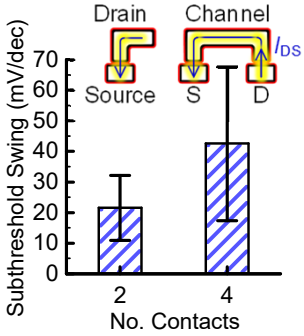
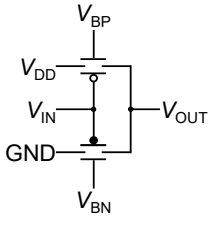


Fig. 7. Average SS values for 2C and 4C PFOTES-coated relays measured at 23 ˚C and 10 μTorr. V_{DS} = 200 mV. $|V_B|$ = ~15 V.



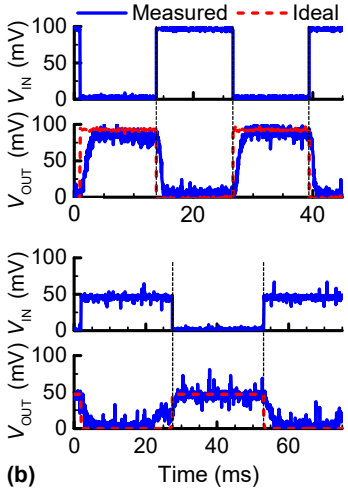


Fig. 8. (a) Schematic circuit diagram for an inverter. (b) Measured timing diagrams for V_{DD} 100 mV and 50 mV at 23 ˚C and 10 μTorr. $|V_B|$ = ~15 V.

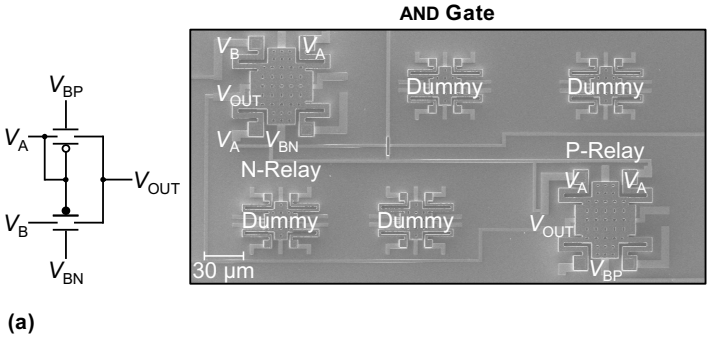


Fig. 9. Schematic circuit diagrams and plan-view SEM images of 2C-relay-based two-input logic gates: (a) AND. (b) OR. (c) XOR.

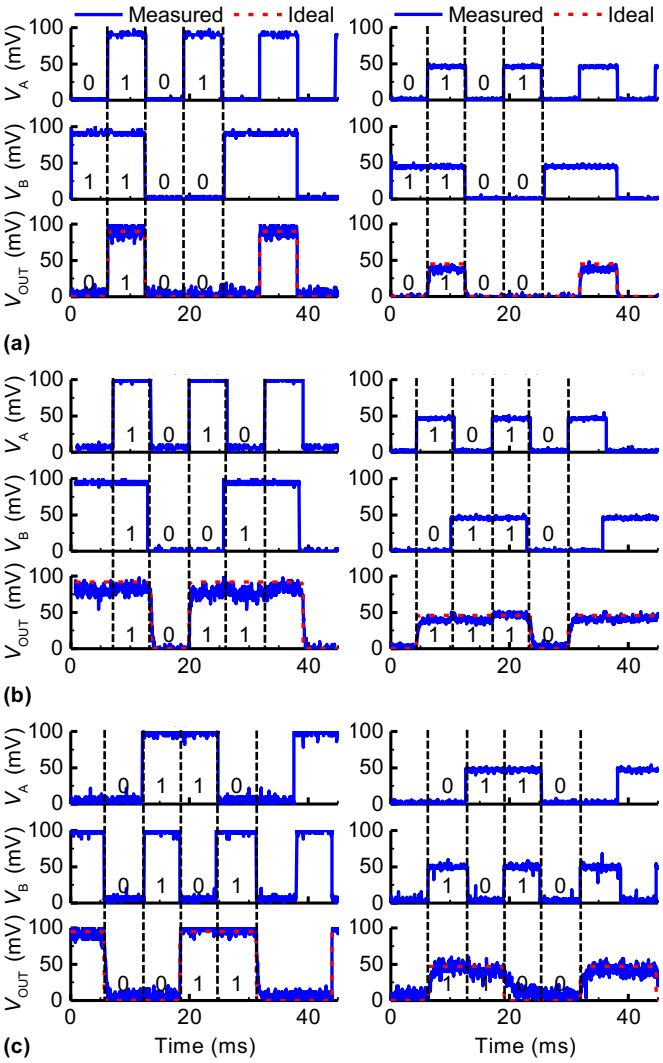


Fig. 10. Waveforms showing ultralow-voltage operation of relay logic gates at 23 ˚C and 10 μTorr. $|V_B|$ = ~15 V. (a) AND. (b) OR. (c) XOR.

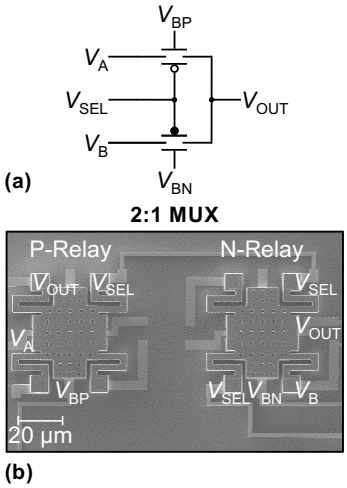


Fig. 11. 2C-relay-based 2:1 MUX. (a) schematic circuit diagram. (b) plan-view SEM image.

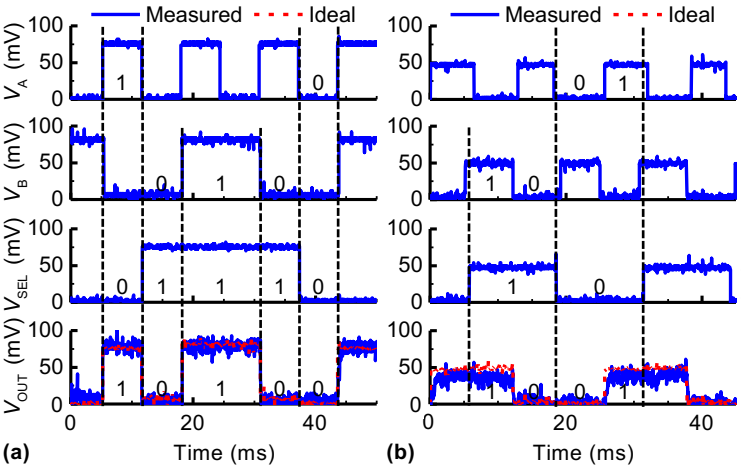


Fig. 12. Measured voltage waveforms demonstrating operation of the 2:1 MUX for low V_{DD} (a) 80 mV and (b) 50 mV at 23 ˚C and 10 μTorr. $|V_B|$ = ~15 V.

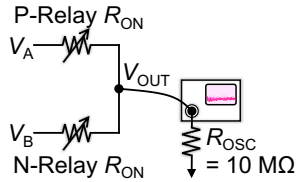


Fig. 13. Equivalent circuit.

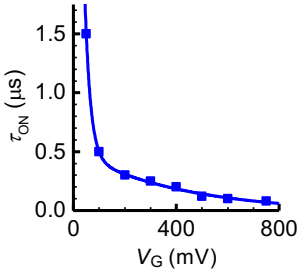


Fig. 14. Relay turn-on delay (τ_{ON}) *vs.* V_G at 23 ˚C and 10 μTorr. V_B = -14.3 V.