28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator

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PicoNodes have applications in warehouse inventory, smart homes, or integrated patient monitoring and require ultra-low power consumption to eliminate battery replacement or enable batteryless systems. A small form factor is key for ubiquitous deployment. Recently, wake-up receivers [1,2] have traded off latency for improved sensitivity for non-latency-critical applications. However, the improved sensitivity requires a high-Q front-end inductor that limits operation to below 200MHz; this stands in the way of a small antenna form factor. Higher-frequency operation makes a smaller antenna possible, but entails lower-Q inductors and higher package parasitics. A receiver with a gate-biased self-mixer [3] has demonstrated a moderate sensitivity at 550MHz with a relatively low-Q matching network, however, the self-mixer introduces extra input capacitance.

Fig. 28.1.1 shows the proposed wake-up receiver architecture to receive an 11b wake-up code OOK modulated at 100b/s on the RF carrier. We introduce gate-biasing for a MOS envelope detector (ED) to reduce its input capacitance and enable high-frequency operation, as well as a time-domain, baseband windowed integrator and a first-order DLL bias loop, to drastically reduce power consumption. The RF input signal passes through the L-C matching network and hits a 40-stage MOS ED. The DC gate potential, V_{gate_bias}, generated using a current-biased replica ED, biases the ED transistors in the weak-inversion linear region. The matching network provides 23dB of passive gain, and combined with the ED, the RF-to-baseband conversion $v_{bb,edo}/P_{in}$ is 21mV/nW. The ED baseband output $v_{bb,edo}$ is amplified by 26dB with a g_m-reuse amplifier and then fed to a clocked voltage-controlled delay line ($VCDL_A$). When the OSC CLK is high, $VCDL_A$ and a reference $VCDL_B$ are put in a VCO configuration and encode the signal and reference $V_{delay,ref}$ in the time domain. They operate as windowed integrators with a sinc frequency response that rejects high-frequency noise before digitization. Its outputs pass through delay lines to set the comparator threshold and are then compared using a PFD and latched. The comparator output is fed to an 11b digital correlator to detect the wakeup signature. The outputs of the VCDLs are also compared using a PFD and fed back to the ED reference input $v_{ed,ref}$. This first order, low bandwidth, delay-locked loop rejects the DC signal due to continuous-wave interferers at the receiver input and any DC offsets introduced by the baseband circuits.

Optimizing the RF front-end design for wake-up receivers is critical to maximize sensitivity. The maximum Q-factor of the inductor available for the matching network and the input capacitance of the ED decide the achievable front-end passive gain and operating frequency. For a given inductor Q-factor, the achievable passive gain increases with the input resistance of the ED, $R_{in,ed}$ (Fig. 28.1.2). While a high $R_{in,ed}$ is desired for maximum passive gain, due to the passive nature of the ED, with increasing input resistance, the output resistance also increases, thus increasing the noise floor at the output of the ED. Optimizing the SNR at the output of the ED requires a careful selection of $R_{in,ed}$. With gate biasing, the ED $R_{in,ed}$ can be tuned. A 3.5dB improvement in sensitivity is obtained by reducing the $R_{in,ed}$ from 1MΩ (value for max. gain) to 50kΩ (value for max. SNR) for a 108nH inductor with a Q-factor of 200 at 433MHz. Additionally, the gate-biasing technique doesn't affect the conversion gain, makes the ED independent of processes variations, and provides a significant reduction of the input capacitance to only 44fF for a 40-stage ED. In our design, we selected a 200kΩ $R_{in,ed}$, which is only 1dB removed from the optimum while giving 2× advantage in power consumption.

A 40-stage gate-biased ED with an $R_{in,ed}$ of 200kΩ has an $R_{out,ed}$ of 320MΩ. For a current-reuse baseband amplifier (Fig. 28.1.1), the input-referred noise is $4kT\gamma/(2g_m)$. Assuming γ=1.2 and g_m/I_d=29, an I_d=370pA offers a simulated 1dB amplifier NF compared to the ED noise and provides a 26dB gain, while only consuming 150pW at 0.4V. The amplifier is current-biased using a PMOS current mirror with AC coupling while the NMOS input transistor is biased through the delay-locked loop. Figure 28.1.2 shows the noise PSDs demonstrating a 1dB amplifier NF in the signal bandwidth from 10Hz to 100Hz. The low-frequency flicker noise is rejected by the DLL.

A time-domain windowed integrator was proposed in [4] for power-efficient ADCs, but can be used here to serve as a matched detector for the rectangular bit shape; it filters the high-frequency baseband noise and improves SNR before sampling. Two voltage-controlled delay lines ($VCDL_A$ and $VCDL_B$) with clocked feedback realize a V-to-T signal conversion and time-domain integration (Fig. 28.1.3). The integration begins at the rising edge of the OSC CLK running at 200S/s for 2× oversampling, which is derived from the REF CLK provided by an on-chip oscillator operating at 1.6kHz.

In the signal path, current-controlled delay cells with a different delay (τ_n and τ_p) in each branch after VCDLs determine the comparison threshold, which allows to keep the false-alarm rate below 1/hr. A PFD compares the output phases and a clocked latch samples the output at the end of the integration period. The latch output then passes through a D-flipflop to the digital correlator. The sampling instances are not synchronized with the incoming data and, due to possible misalignment, with 2× oversampling every alternate bit can be unreliable. The on-chip 100pW 11b sliding-window digital correlator skips every alternate bit and thus correlates with the most reliable data and is flexible across different codes. Figure 28.1.4 shows the corresponding correlator coefficients, the correlator implementation and receiver response to a -79dBm wake-up signal at 434.4MHz.

In the DLL path (Figs. 28.1.1&3), a PFD-CP samples the phase offset of VCDLs and feeds the lowpass filtered DC offset back at the reference input of the ED. The 1pA CP with a 40pF load is enabled every alternate sample for 1/8× the clock period at the end of integration cycle to reduce the loop bandwidth to 5Hz. The integrator response from the CP ensures that the DC phase offset at the VCDL output is minimized, which is exactly what is desired for the comparator in the signal path. This allows for drastically reducing the size of VCDL integrators without affecting the baseband offset, and then for operating them at only 100pW.

The 65nm LP CMOS wake-up receiver prototypes (Fig. 28.1.7) have been measured at 151.25MHz and 434.4MHz, providing a 3dB bandwidth of 4MHz and 10MHz, using two ICs with the respective matching networks; the corresponding S_{11}'s are in Fig. 28.1.5. The power consumption from the 0.4V supply was measured using an 8.5-digit digital multimeter; at 434MHz the total consumption was 420pW (breakdown in Fig. 28.1.7) and at 151.25MHz it was 370pW. The missed detection ratio (MDR) was measured (Fig. 28.1.5) using the on-chip correlator with a code of "11100100110" at 100bps. For an MDR of 10^{-3}, a -78.3dBm/-79.1dBm sensitivity was obtained for 151.25MHz/434.4MHz. The signal-to-interference ratio (SIR) to maintain an MDR of 10^{-3} was measured (Fig. 28.1.5) with the desired signal at -77dBm. For a worst-case AM interferer 100% modulated with 1010-pattern at 100bps, the SIR was -3.7dB/+5.8dB at 3MHz offset for 151.25MHz/434.4MHz; the DLL does not offer rejection to AM interference and the SIR frequency profile follows the S_{11} profile. For a continuous-wave interferer at 3MHz offset, the SIR is as good as -23.3dB/-13.8dB for 151.25MHz/434.4MHz, thanks to the additional 20dB rejection by the DLL; the maximum rejection is limited by the dynamic range of the DLL CP. Figure 28.1.6 shows the comparison with state-of-the-art wake-up receivers. The receiver provides an 8dB better sensitivity at 434.4MHz and a 3dB better sensitivity at 151.25MHz, both at a 10× lower power consumption compared to the prior art.

Acknowledgments:
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References:
[1] J. Moody et al., "A –76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation," *ISSCC*, pp. 452-454, Feb. 2018.
[2] P. P. Wang et al., "A Near-Zero-Power Wake-Up Receiver Achieving –69-dBm Sensitivity," *IEEE JSSC*, vol. 53, no. 6, pp. 1640-1652, June 2018.
[3] V. Mangal and P. R. Kinget, "An Ultra-Low-Power Wake-Up Receiver with Voltage-Multiplying Self-Mixer and Interferer-Enhanced Sensitivity," *IEEE CICC*, pp. 1-4, 2017.
[4] S. E. Hsieh and C. C. Hsieh, "A 0.4V 13b 270kS/S SAR-ISDM ADC with an Opamp-less Time-Domain Integrator," *ISSCC*, pp. 240-242, Feb. 2018.

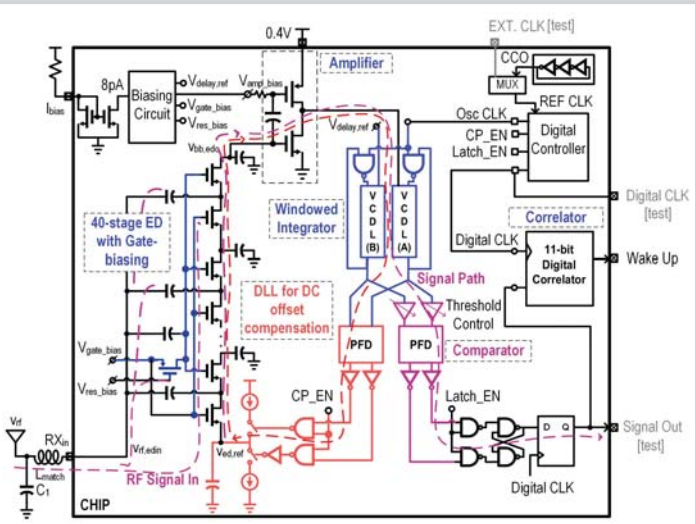

Figure 28.1.1: Fully integrated wake-up receiver using an ED with gate-biasing, a time-domain windowed integrator, an 11b correlator, and a first order DLL.

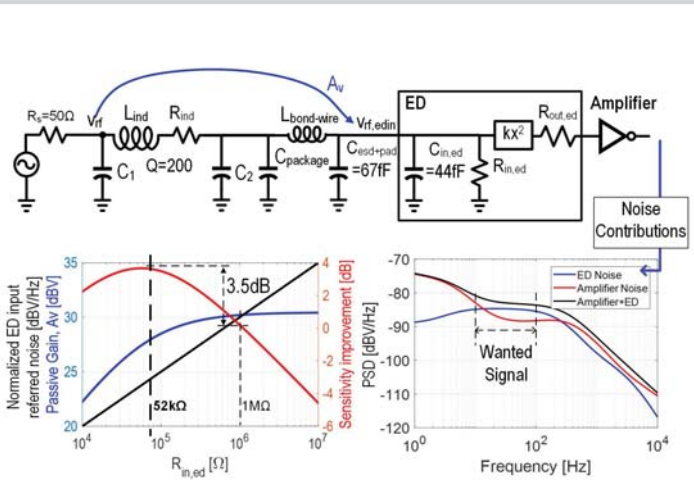

Figure 28.1.2: Optimization of the energy detector's input resistance $R_{in,ed}$ for optimal sensitivity at 434MHz.

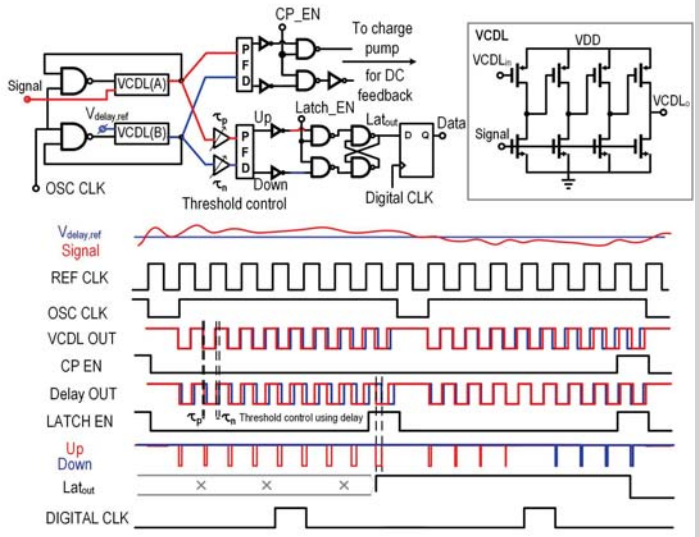

Figure 28.1.3: Operation of the time-domain windowed integrator and comparator.

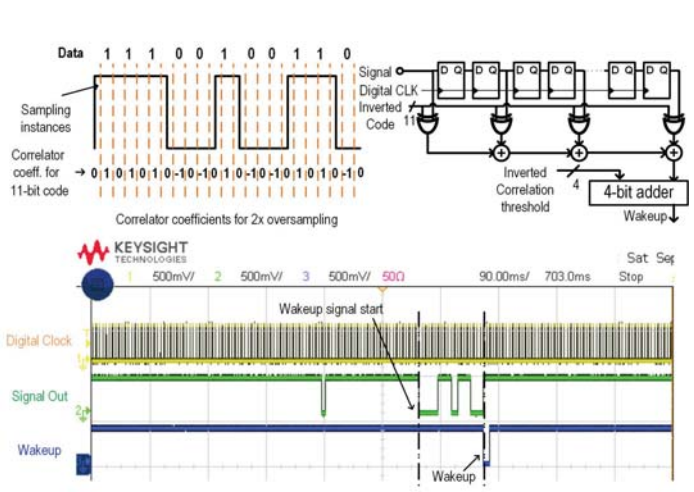

Figure 28.1.4: Implementation of the low-power 11b correlator and it's response for a -79dBm wake-up signal at 434.4MHz.

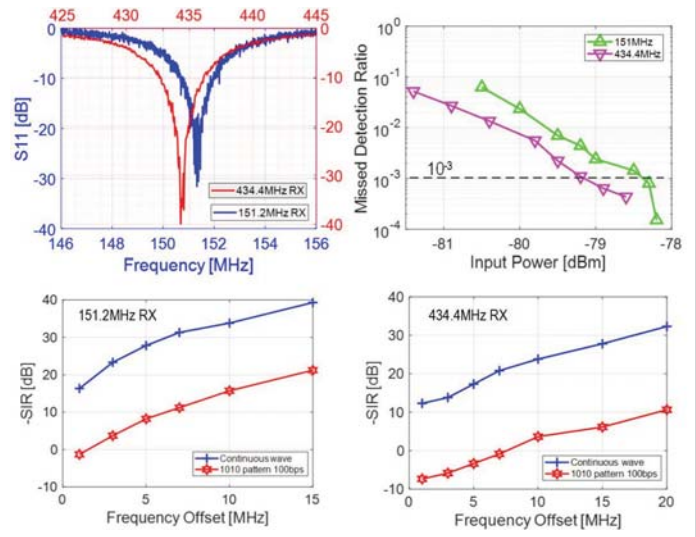

Figure 28.1.5: Receiver RF input reflection S_{11}, missed detection ratio and sensitivity, inverse of SIR for continuous-wave and worst-case AM interferer.

		Wang ESSCIRC'17	Jiang ISSCC'17	Sadagopan RFIC'17	Mangal CICC'17	Moody ISSCC'18		This Work	
Features		Active Rectifier	Active Rectifier	High-Q FE Co-design	Self-Mixer	Passive Rectifier + Auto-threshold compensation		Gate-biased ED + Time-domain Integrator	
Tech Node		180 nm	180 nm	65 nm	130 nm	130 nm		65nm LP	
Frequency	[MHz]	405	113.5	2400	550	151.8	433	**434.4**	**151.25**
Modulation		OOK	OOK	OOK	OOK	OOK		OOK	
Chip Rate	[kbps]	0.3	0.3	2.5	400	0.2		0.1	
Code Length		16-bit	16-bit	32-bit	11-bit	16-bit		11-bit	
Power	[nW]	4.5	4.5	365	222	7.4		**0.42**	**0.37**
Passive Gain	[dB]	18.5	25	N/A	19	NR	NR	23	23
Sensitivity	[dBm]	-63.8	-69	-61.5	-56.4	-76	-71	**-79.1**	**-78.3**
Latency	[mSec]	53.3	53.5	12.8	0.028	82.5	82.5	**110**	**110**
In Band SIR[1] [3MHz off.]									
AM Jammer	[dB]	N.R.	-4	N.R.	-2	-4	N.R.	5.8	-3.6
Cont. Wave	[dB]	N.R.	-11	N.R.	-14	-30	N.R.	-14	-23.3
Latency Norm. Sens. [dBm]		-70.2	-75.4	-71.2	-79.2	-81.4	-76.4	**-83.9**	**-83.1**
FoM	[dB]	-154	-159	-136	-146	-163	-158	**-178**	**-177**

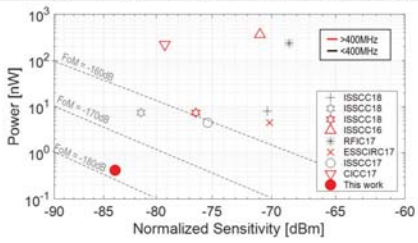

Figure 28.1.6: Summary of performance and comparison with state of the art.

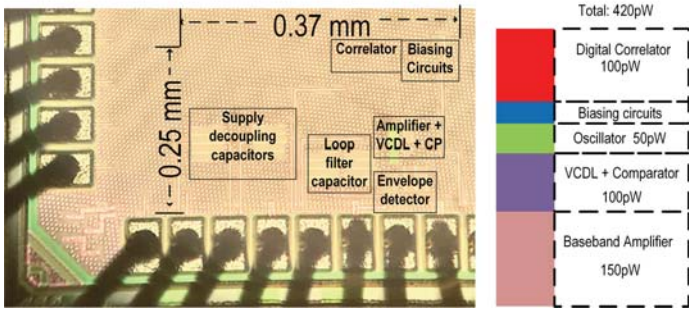

Figure 28.1.7: Die micrograph (active area is 0.093mm²) and breakdown (in part based on simulations) of the measured 0.42nW total power consumption at 434MHz.

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