A 0.18μm Probabilistic-Based Noise-Tolerate Circuit Design and Implementation with 28.7dB Noise-Immunity Improvement

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Abstract

As the size of CMOS devices is scaled down to the nanoscale level, noise interferences start to significantly affect the VLSI circuit performance. Because the injected noise is random and dynamic in nature, a probabilistic-based approach is more suitable to handle signal errors than the conventional deterministic circuit designs. In this paper, we design and implement an 8-bit Markov Random Field carry lookahead adder (MRF_CLA) probabilistic-based noise-tolerant circuit in 0.18μm CMOS process technology. This is the first working silicon design to prove the design concept of the noise-tolerant MRF circuits. The measurement results show that the proposed of the MRF adder can provide 28.7dB of noise-immunity as compared with its conventional CMOS design, when both circuits are facing the same server SNR environment. The MRF adder circuit can also achieve 10^{-6} BER when the supply voltage is only 0.45V and SNR is only 10dB.

I. Introduction

As we move into the nanoscale CMOS designs, signal errors, which directly account for thermal noise, become significantly and start to affect the VLSI circuit performance. Because the faults are random and dynamic in nature, a probabilistic approach is more suitable to handle these random injected noises. Recently, many recent noise-tolerant circuit techniques have been proposed [1-3]. However, they all focus on dealing with a certain kind of noise source. As a result, they cannot effectively solve the random thermal noises that become dominant in future nanoscale VLSI systems. Refs. [4-6], on the contrary, proposed systematic ways to deal with structural and signal errors for future nanosystems.

In this paper, we follow the design concept of [6] and propose a probabilistic noise-tolerant circuit design. It can efficiently handle randomly injected noises based on the theory of Markov Random Field (MRF) [6]. The MRF provides a formal probabilistic framework so that computation can be directly embedded in a network with immunity to both device and signal failures. By computing the logic states in a probabilistic way, the proposed MRF-based noise-tolerant circuit can bring the circuit to operate much near the physical limitation. Moreover, the MRF is general and directly programmed without the learning required by neural network architectures. To demonstrate the noise-tolerance capability, we implement an MRF 8-bit Carry lookahead adder (MRF_CLA) in 0.18μm CMOS process technology. From the measurement results, the noise-immunity of the proposed MRF_CLA can be improved by about 28.7dB as compared to the conventional static CMOS CLA (CMOS_CLA) under the same low SNR environment.

II. Noise-tolerant Nanoscale Design

We proposed the probabilistic design [6] to handle the noise (please refer to [6] for detailed discussion about MRF design). A possible MRF circuit design was presented in [7]. The MRF provides a formal probabilistic framework, which has been commonly used in many fields, including pattern recognition and communications. The main reason for selecting the Markov random network as the basis for our design is that its operation does not depend on perfect devices or perfect input signals. The basic idea of MRF design is as follows: under the probabilistic framework, we cannot expect logic values in a circuit at a particular time to be correct. We can only expect the probability distribution of the values to have the highest likelihood in a correct logic state. The appropriate mathematical framework for this type of analysis is the MRF, which was developed [6] to support the optimization of the values of a large set of random variables so that their overall joint probability has a global maximum.

Taking the M3 module of the ISCAS-85 C432 interrupt controller [8] shown in Fig. 1(a) as an example circuit, we can explain the MRF mapping as follows. The M3 circuit can be mapped onto an MRF as shown in Fig. 1 (b).

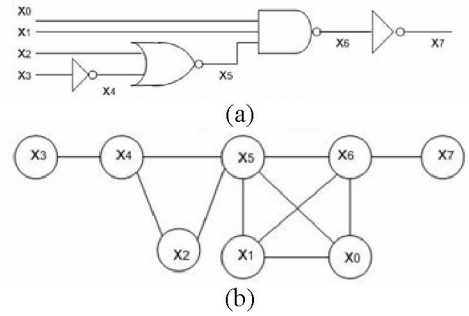


Fig. 1: A logic circuit & its MRF graph (a) A sample circuit; (b) its MRF graph. [7]

Ref [7] shows one of the possible implementations of the MRF designs. Fig. 2 shows MRF NAND implementation. The principle of the MRF design is to design the circuit so that the optimal setting has the highest probability. To achieve this goal, four feedback loops, $([\overline{x_0}\,\overline{x_1}\,x_2],[\overline{x_0}\,x_1\,\overline{x_2}],[x_0\,\overline{x_1}\,\overline{x_2}],[x_0\,x_1\,\overline{x_2}])$ in Fig. 2, are implemented to strengthen the NAND-gate correct logic relationship. For example, suppose that $\{x_0 = 0, x_1 =$

0, x_2=1}. The AND gate at the very top is active and feeds a logic '1' back to the input of the NOR gates at the bottom. The other AND gates feeds back a logic '0'. These feedback values are consistent with the input values {x_0=0, x_1=0, and x_2=1}, and the overall circuit latches into this correct state [$\overline{x_0}\,\overline{x_1}\,x_2$]. The other correct configurations, such as {x_0 = 0, x_1 = 1, x_2=1) or [$\overline{x_0}\,x_1\,x_2$], are also stable. The incorrect configurations, such as {x_0 = 0, x_1 = 0, x_2=0}, are not stable and will converge to a correct state, such as [$\overline{x_0}\,\overline{x_1}\,\overline{x_2}$] converges to [$\overline{x_0}\,x_1\,x_2$]. The AND and NOR gates in Fig. 2 are the conventional logic gates. The power of the MRF approach is that the joint distribution of random logic levels in the circuit can be made to converge to the correct logic operation with the high probability.

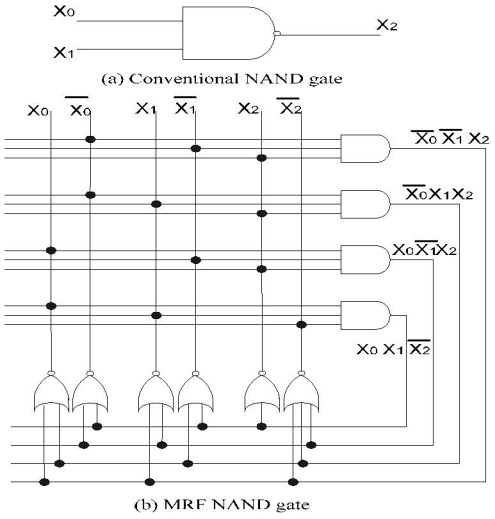


Fig. 2: The schematic of a NAND logic (a) A CMOS NAND gate & (b) its MRF NAND logic. [7]

The corresponding SPICE simulation is shown in Fig. 3 by using the 70nm CMOS library from Berkeley (http://www-device.eecs.berkeley.edu/~ptm/) at room temperature. The top two curves are the input signals, which are generated by adding the Gaussian noise with zero mean to logic '1' and to logic '0'. The noise on the inputs causes the standard CMOS NAND gate to switch between correct and incorrect output values as shown in the bottom curve in Fig 3. The MRF outputs remain robust as shown in the second curve above the bottom. We can see that the MRF design has much better noise-tolerance capability.

In a logic circuit, hundreds of internal logic signal paths exist from the inputs to the output. Only one set of variable assignments has the highest probability of being correct, and the correct set corresponds to the optimum setting. The propagation of logic states through the network is such that the distribution of each variable has a local maximum probability in order to have the correct logic values. The noise-tolerant capability is achieved because the MRF network is updated by iteratively changing the state of nodes and propagating these changes

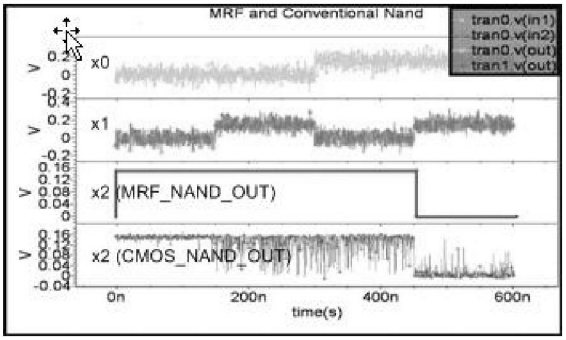


Fig 3: Simulation results of the inputs/ouputs of CMOS and MRF NAND.

through the network. Ultimately the network converges to a stable set of state probabilities corresponding to the correct logic states. A computational result is then determined by selecting these visible output states. Successful operation only requires that the energy of correct states is lower than the energy of errors.

III. Chip Implementation and Measurement

3.1 Chip implementation

To demonstrate the noise-tolerance capability of the MRF circuits, we utilize an 8-bit carry-look-ahead adder (CLA) as a proof-of-concept design for performance comparison. The proposed 8-bit MRF CLA is illustrated in Fig. 4. To construct a MRF-CLA, we divide the whole CLA into many basic cells and map the MRF circuit on these basic cells. By this way, the design overhead will not increase rapidly and the noise-tolerance performance can be preserved.

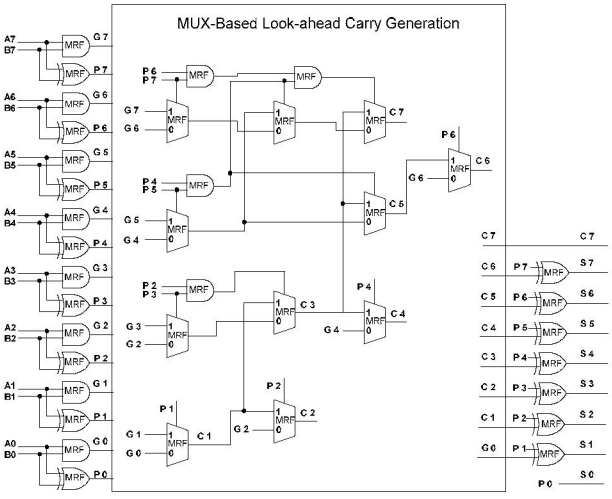


Fig 4: Architecture of the proposed 8-bit MRF-CLA.

Both the probabilistic-based MRF CLA and the conventional deterministic CMOS CLA circuits are implemented by UMC 0.18μm CMOS process. The MRF CLA layout and die photo are shown in Fig. 5. The performance summary is collected in Table 1. As a comparison, the transistors count in the proposed MRF design needs 5040 transistors, which is more complex

than the conventional CMOS design. The noise tolerance ability of MRF design, however, can be improved about 10^2~10^4 times under various AWGN noise interference. With superior noise-tolerant ability, the operation voltage in the MRF design can be significantly reduced to operate under the sub-threshold region for power savings. The conventional CMOS design simply cannot operate under such low power environment. In extremely noisy nanoscale computing system, the improvement of noise-tolerance ability and energy consumption outweigh what we compromise in the design complexity. Moreover, by using nanofabrication technology, we expect nanoelectronics to compensate the drawbacks of MRF. Noise interference is certainly going to get much worse in nanoelectronic circuits, and conventional CMOS circuit technique simply cannot deal with the problems.

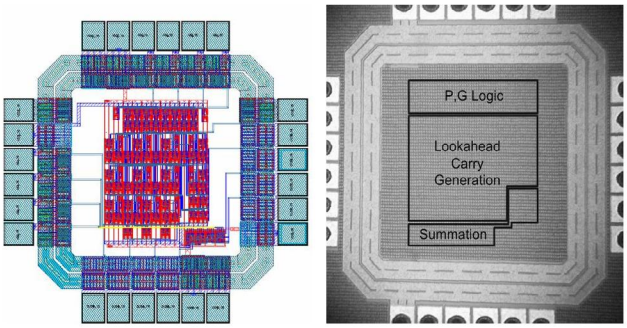


Fig. 5: Layout and die photo of MRF CLA chip.

Table 1: MRF chip performance summary

Process	UMC 0.18um
Area	0.8um*0.8um
transistor	5040
Energy	8 uw/MHz @ 0.45V 25 uw/MHz @ 0.5V 95 uw/MHz @ 0.8V 724 uw/MHz @ 1.8V
BER	2.88E-06@10.6dB SNR 1.95E-07@11.9dB SNR 2.50E-10@14.8dB SNR
Noise Immunity Improved 28.7dB	

We use the power splitter to combine the noise-free input signal with a large AWGN noise as illustrated in Figure 6. The combined noisy signal is then injected into both the MRF CLA and the CMOS CLA circuits for the noise-tolerance performance comparison. In measurement, as illustrated in Fig. 7, we can observe each single bit in the CLA output to compare the waveforms under noise interference. We can further employ the eye-diagram to observe the output waveform of circuits under the interference of random noise by continually reduplicating "0" and "1" signals under random noise interference. Comparing the eye-diagram of Fig. 8 under the case of $1V_{pp}$ AWGN noise interference, we can demonstrate the noise-tolerance performance of the proposed MRF noise-tolerant circuit is much better than the CMOS_CLA circuit. Under ultra-low voltage operation, we can use the histogram to compare the noise-tolerance under sub-threshold region, as illustrated in Fig. 9. The noise-tolerance of the proposed MRF design is much better than the CMOS_CLA circuit under ultra-low voltage operation.

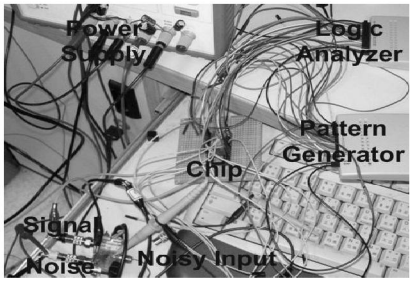
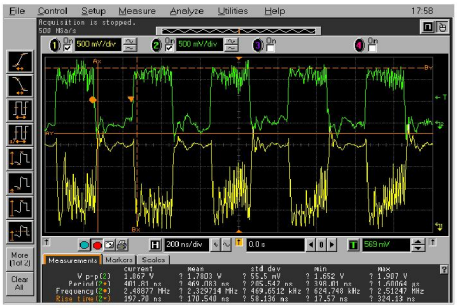
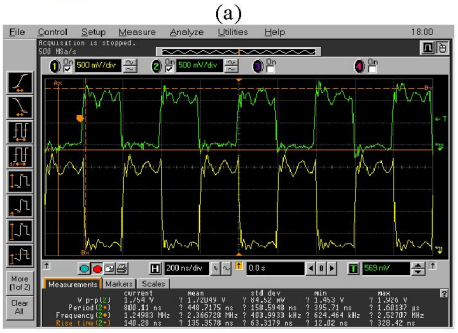


Figure 6: Measurement Setup of MRF Probabilistic-based Noise-tolerant Circuit.

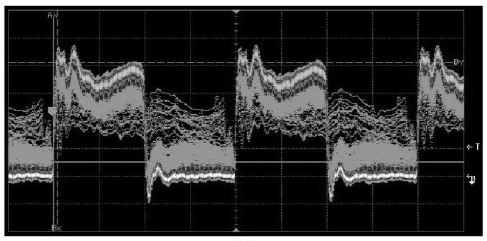


(a)

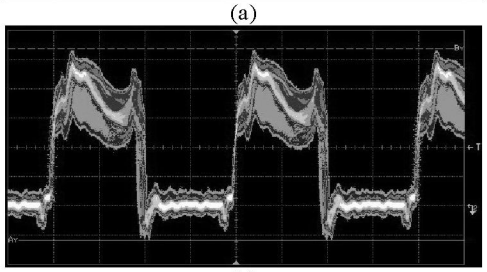


(b)

Fig. 7: Measured single-bit waveform of the CMOS_CLA (a) and the MRF_CLA circuit (b) under $1V_{p\_p}$ AWGN noise.



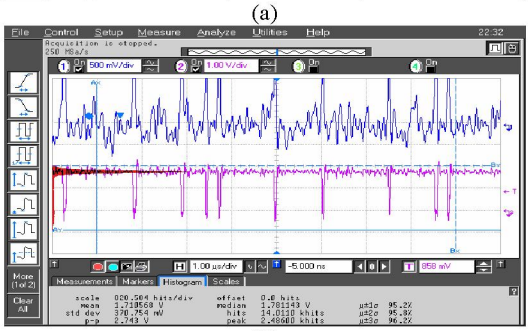
(a)



(b)

Fig. 8: Eye-diagram of the CMOS_CLA (a) and the MRF_CLA circuit (b) under $1V_{p\_p}$ AWGN noise interference.

(a)



(b)

Fig. 9: Histogram of the CMOS_CLA (a) and the MRF_CLA circuit (b) under sub-threshold region with noise interference.

By adjusting the noise power and supply power, we can measure the Bit-Error-Rate (BER) of MRF_CLA and CMOS_CLA circuits under various Signal-to-Noise Ratio (SNR) levels as illustrated in Fig. 10. Based on our real-time measurement results, the noise-immunity of the MRF_CLA can be enhanced by 28.7dB, which means with about $7.4*10^2$ times improvement in BER, as compared to the conventional CMOS_CLA. High noise-immunity feature of the MRF circuit is also very useful to low-power silicon circuits when they operate under very low Vdd condition. In 0.18µm process, under 11dB low SNR condition, the MRF circuit can achieve 10-6 BER under 0.45V supply voltage, which consumes only 8µw/MHz. By replacing the normal MOS transistor with the low-Vth MOS transistor, the operating voltage can be further reduced to 0.24V with only 1.3µw/MHz energy consumption. This MRF_CLA chip has demonstrated the first prototyping design of the noise-tolerant MRF circuits. Hence, it is a good candidate for future nanoscale circuit designs where the operating environment is very noise intensive.

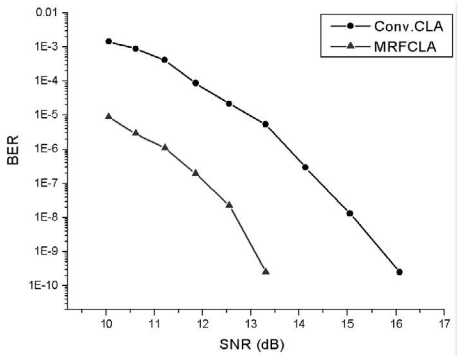


Fig. 10: Noise-Immunity Comparison of MRF_CLA and CMOS_CLA circuit under various SNR.

V. Conclusion

In our MRF design, we directly embed logical computation in a network with immunity to noise. We adopt MRF because this methodology is general and can be directly built onto individual logic gates without the learning as required by the neural network design. To demonstrate the performance of the proposed MRF design, we implemented a proof-of-concept MRF carry-lookahead adder (CLA) onto a silicon chip. Our preliminary measurements show that the noise-immunity of the CLA can be improved by about 28.7dB as compared to the conventional CMOS CLA. With better MRF design and nanofabrication technology, we expect the performance to improve further.

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References

[1] Andre DeHon. "Array-based architecture for fet-based, nanoscale electronics". IEEE Transactions on Nanotechnology, 2(1):23–32, March 2003.

[2] S. C. Goldstein and M. Budiu, "Nanofabrics: Spatial computing using molecular electronics". 28th Annual International Symposium on Computer Architecture, pages 178–189, 2001.

[3] J. von Neumann, "Probabilistic Logic and the Synthesis of Reliable Organisms from Unreliable Components". Automata Studies. Princeton University Press, 1956.

[4] Jie Han and Pieter Jonker, "A system architecture solution for unreliable nanoelectronic devices". IEEE Transactions on Nanotechnology, 1(4):201–208, December 2002.

[5] S. Folling, O. Turel, and K. Likharv, "Single-electron latching switches as nanoscale synapses". In Proc. of Int. Joint Conf. on Neural Networks, pages 216–221, July 2001.

[6] Samuel Luckenbull, "Building bayesian netorks with analog subthreshold CMOS circuits". http://zoo.cs.yale.edu/classes/cs490/01-02b/luckenbill.samuel.sbl23/.

[7] Kundan Nepal, R. Iris Bahar, Joseph Mundy, W. R. Patterson, A. Zaslavsky, "Designing logic circuits for probabilistic computation in the presence of noise". In Proc. of Design Automation Conference 2005, pp. 485-490, June, 2005.

[8] F. Brglez, et. al., "A neural netlist of 10 combinational benchmark circuits and a target translator in Fortran," in Proceedings of IEEE Intl. Symp. on Circuits and Systems, pp. 663–698, June 1985.