20-nm magnetic domain wall motion memory with ultralow-power operation

S. Fukami[1,*], M. Yamanouchi[1,2], K.-J. Kim[3], T. Suzuki[4], N. Sakimura[5], D. Chiba[3,6,7], S. Ikeda[1,2], T. Sugibayashi[5], N. Kasai[1], T. Ono[3], and H. Ohno[1,2,8]

[1]Center for Spintronics Integrated Systems, Tohoku University, 2-1-1 Katahira, Aoba, Sendai 980-8577 Japan

[2]Laboratory for Nanoelectronics and Spintronics, RIEC, Tohoku University, 2-1-1 Katahira, Aoba, Sendai 980-8577 Japan

[3]Institute for Chemical Research, Kyoto University, Uji, Kyoto 611-0011 Japan

[4]Renesas Electronics Corporation, 1120 Shimokuzawa, Chuo, Sagamihara 252-5298 Japan

[5]Green Platform Research Laboratories, NEC Corporation, 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501 Japan

[6]Department of Applied Physics, Faculty of Engineering, The University of Tokyo, Bunkyo, Tokyo 113-8656 Japan

[7]PRESTO, Japan Science and Technology Agency, Kawaguchi, Saitama 332-0022 Japan

[8]WPI Advanced Institute for Materials Research, Tohoku University, 2-1-1 Katahira, Aoba, Sendai 980-8577 Japan

* TEL: +81-22-217-5555, E-mail: s-fukami@csis.tohoku.ac.jp

Abstract

We study the write and retention properties of magnetic domain wall (DW)-motion memory devices with the dimensions down to 20 nm. We find that the write current and time are scaled along with device size while sufficient thermal stability and low error rate are maintained. As a result, ultralow-power (a few fJ) and reliable operation is possible even at reduced dimensions.

Introduction

Nonvolatile spintronics memory, *e.g.*, MRAM, devices embedded into VLSIs allows one to eliminate the standby power and interconnect bottleneck (1). In particular, a three-terminal cell circuit with the spintronics device is advantageous from a view point of fast operation with a wide margin. This feature makes it possible to design various types of nonvolatile memory macros that can operate with the same clock frequencies as SRAMs (2,3). A DW-motion device is suitable for the three-terminal cell circuit (4). Up to now, the basic operation of the three-terminal cell with ~100-nm-wide DW-motion device has been successfully demonstrated (5,6). To apply it to leading-edge CMOS technologies, it is essential to investigate the properties of device with reduced dimensions down to a few tens of nm. In most memory devices, as the size decreases, one faces difficulties in managing write properties including error rate and retention property. Here, we study how the characteristics of DW-motion devices vary as their size decreases by evaluating devices with various widths down to 20 nm and discuss their scalability on the basis of the experimental results.

Device structure

Figure 1 depicts the structure of the three-terminal DW-motion MRAM device (3T-dev) (5,6). For writing, a DW pinned by pinning layers (PLs) is moved by applying a write current I_W to a free layer (FL); this is the key ingredient of the operation. To focus on the write and retention properties, we use Hall devices (Fig. 2) in which the anomalous Hall effect is used to detect the DW position. For the FL, a Co/Ni multilayer with perpendicular easy axis (5-10) is used. We fabricate the devices with various widths w. The average width of nominally 20-nm-wide devices is estimated electrically to be 19.9 nm from their wire resistances.

Experimental results and discussion

A. Write current and bit-to-bit distribution

Figure 3 shows the basic properties [resistance *vs.* magnetic field (*R-H*) and resistance *vs.* current (density) (*R-I*(*j*)) curves] of the 20-nm device. The critical magnetic field for DW depinning is 110 mT, which is about three times larger than that of a 100-nm device, whereas the critical current I_C is 85 μA, which is less than 1/3 that of a 100-nm one. Figure 4 shows the I_C and critical current density j_C as a function of w. The expected I_C in a 3T-dev is also plotted, where a shunt current to adjacent layers to the FL is corrected. The requirement for the smallest layout of the cell is I_C < 200 μA and this is satisfied at w < 100 nm. The j_C shows a minimum around w = 50 nm and increases as w decreases from the w due to the change in the DW structure (7); however, j_C for w = 20 nm is 6×10^{11} A/m^2, which is small enough in terms of both cell size and write endurance (8). The *R-j* curves for 80 devices are shown in Fig. 5a. The ratio of standard deviation to average (σ/ave) is

less than 10%. We reveal that the dominant factor of the bit-to-bit distribution is a self-distribution (Fig. 5b). We also note that results obtained from the Hall device grasp the essence of the write properties of a 3T-dev in which the DW is pinned by the PL (Fig. 6).

B. Retention

We measure the thermal stability, *i.e.*, retention property, of the 20-nm device. We use a retention time measurement under a DC magnetic field (Fig. 7a), which has been found to be effective in evaluating the thermal stability of DW-motion devices (9). The obtained results are well described by the Néel-Brown model (Fig. 7b). Based on a theoretical equation, the thermal stability factor Δ ($\equiv E/k_BT$) is determined to be 197 (Fig. 7c). Figure 8 shows Δ and intrinsic critical field H_{C0} as a function of w. Thanks to an increase in the H_{C0} with size reduction, Δ is size-independent and much more than 100 even at 20 nm. This is a great advantage of DW-motion devices since the I_C, independent of the H_{C0}, decreases while the thermal stability, dependent on the H_{C0}, does not degrade as the device size is reduced. Note that the increase in the H_{C0} with the size reduction is found to be a feature unlimited to the Hall devices.

C. Write time (DW motion velocity)

The write time t_W of a DW-motion device mainly depends on the DW-motion velocity v_{DW}. Figure 9 shows the measured v_{DW} for different w's. For all w's, $v_{DW} > 50$ m/s is obtained at $j > 1.4j_C$. Based on the measured v_{DW}, t_W is derived for each w as a function of applied current (Fig. 10). The t_W scales along with w just like the I_C and becomes about 1 ns for $w = 20$ nm; this is short enough to replace conventional volatile cells such as SRAMs.

D. Write error rate

Figure 11 shows the experimental and calculation results of the DW-depinning/motion error rate. We have found that the error rate steeply decreases with increasing j above j_C for a 160-nm device with 2-ns-long current pulses (10). The steep decrease is also found in the 40-nm device. A numerical calculation using one-dimensional Landau-Lifshitz-Gilbert (LLG) equation with thermal fluctuations (10) reproduces well the experimental results. From the fluctuation-dissipation theorem (11), it is concerned that a smaller w leads to a worse error rate due to a volume reduction because a random magnetic field originating from the thermal fluctuation is proportional to $1/\sqrt{\text{Volume}}$. However, numerical calculation reveals that the decrease in the error rate is sufficiently steep because of large H_{C0} at small sizes.

E. Summary

Table 1 summarizes the properties at small sizes. The derived power consumption for writing (a few fJ) is more than one order of magnitude smaller than that of the state-of-the-art two-terminal STT-MRAM (90 fJ) (12); this is mainly owing to the low resistance of the write-current path of the three-terminal DW-motion device (~100 Ω).

Conclusion

We confirm scalability of three-terminal DW-motion device down to 20 nm with $I_W < 100$ μA, σ/ave < 10%, $\Delta \gg 100$, $t_W \approx 1$ ns, and low error rate. Required power for writing is a few fJ, which is more than one order of magnitude smaller than the state-of-the-art values. These results indicate that the DW-motion device has high potential to be embedded into leading-edge and future CMOS technologies while possessing ultralow-power and nonvolatile features.

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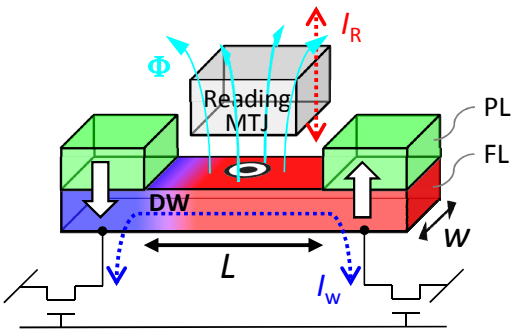

FIG 1: Structure of three-terminal DW-motion MRAM cell. DW is moved in free layer (FL) by applying write current I_W. Pinning layer (PL) fixes magnetization of both ends of FL and pins DW. Read current I_R is applied to reading MTJ, where tunnel magnetoresistance is changed according to stored data through magnetic flux Φ generated from FL.

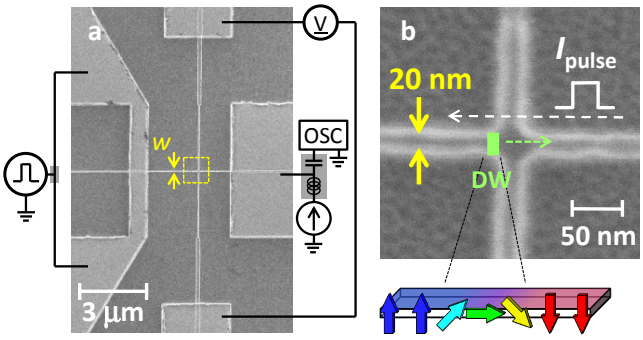

FIG 2: SEM image of Hall device we use. **a**) Low-magnification image with measurement circuit. **b**) High-magnification image of region inside dashed box in **a**. Device is patterned using EB lithography. Minimum width of wire is 20 nm.

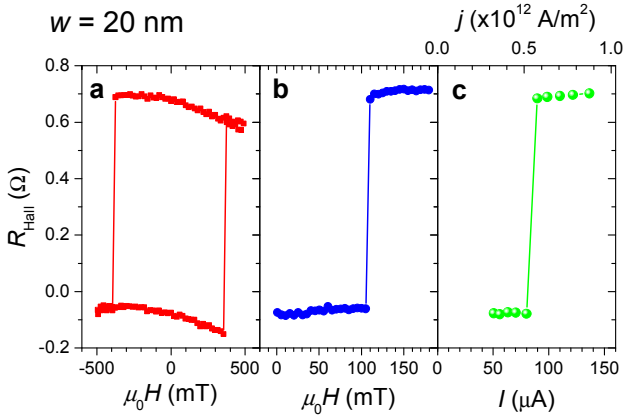

FIG 3: *R-H* and *R-I*(*j*) properties of 20-nm device. **a**) Major *R-H* curve. Switching field, *i.e.*, nucleation field, is 380 mT. **b**) *R-H* curve after preparing a DW. Required magnetic field to move DW, *i.e.*, depinning field, is 110 mT. **c**) *R-I*(*j*) curve of device with a DW. Required current to move it is 85 μA.

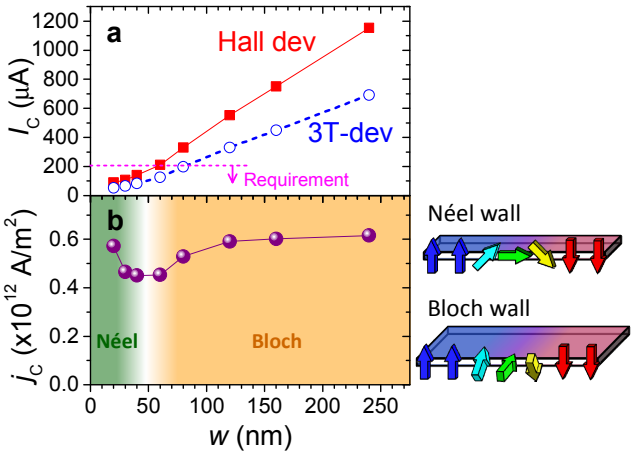

FIG 4: I_C (j_C) *vs. w*. Each plot is averaged value of 80 devices. **a**) I_C measured for Hall devices [closed squares] and calculated values for 3T-dev [open circles], where correction on shunt current is made. (Hall device leads to overestimation of I_C due to shunt current.) Horizontal broken line denotes requirement for the smallest layout of the cell (I_C < 200 μA). **b**) j_C. It has minimum at around 50 nm due to change in DW structure (Bloch wall/Néel wall) (7).

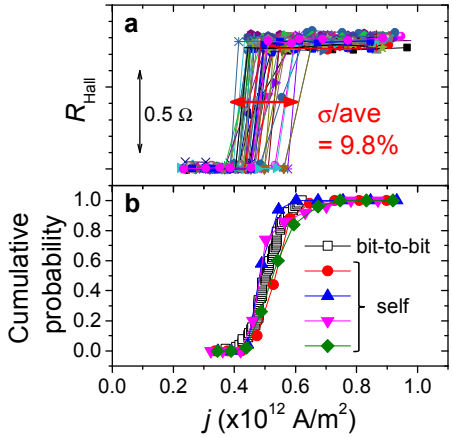

FIG 5: Bit-to-bit distribution of *R-j* properties of 40-nm devices. **a**) *R-j* curves of 80 devices. σ/ave of j_C is as small as 9.8%. **b**) Cumulative probability of DW motion as a function of *j* and its comparison with self-distribution of four devices. Dominant factor of bit-to-bit distribution is found to be self-distribution.

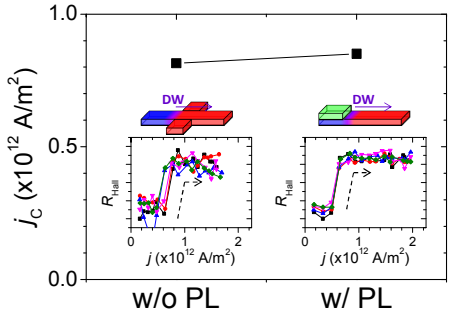

FIG 6: Comparison of *R-j* properties between devices with or without PL. Plots denote average value of 50 devices Inset shows *R-j* curves of each device. Equivalent *R-j* properties are obtained between the two. This indicates that Hall device we use grasps essence of write properties of 3T- dev shown in Fig. 1.

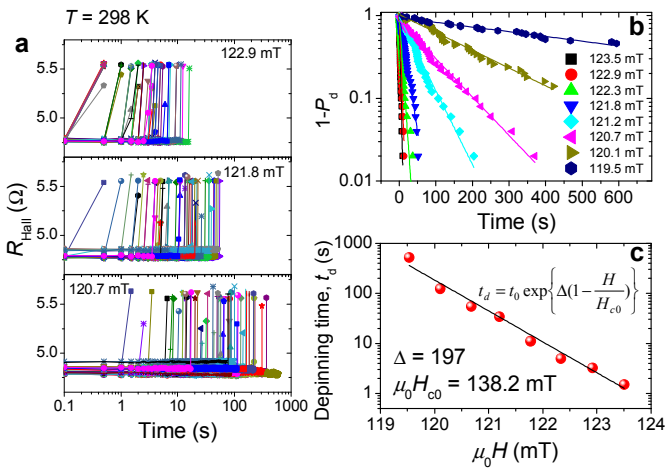

FIG 7: Measurement of retention property for 20-nm device. Hall resistance is measured at a regular interval (0.5 s) to detect DW depinning under an application of DC magnetic field. **a**) Time variation in Hall resistance for three magnitudes of magnetic field. Measurement is repeated 50 times. **b**) Probability of not depinning ($1\text{-}P_d$) as a function of time for various magnetic fields. Solid lines are fittings based on Néel-Brown model. **c**) Depinning time *vs.* magnetic field. Δ ($\equiv E/k_BT$) is derived to be 197 from theoretical equation denoted in the figure.

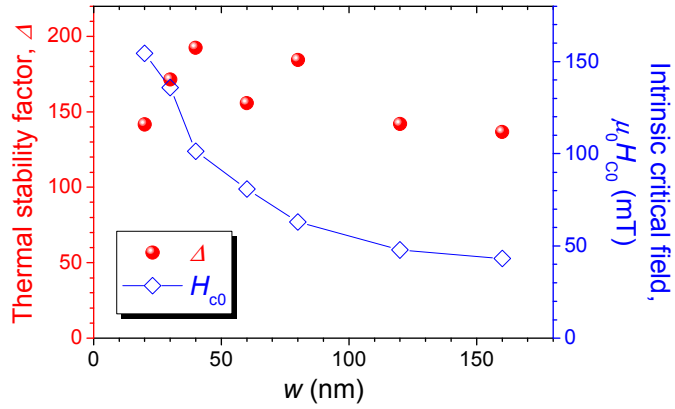

FIG 8: Δ and H_{C0} *vs.* w. Each plot represents averaged value of three devices. Δ is much more than 100 regardless of w down to 20 nm, whereas H_{C0} increases as w decreases.

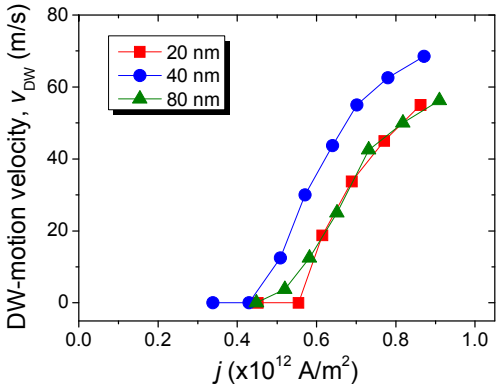

FIG 9: DW-motion velocity v_{DW} *vs.* current density j for devices with different w. In all devices v_{DW} becomes 50 m/s when j is about 40% larger than a certain threshold.

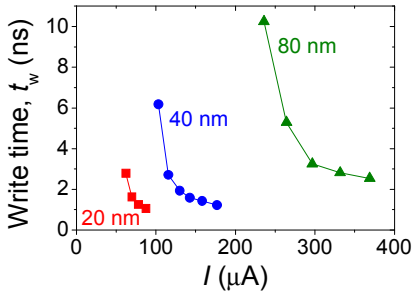

FIG 10: Write time t_W *vs.* applied current I for different w. t_W includes time for displacement and that for depinning; the latter is derived numerically. The t_W is scaled along with w.

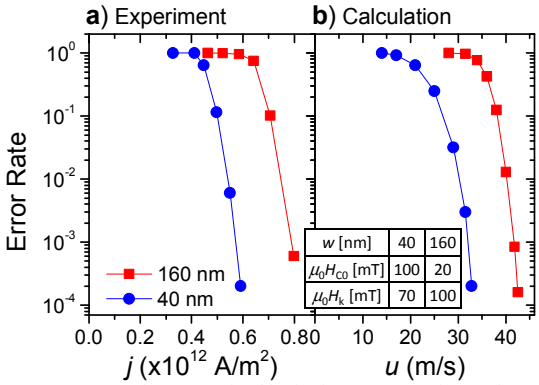

FIG 11: Error rate of DW motion/depinning. **a**) Experimental results for devices with different w. Steep decrease in error rate above a certain threshold is obtained regardless of w. **b**) Calculation results. 1D-LLG equation with thermal fluctuations is used. Table in figure shows parameters used for calculation. H_k denotes hard-axis anisotropy field (magnetic anisotropy field of DW).

Table 1: Summary of device properties based on the present experiments for 20-nm and 40-nm wide devices. w, width; L, length between two PLs (see Fig. 1); Δ, thermal stability factor (E/k_BT); j_W, current density for writing; I_W, current for writing; t_W, write time; R_W, resistance of write-current path; P_W, power for writing to 1 bit. Estimated P_W is more than one order of magnitude smaller than that of state-of-the-art two-terminal STT-MRAM (90 fJ) (12).

Parameter	Definition	Value	
w [nm]		20	40
L [nm]	$=w+2m+\delta_{DW}$ *1	49.2	74.2
Δ	$=E/k_BT$	>>100	>>100
j_w [TA/m^2]	$=1.3\times j_C$ *2	0.74	0.58
I_w [μA]	$=1.3\times j\times S$ *3	98	154
t_w [ns]	$=L/v + t_{dpn}$	1.26	2.56
R_w [Ω]	$=R_{sq}\times L/w$ *4	145	109
P_w [fJ]	$=R_w\times I_w^2\times t_w$	1.8	6.7

*1) Alignment margin m for each generation is extracted from ITRS. DW width δ_{DW} ($=\pi\sqrt{A/K_u}$) is assumed to be 15 nm.
*2) 1.3-times larger j_w than j_C is assumed for sufficiently low write error rate.
*3) 30% shunt current is assumed. S is section area of magnetic layer.
*4) Sheet resistance, R_{sq}, = 59 Ω/□.