An Ultra-Low-Power 868/915 MHz RF Transceiver for Wireless Sensor Network Applications

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***Abstract* — This paper describes an ultra-low-power RF transceiver implemented as part of a system-on-chip. The transceiver operates in the 868/915 MHz frequency band using binary FSK modulation at a 45 kbit/s data rate. It achieves -89 dBm receiver sensitivity and -6 dBm transmitter output power while consuming 1.6 mA and 1.8 mA, respectively, from a 1.2 to 1.5 V supply. It is fabricated in 0.13 µm CMOS occupying 1.5 mm^2, and it uses only four external components (i.e., battery, antenna, SAW-filter and crystal). The transceiver offers a small form factor, low cost and low power solution for wireless sensor network applications.**

***Index Terms* — Frequency shift keying, low power radio, RF transceivers, wireless sensor networks, crystal oscillators.**

I. Introduction

Wireless sensor networks (WSN) are an active field of research with numerous applications in industrial monitoring, patient monitoring, building automation, logistics tracking, etc. A WSN is made up of small nodes, each node consisting of one or more sensors, a wireless transceiver, a microcontroller and a power supply generally formed by a battery. Typical requirements for a WSN node are a small form factor, low cost and long battery life, which are generally pursued by means of miniaturization and power reduction.

As regards miniaturization, a high level of integration is essential implying a System-on-Chip (SoC) solution with minimum chip area and a minimum of external components. As regards power reduction, the power of a WSN node is typically dominated by the radio part. Both the average and the peak power should be reduced. The former to prolong battery life and the latter to enable the use of small form factor batteries such as zinc-air coin cells or flexible printed batteries, which can only sustain a few mA's of peak current at 1.5 V.

Although some low-voltage low-power transceivers for WSN applications have been reported [1]-[2], this paper presents an RF transceiver that uses less peak power, less chip area and less external components. In addition, it has a short start-up time to minimize energy wasted during wake-up. It enables a small form factor, low cost and long battery life for WSN nodes. The transceiver is part of a SoC further including asynchronous digital baseband and memory to be published in the future.

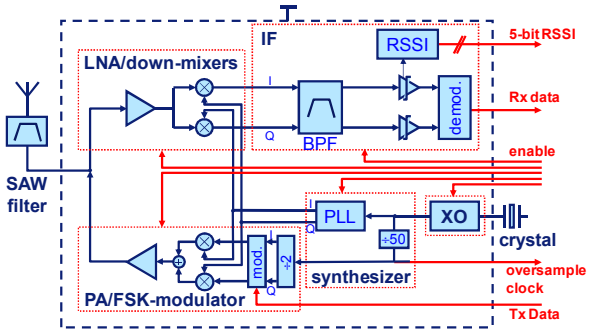

Fig. 1. Zero-IF architecture and block diagram for transceiver.

II. System Definition & Architecture

The transceiver targets the European 868-870 MHz (SRD) and North American 902-915 MHz (ISM) frequency bands, which have been chosen as a trade-off between path loss and power consumption on the one hand, and antenna size on the other hand. The modulation scheme is binary FSK, which is of a constant envelope allowing the use of efficient non-linear PA and overcoming the necessity for gain control at baseband. The data rate is kept relatively low to reduce transceiver complexity and power consumption.

To minimize the number of external components and the power consumption, the transceiver makes use of a zero-IF architecture as shown in Fig. 1. Typical drawbacks such as low-frequency noise and dc-offset errors are circumvented by using FSK with a high frequency deviation (of roughly ±180 kHz) and ac-coupling in the signal path. The transceiver consists of five blocks that can be separately enabled by the baseband. In receive mode, the low-noise amplifier (LNA)/down-mixers, IF, frequency synthesizer and crystal oscillator (XO) blocks are enabled, whereas in transmit mode, the power amplifier (PA)/FSK-modulator, frequency synthesizer and XO blocks are enabled. Note that no use is made of external RF-switches, inductors, impedance matching, etc. The transceiver uses four external components: an

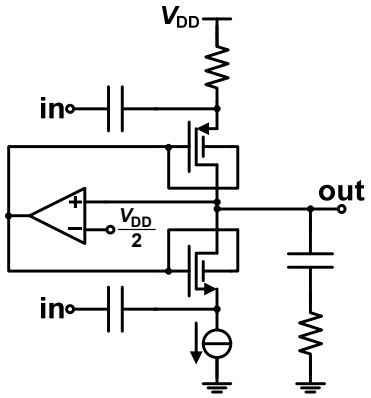

Fig. 2. Simplified LNA schematic.

antenna, a SAW band-pass filter, a crystal, and a battery. The nominal battery supply voltage is 1.5 V. A different crystal and SAW filter need to be used for the 868 and 915 MHz frequency band. In Fig. 1, the oversample clock output is used in the asynchronous digital baseband to process in- and outgoing data, and it thus determines the data rate. The data rate is $1/8^{th}$ of the oversample clock, which is $1/50^{th}$ of the crystal frequency. The FSK frequency deviation f is divided down (by a factor of 100) from the crystal frequency.

The radio targets a 10 m range. Based on the architecture in Fig.1, this translates to a required -89 dBm sensitivity and -6 dBm output power assuming a 10 m line-of-sight loss of -51 dB at 900 MHz, an additional fade margin of 20 dB, and 6 dB RF front-end losses (due to antenna and SAW filter).

III. Circuit Implementation

The transceiver is implemented in a 6 metal 0.13 μm general-purpose CMOS technology with mixed-signal options such as ultra thick top metal, MiM-capacitors and deep n-well. In this Section, we will briefly discuss the circuit implementation of all five transceiver blocks. Each block contains an on-chip LDO (with bandgap reference) that regulates the 1.5 V battery supply down to an internal 1.2 V supply. To keep the chip area small, the use of on-chip inductors is avoided where possible. To minimize power consumption, MOS transistors are biased at threshold (where the gm-over-I ratio is maximum) and current re-use is applied where possible. Further care is taken to keep the start-up time of each block small.

A. Low-Noise Amplifier (LNA) & Down-Mixers

The LNA is designed to achieve 50 input impedance, high voltage gain and low noise figure at minimum power; it is shown in Fig. 2. The LNA comprises a common-gate configuration with current re-use making use of feedback for dc-biasing. Each common-gate MOSFET has its gate and bulk short-circuited which effectively reduces threshold voltage enabling a more efficient use of voltage headroom. The LNA is coupled to the quadrature down-mixer, which uses a double-balanced Gilbert cell configuration with current bleeding *p*-MOSFET. The mixer outputs have a first-order low-pass characteristic with a 1 MHz cut-off frequency, and are ac-coupled to the analog IF-part.

Simulations of the RF front-end show 31 dB voltage conversion gain, 7.3 dB noise figure and a wide-band |S11| < -10 dB at a supply current of 770 μA.

B. IF-block

The analog IF part of the receiver contains a channel selection filter, a limiting amplifier with 5-bit RSSI functionality and a demodulator, see Fig. 1. A special focus is on reliable reception, which is achieved by implementing the sensitive parts of the I and Q paths differentially, and by making use of a channel selection filter with a high out-of-band suppression and a high dynamic input range.

The channel selection filter is a 3^{rd}-order Chebyshev filter. Its first pole is implemented passively in order to achieve high linearity at low power consumption. The required inductor uses a g_m-C implementation to achieve a good dynamic range while using little power and area. The limiting amplifier consists of five cascaded differential band-pass amplifiers, each with 12 dB gain. The output of each band-pass amplifier in the I path contains a level detector to generate one bit of the RSSI signal.

A final high gain stage provides fully saturated rail-to-rail input signals for the binary FSK demodulator. The demodulator contains four edge detectors, for the rising and falling edges of both I and Q. On every edge of I and Q, the Q and I signals are sampled, respectively, giving an instantaneous indication whether a digital one or zero has been transmitted. This digital value is forced upon a single latch. In the digital baseband, the buffered latch output (Rx data in Fig. 1) is sampled, a time average running over one bit period is calculated and the non-synchronized raw data is then further processed.

C. Power Amplifier (PA) & FSK Modulator

The primary design challenge of the PA is to efficiently drive a constant-envelope low-power RF signal (ranging between -6 and 0 dBm) in a 50 load without using inductors. The most efficient output power is determined by the load impedance R_{LOAD} and the available output voltage swing $v_{out,max}$:

$$P_{out,eff} = \frac{v_{out,max}^2}{2 \cdot R_{LOAD}} \quad (1)$$

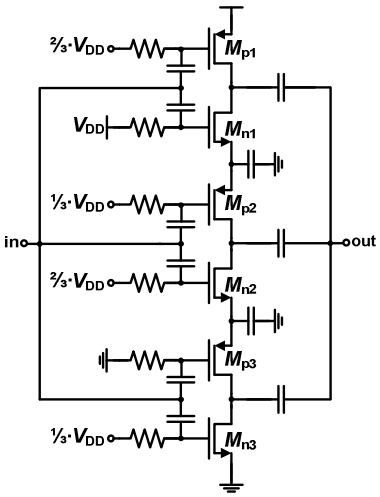

Fig. 3. Stacked push-pull class A/B power amplifier for efficient low-power output.

As R_{LOAD} is fixed, we need to reduce $v_{out,max}$ in order to design an efficient PA with very low power output. Extending the approach in [3], this is achieved by using a triple stacked 50% duty-cycle push-pull amplifier as shown in Fig. 3, where $v_{out,max}=V_{DD}/6$. For optimum overall efficiency the power amplifier is directly connected to 1.5V battery supply; it is driven by two cascaded inverters running at 1.2 V internal supply. Devices were sized to minimize the overall dissipated power in the driver and the push-pull transistors. The simulated output power is -2.4 dBm at 53% efficiency for the power amplifier or 38% efficiency including the inverter driver stages.

The FSK-modulator combines quadrature LO signals and frequency deviation (f) signals to form a single FSK-modulated signal depending on the transmit data input (TX), see Fig. 4. The FSK-modulator mainly comprises an SSB-mixer using a novel digital implementation in which the multiplication function is replaced by the exclusive-or function and the summation function is replaced by the AND or NOR function; the set-reset latch combines the outputs of the AND/NOR to deliver 50% duty-cycle (needed to efficiently use the PA). The simulated supply current of the FSK-modulator is 110 µA.

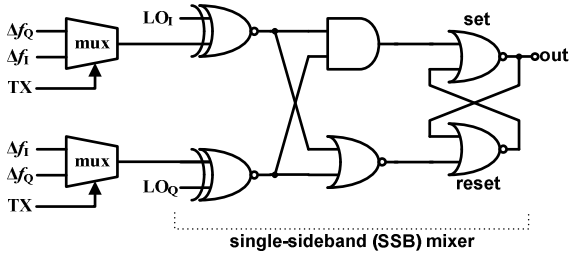

Fig. 4. Digital implementation of FSK-modulator; output frequency is $f_{LO}+f$ for TX=1 and $f_{LO}-f$ for TX=0.

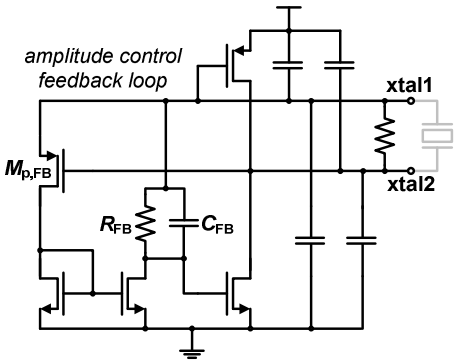

Fig. 5. Low-power crystal oscillator.

D. Frequency Synthesizer

The frequency synthesizer is an integer-N PLL consisting of an I/Q-VCO, feedback divide-by-48 frequency divider, a phase-frequency detector/charge pump combination, and an on-chip loop filter. It uses an 18.103 or 19.026 MHz crystal reference frequency to generate differential quadrature output signals of 869 or 915 MHz, respectively. The I/Q-VCO comprises an *LC*-VCO (running at twice the output frequency), a buffer and divide-by-2 frequency divider. The *LC*-VCO incorporates the only on-chip inductor used in the transceiver; it has a quality factor of 16 at 1.8 GHz. According to simulations, the PLL drains 570 µA at 1.2 V supply and it starts-up and locks within 10 µs.

E. Crystal Oscillator (XO)

The XO-block provides the 18.103 or 19.026 MHz reference input to the frequency synthesizer. While using only a crystal as an external component, it is designed to achieve ±30 ppm frequency accuracy, low phase noise and low power. The XO-core makes use of an inverter-based Pierce oscillator extended with a feedback loop controlling the oscillation amplitude to reduce power

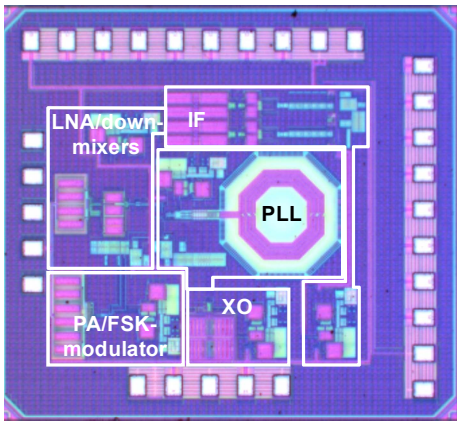

Fig. 6. Photo of RF-transceiver test chip in 0.13 µm CMOS.

TABLE I
TRANSCEIVER BLOCK MEASUREMENTS @ 1.5 V SUPPLY

transceiver block	supply current (µA)	wake-up time (µs)
LNA/down-mixers	898	<20
IF	77	<100
PA/FSK-modulator	1143	<20
Frequency Synthesizer	611	<20
Crystal Oscillator	18	1200

consumption, see Fig. 5. At small amplitudes, the inverter transconductance g_m is high to ensure fast and reliable start-up. With increasing amplitude, g_m decreases until the amplitude saturates at a relatively small value ensuring low power. The XO-core is followed by a buffer that translates the differential output to a single-ended rail-to-rail signal without significantly affecting the phase noise.

IV. MEASUREMENT RESULTS

The RF-transceiver test chip (including bond pads for all inputs and outputs) is shown in Fig. 6. The chip area is 1.6×1.4 mm^2, which reduces to 1.4×1.1 mm^2 when the transceiver is incorporated in a SoC combining RF & baseband, where most inputs/outputs remain on-chip.

All transceiver blocks have been tested separately as well, their respective supply current is summarized in Tab. I. The LNA/down-mixer block shows a 32 dB voltage conversion gain, a 10 dB noise figure and a -22 dBm IIP3 (with spurs at 300 and 400 kHz). It further shows good impedance matching of -13.4 dB |S11| at 900 MHz. The IF-block performs band-pass filtering between 70 kHz and 400 kHz. The PA delivers -4 dBm maximum output power with 32.4% overall efficiency (47.6% efficiency for the output stage). The digital FSK-modulator is functional but has sub-optimum performance in combination with the PA. As a consequence, the PA/FSK-modulator combination only delivers -6 dBm. This will be improved in a redesign. The I/Q-VCO has 175.5 FOM and 825 to 983 MHz tuning range covering the frequency bands of interest. The frequency synthesizer shows -97 and -121 dBc/Hz phase noise at 100 kHz and 10 MHz offset, respectively. The XO shows -128 dBc/Hz phase noise at 100 kHz offset.

TABLE II
MEASURED TRANSCEIVER IC PERFORMANCE

	parameter	value	unit
general	operating frequency	862• 870 (EU) 902• 928 (NA)	MHz
	data rate	45 (EU) 48 (NA)	kbit/s
	frequency deviation	181 (EU) 190 (NA)	kHz
	chip area (incl. pads)	1.5	mm^2
	CMOS technology	0.13	µm
	external components	4	•
	supply voltage	1.2• 1.5	V
	sleep current	0.8	µA
receive mode	supply current	1.6	mA
	sensitivity (@BER=0.1%)	-89	dBm
	max input signal	-10	dBm
	LO leakage	-90	dBm
transmit mode	supply current	1.8	mA
	output power	-6	dBm

Typical measurement results for the RF-transceiver are summarized in Tab. II. The transceiver sensitivity and transmit output power meet the requirements as discussed in Section II.

V. CONCLUSION

This paper describes an ultra-low-power RF transceiver operating in the 868/915 MHz ISM frequency band using binary FSK modulation at a 45 kbit/s data rate. The transceiver achieves -89 dBm receiver sensitivity and -6 dBm transmitter output power while consuming 1.6 mA and 1.8 mA, respectively, from a 1.2 to 1.5 V supply. It is fabricated in 0.13 µm CMOS occupying 1.5 mm^2, and it uses four external components (i.e., battery, antenna, SAW-filter and crystal). The new RF-transceiver uses less chip area, less external components, less wake-up time and less peak power than similar radios in the same frequency bands [1]-[2]. As such it offers a small form factor, low-cost and low-power transceiver solution for wireless sensor networks.

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