A new logic family based on hybrid MOSFET-polysilicon nanowires

S. Ecoffey, M. Mazza, V. Pott, D. Bouvet, A. Schmid, Y. Leblebici, M.J. Declercq and A.M. Ionescu

Institute of Microelectronics and Microsystems, Swiss Federal Institute of Technology Lausanne, Switzerland

Abstract

A new logic family based on ultra-thin film (10nm) nanograins (5 to 20nm) polysilicon wires (polySiNW) is proposed, validated and studied. This logic family can be operated from 4K up to 400K and hybridized with conventional CMOS. Ultra low power dissipation in the order of hundreds of pWs has been observed, which is outperforming CMOS technology, in terms of power consumption, by orders of magnitude.

Introduction

One-dimensional nanostructures have demonstrated their ability to realize new building blocks for nanoelectronics. Silicon nanowires (SiNW) and carbon nanotubes (CNT) are the most credible candidates for future nanosystems (1-3), especially in a CMOS hybridization perspective. Room temperature operation and novel functionality are considered to be priorities for the success of new nanotechnologies.

A CMOS-compatible lithography fabrication process for polySiNW build on ultra-thin nanograin films has been proposed recently (4) as depicted in Fig. 1, allowing the development of novel applications such as low power memory and negative differential resistor (5). In this paper, a new logic family using the same technology is presented.

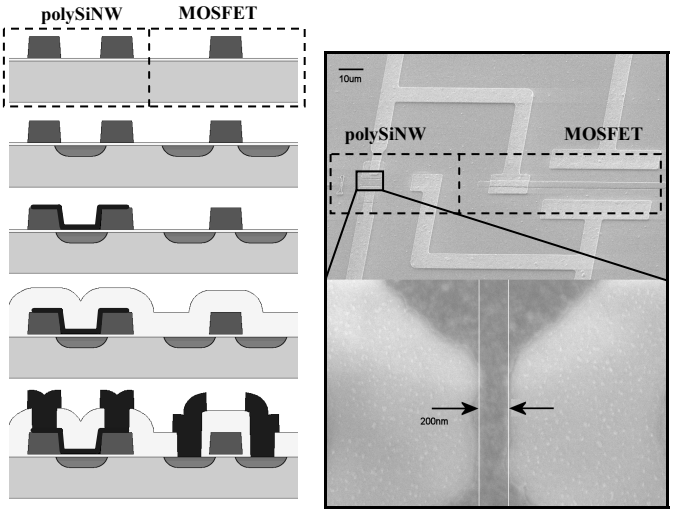


Fig. 1: Simplified process flow for hybrid nMOS-polySiNW co-fabrication and die photo of fabricated hybrid circuit. The gate oxidation is followed by thick polySi deposition and patterning. An auto-aligned implantation of both the gate of the polySiNW and the source/drain of the nMOS transistor is then performed. Thin polySi is deposited, "hot" phosphorous implanted and etched to obtain the polySiNW. LTO oxide is deposited for passivation and AlSi is finally sputtered and structured for contacting both the polySiNW and the nMOS transistor. The detailed process flow was described in (4).

PolySiNW electrical characterization

Typical widths and lengths of the gated polySiNW are W = 0.2 to 0.5µm and L = 0.5 to 2µm. Gate oxide thicknesses of 20nm and 40nm are used to obtain a very low gate current leakage. Fig. 2 shows the V-shape (log scale) I_{DS}-V_{GS} characteristics of the fabricated thin film polySiNWs; the V-shape is explained by ambipolar conduction. Band-to-band tunneling is responsible for the 2nd negative slope region of I_{DS}-V_{GS} (see Fig. 2, family of curves for N_D=7x10^{19}cm^{-3}). Fig. 3 reports the original proposed operation of the polySiNWs: at constant injected current of the order of tens to hundreds of pAs, unique V_{DS}-V_{GS} output characteristics with two negative slopes are reported. A unique hysteresis appears when the polySiNW device is biased at constant current (see Fig. 4). We explain this hysteresis by the electrical field assisted charge trapping in the nano-sized grains of the ultra-thin 10nm polysilicon film. The positions of the negative slope and hysteresis of the V_{DS}-V_{GS} characteristic can be tuned with the injected current (in the order of tens to hundreds of pAs). Extensive measurements over large number of devices at the wafer level and from wafer to wafer have shown that the unique polySiNW characteristics are highly reproducible.

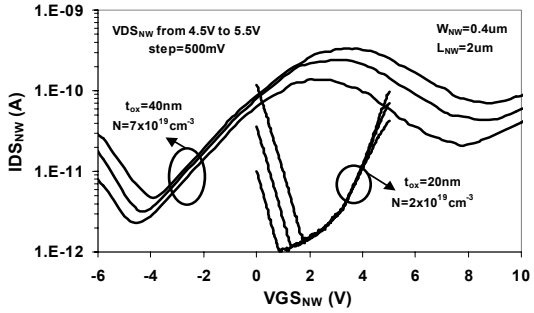


Fig. 2: IDS_{NW}-VGS_{NW} characteristics. Both characteristics present a V-shape at low gate voltage whereas only the one with the thicker oxide (40nm) and higher phosphorous doping shows a second negative slope region explained by band-to-band tunneling conduction.

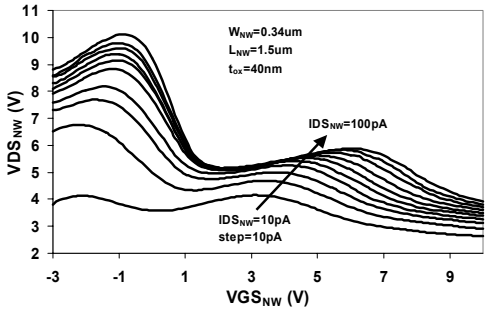


Fig. 3: Transfer characteristics of a polySiNW at various constant current. Two negative slope regions are clearly transferred.

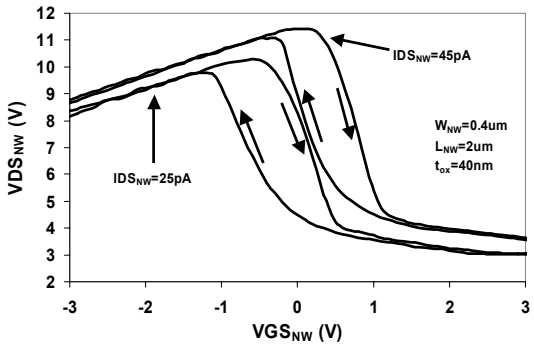


Fig. 4: Typical measured transfer characteristics *with hysteresis*, VDS_{NW}-VGS_{NW}, at constant current (*basic biasing scheme* for the proposed logic) at room temperature.

Non-conventional logic scheme

Large-scale digital systems are based on a layered arrangement of combinatorial logic circuits to be placed in between register stages. The arrangement of three nanowire devices which is depicted in Fig. 5 composes a versatile digital gate taking benefit of the hysteresis behavior to synthesize the basic range of digital functions (NAND, NOR and Flip-Flop) required to construct complex digital systems. The proposed gate is composed of a nanowire N1, which is operated in turn as an input precharge device and subsequently as the first gate input variable A. The nanodevice N2 is operated as two-level current source. The switching of N2 is dependent on the state of the second gate input variable B. The nanowire N3 is used as a constant current source biasing the system to its operating point.

The proposed circuit operates with a two non-overlapping clock phase scheme consisting of a precharge followed by a logic evaluation phase. The circuit can be used in several working modes to produce various Boolean functions. The synthesis of a logic two-input NAND is depicted in Fig. 6, where A and B stand for the input variables, and U the output variable. The possible binary states are Logic 0 and Logic 1. An output noise margin has been considered, and is represented as a grey portion on the output axis V_{DS}. The ideal transfer function has been plotted over measurement results in grey.

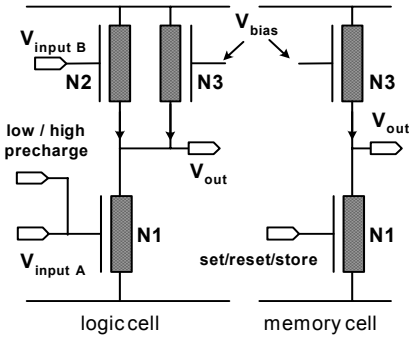
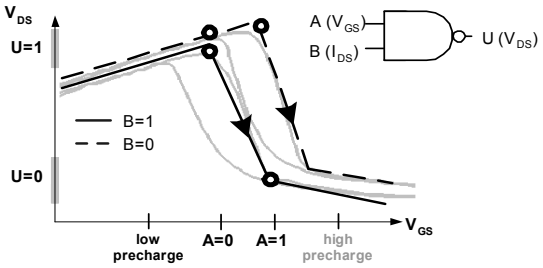


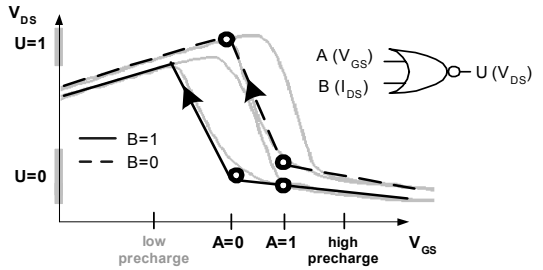
Fig. 5: Versatile digital function generator circuit, and memory cell configuration.

The generation of a result is a dynamic process starting with a low-precharge of the circuit input to a predefined voltage level. Input variable B dictates the limits of the hysteresis loop in the input-output space, and is applied during precharge. The arrowheads show alternate paths on the hysteresis curves that are selected with respect to the actual state of B. Input variable A is applied during the evaluation phase as a biphasic voltage increase of a calibrated amplitude depending on the input variable state. The proposed versatile gate circuit can be operated in an alternate symmetrical operation mode where high-precharge is considered in replacement of the described low-precharge phase. The circuit operation sequence is similar to the previous case and allows synthesizing various NOR operators, as depicted in Fig. 7. Similarly, a flip-flop cell based on the hysteresis property of the nanowire is shown in Fig. 8. Biased with a steady current the polySiNW can be used to store a binary value, this value is kept indefinitely while the gate voltage is constant at "store" level. When the gate voltage is moved to set or reset value, the stored value is changed.



Resting State: DISCHARGE	A (V_{GS})	B (I_{DS})	U (V_{DS})
STANDARD Voltage Perturbation A	0	0	1
	0	1	1
	1	0	1
NAND	1	1	0

Fig. 6: Proposed boolean NAND transfer function. Principle: *black* curves, measurement (extracted from Fig. 4): *grey* curves.



Resting State: PRECHARGE	A (V_{GS})	B (I_{DS})	U (V_{DS})
STANDARD Voltage Perturbation A	0	0	1
	0	1	0
	1	0	0
NOR	1	1	0

Fig. 7: Proposed boolean NOR transfer function. Principle: *black* curves, measurement (extracted from Fig. 4): *grey* curves.

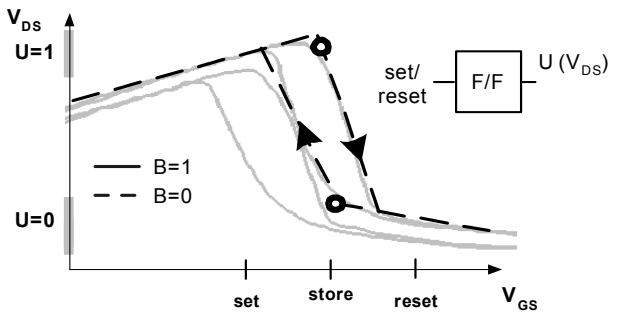


Fig. 8: Proposed transfer function of the flip-flop cell. Principle: *black* curves, measurement (extracted from Fig. 4): *grey* curves.

Practical use of the proposed polySiNW logic involves CMOS co-integration for interfacing. Fig. 9 shows a simple common source amplifier used as a buffer/amplifier. Current tunable MOS drain current versus polySiNW gate voltage characteristics are presented in Fig. 10. Principle schema for a NW-based memory cell with less than 1nW/bit power consumption in the storing state, almost infinite retention time (5) and fast read time (standard MOS technology) is depicted in Fig. 11.

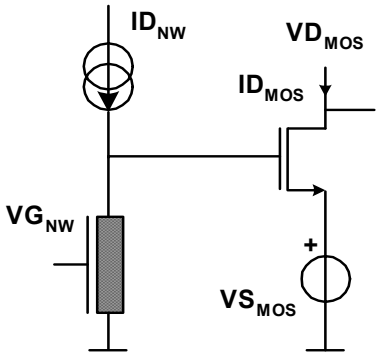


Fig. 9: MOS output interface for a single polySiNW memory cell.

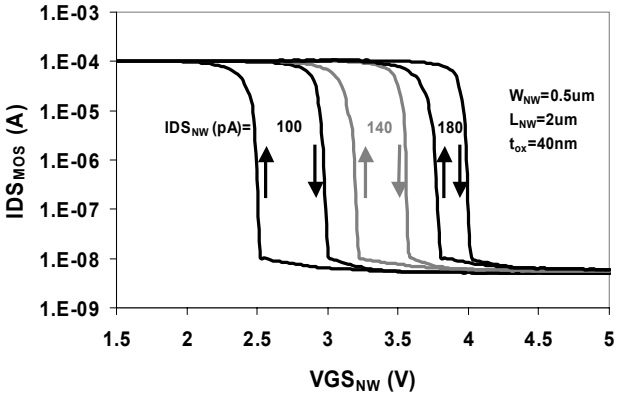


Fig. 10: MOS drain current versus nano-wire gate voltage transcharacteristics: an extremely abrupt negative slope is transferred to the MOSFET current.

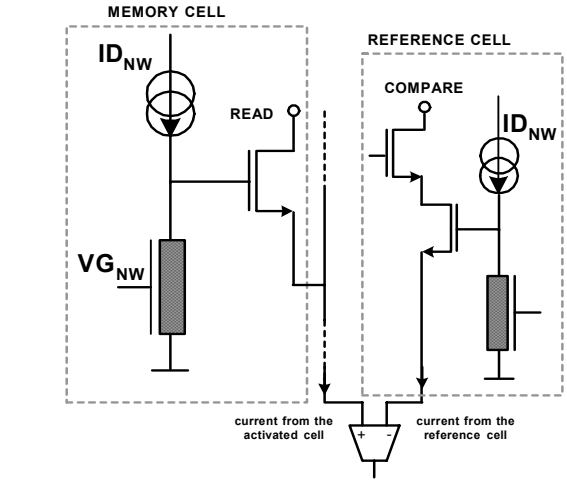


Fig. 11: PolySiNW-based memory cell, with CMOS interface.

Temperature dependence of polySiNW characteristics

Finally, we show that for the proposed polySiNW and architectures using constant current bias scheme, the temperature does not significantly affect neither NDR slope nor the hysteresis width. Combined with differential current sensing, *an excellent and unique memory capability is preserved even at high temperature operation*. Fig 12 shows the V_{GS}-V_{DS} characteristics of a polySiNW biased at constant current as a function of temperature (from 4K up to 125°C). The hysteretic behavior is preserved up to 100°C and began to be degraded at higher temperatures. Two hybrid CMOS-polySiNW transfer characteristics are also reported over temperature on Fig. 13. Two different biasing conditions are used, illustrating *the possibility to compensate the temperature drift by an adequate current injection and/or biasing conditions*. The abrupt negative slope (-40mV/decade, in excess of the subthreshold slope theoretical limit of a conventional MOSFET, obtained here due to the transfer of polySiNW characteristic to the MOSFET) and hysteresis are both well preserved despite the increase of temperature.

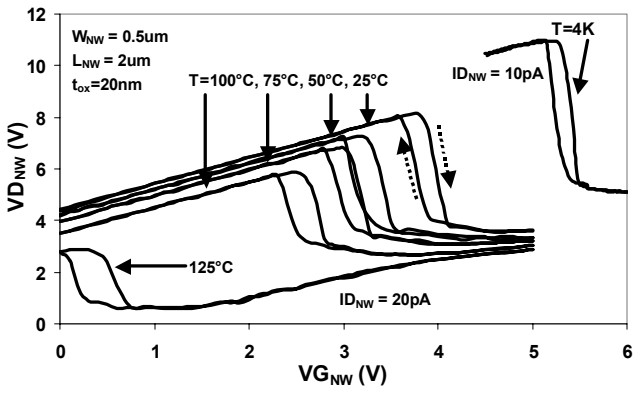


Fig. 12: Experimental temperature dependence of polySi-NW hysteretic transfer characteristics at constant current bias from 4K to 125°C. Thermal drift can be compensated back by properly selecting the injected current.

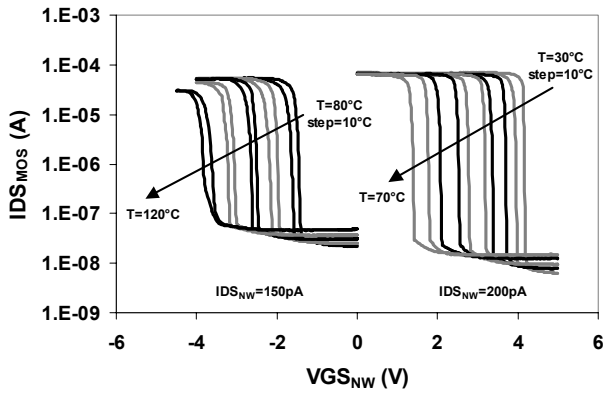


Fig. 13: Temperature dependence of hybrid MOSFET-polySiNW hysteretic characteristics at constant current bias. Hysteresis width and associated negative slope are almost insensitive to temperature variation, while the reference voltage provided by the very abrupt negative slope varies almost linearly with the temperature.

Measurements at low temperatures, from 4.1K up to 250K (Fig. 14 and Fig. 15) have shown two different thermally activated conduction mechanisms. Above 150K, conduction is dominated by *thermally activated hopping* over the barrier at the polySi grain boundaries.

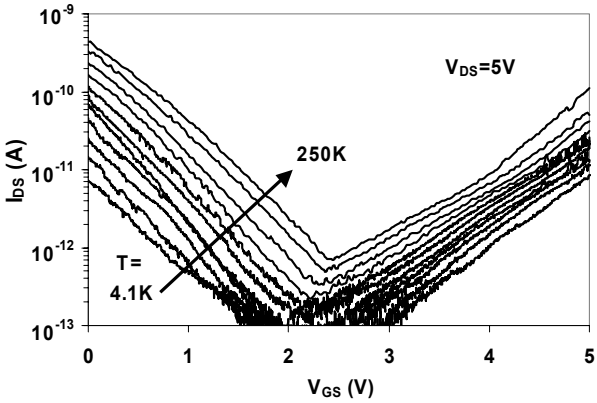


Fig. 14: Temperature dependence of V-shape (ambipolar) characteristics of thin film (10nm) highly doped (>10^{19}cm^{-3}) gated polySiNW with grain sizes randomly distributed between 5 and 20nm.

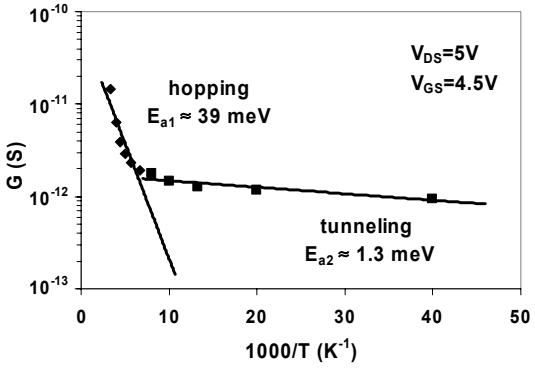


Fig. 15: Conductance, $G=dI_{DS}/dV_{GS}$, of a polySiNW versus 1000/T (data extracted from Fig. 14) showing two conduction mechanisms with two associated activation energies.

The activation energy E_{a1} related to this mode of conduction is calculated by using the Arrehnius law (6) between conductance, G, and activation energy, E_a :

$$G = \frac{dI_{DS}}{dV_{GS}} \propto \exp\left(-E_a \big/ kT\right)$$

where *k* is the Boltzmann constant and *T* the temperature.
Below 80K, the thermal carrier energy is too low to turn on the hopping mechanism. At this range of temperature, *the conduction is only controlled by a thermally assisted tunneling process* through the barrier with a second activation energy E_{a2} of ~1.3meV.

Conclusion

The proposed polySiNW exhibits very specific electrical charateristics as a V-shaped I_{DS}-V_{GS} and histeretic behavior in the transfer function that can be exploited in the development of logic gates with a novel dynamic operation scheme. The proposed nanowire-based gate proves to be a versatile circuit supporting hard and soft programmability of various logic functions that have been experimentally synthesized. Further cascaded operation of several nanowire gates is theoretically possible, and requires a modification of doping levels in order to satisfy the noise margin criteria. Room temperature operation, and very good stability of the transfer functions over a wide range of temperature have been observed. Extensive measurements have confirmed the reproductability of the electrical characteristics. Thus, the proposed nanoelectronic technology proves to be an interesting candidate for the high-density integration of hybrid digital designs.

Acknowledgements

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