Current status of the phase change memory and its future

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Abstract

With the increasing challenge of scaling floating gate non-volatile memory technology to beyond 65 nm, alternative memory technologies are being investigated. Chalcogenide based phase change memory (1) is one of the alternative memory candidates. In this review, the physics and operation of phase change memory will first be presented, followed by discussion of current status of development. Finally, the scaling capability of the technology will be presented. The scaling projection shows that there is no physical limit to scaling down to the 22 nm node with a number of technical challenges being identified.

Introduction

Chalcogenide phase change memories are being studied as a candidate for next generation non-volatile memory. The basic phase change material is a GeSbTe alloy and is the same family of material used in optical re-writable CD/DVD RW

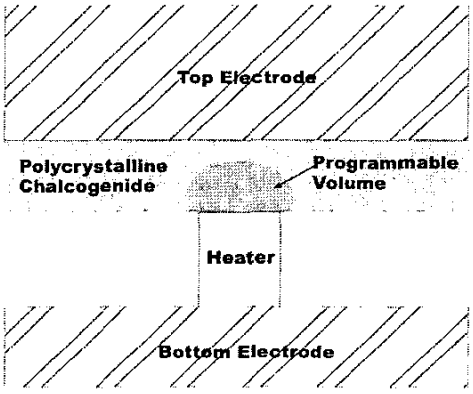

Figure 1: Basic cross section of the phase change memory

disks (2). In the optical disk application, a laser beam with different intensity is used to heat a small volume to switch the material between crystalline and amorphous states. The memory state is determined by reflectivity of the memory layer. In the phase change memory (Fig. 1), electric current of different magnitudes are passed from a heater element to the chalcongenide material and local joule heating is used to change the programmable volume around the contact region. Higher current and fast quenching freezes the material to an amorphous state giving high resistance. The time required for switching to amorphous state is typically less than 10-30 nSec, and the thermal time constant of the cell structure is typically a few nSec only. Figure 2 shows the 3D temperature profile for a typical current pulse (3, 4). It can be

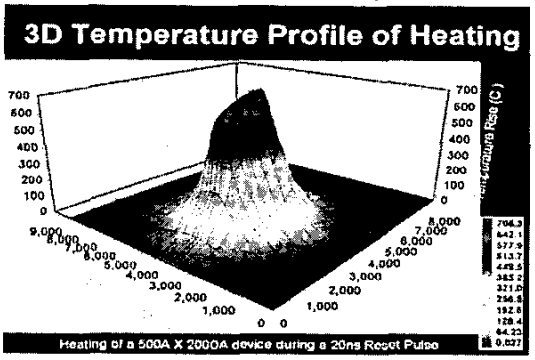

Figure 2: Temperature profile for amorphous state switching

seen that only a small volume of material is being heated to above 650C, sufficient to switch to amorphous state. The temperature drops off quickly and in less then a cell distance away, the material stays below the melting temperature and does not go through a phase change. Medium current for longer pulse time is used to re-crystallize the region to a crystalline state, which has low resistance. A much lower

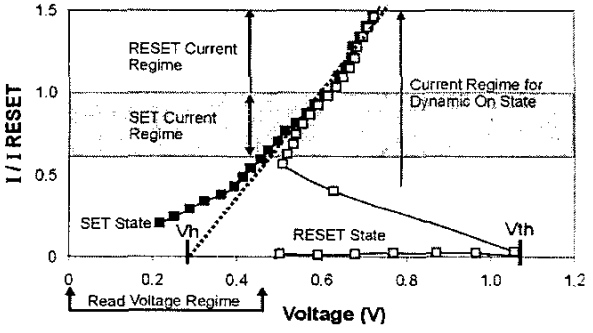

Figure 3: IV curve of basic memory element

current with essentially no joule heating is used for reading the memory, differentiating between the high (amorphous) and low (crystalline) resistance states. Figure 3 shows the basic IV curve of the memory device. A negative resistance is observed when the material switches from a high resistance off state to a low resistance on state used for programming. Once the device current exceeds a minimum level, the IV curves are the same independent of the initial memory state or phase of the material. This gives the direct write characteristics of the memory. This direct write capability

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simplifies the writing to the memory and improves write performance of the memory.

Current Status

The basic phase change memory has been demonstrated by several different research groups (5, 6, 7). There are three areas of focus in current development: 1. Cell physics study, 2. Cell program current reduction and 3. High density array manufacturing development. All three focus areas will be discussed in this paper.

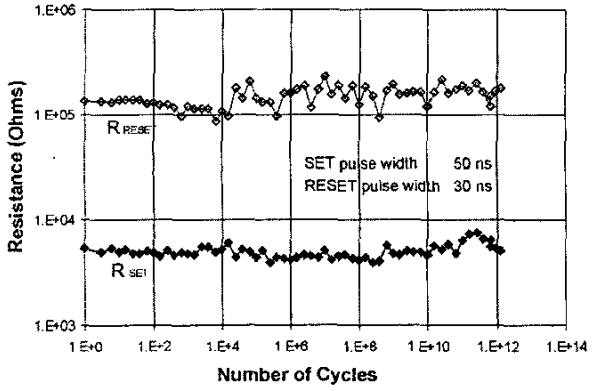

Figure 4: Cycling of phase change memory element

The single cell performance has been studied in detail. Figure 4 shows the cycling capability of a memory element. Up to one trillion cycle capability is demonstrated. It has been observed that there is a dependence of cycling capability with the magnitude of reset current (Fig. 5): over heating the cell with high current gives reduced number of cycles with the failed cells stuck at low resistance states. The failure mechanism is not well understood. Another cell failure observed is stuck reset, possibility due to open circuit at the contact region after large number of cycles. Improvement and optimization involve study of different electrode materials as well as change in composition of chalcogenide alloy. To compete as a non-volatile memory, retention characteristics are important. It was shown that the crystallization of the intrinsic material has high activation energy of 3.47 eV (Fig. 6) and extrapolated retention time at 85C is orders of magnitude more than the 10 year goal. However, it is expected that in high volume manufacturing, extrinsic defect mechanisms will dominate retention characteristics.

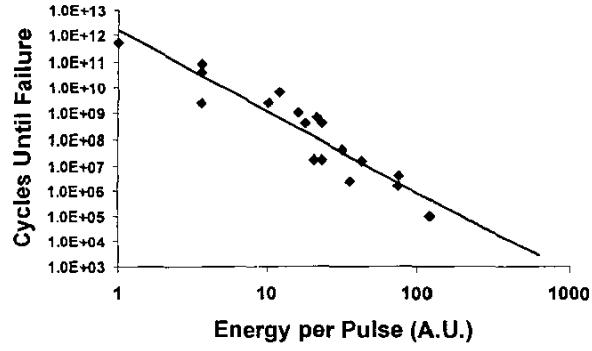

Figure 5: Cycling capability as function of programming energy per pulse

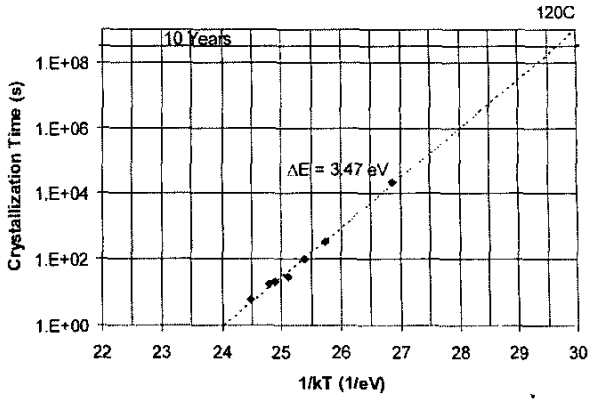

Figure 6: Intrinsic retention characteristics of phase change material

The second focus area of recent development is switching current reduction. The programming current is typically

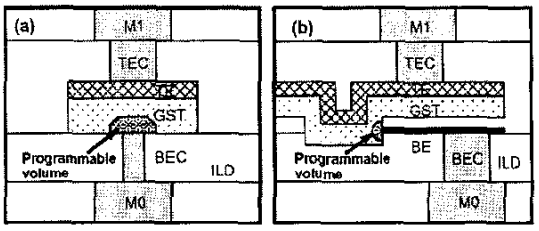

Figure 7: Edge contact to reduce switching current

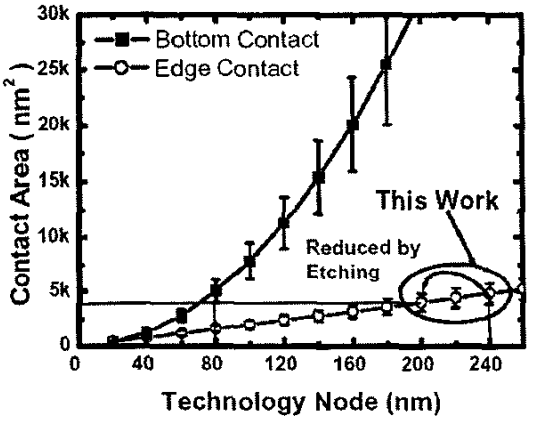

Figure 8: Edge contact current reduction

larger than 1 mA based on 180 nm lithography. For practical products, it is desirable to reduce the current to few hundreds of uA. The programming current scales with the contact area and improves with lithography scaling. One of the more innovative ideas to reduce programming current is the edge contact (Fig. 7) reported by Y.H. Ha, et al (8). The contact area is determined by a thin film thickness in one dimension and very low programming current is achieved (Fig. 8). Another idea for improvement is to dope the chalcogenide material with nitrogen (9) based on research work on rewritable optical memory disks. Higher resistance material is achieved by nitrogen doping and this leads to reduced programming current.

The third focus area is the study of array architecture and statistical manufacturing and reliability learning. In an array construction, either a transistor or a diode is required for switching the memory element. In order to achieve the

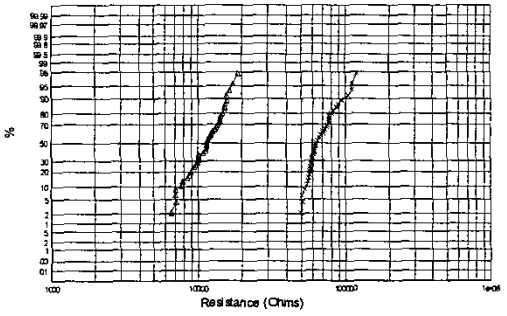

Figure 9: Set and reset resistance distribution in memory array

smallest cell size, the diode selection device is preferred. Given the fact that one is trying to sense change in resistance, parasitic paths of series resistance as well as leakage current are very important. A 4Mbit test chip has been fabricated based on 180 nm lithography. Figure 9 showed the resistance distribution in a memory array. The array distribution is wider compared to single cells due to parasitic effects but there is still a good operating window between the highest resistance set bit and the lower resistance reset bit. Another challenge in array construction is the fact that wordlines are required to pass the relatively large reset current, as opposed to the case of a floating gate transistor where the wordline current is small, requiring only to charge the control gates capacitively. As a result, for phase change memory, larger X-decoders are required to handle the current, requiring higher support circuit overhead and larger die area.

Scaling

Given the high level of R&D investment required to introduce a new memory technology, it is important that the technology can be scaled for multiple generations. One key scaling concern is proximity disturb. Analysis and experiments showed that it is not a problem. First, measured data showed that for current structures, programming of one cell multiple times has no impact on adjacent cells. The simulation data shows that the decrease in radial temperature,

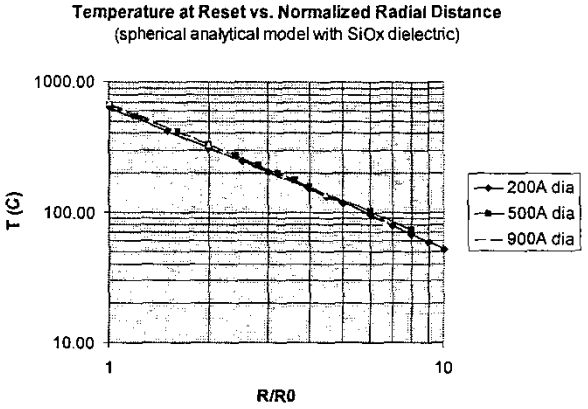

Figure10: Temperature as function of normalized radial distance for different size memory contact

when normalized to the dimension of the heating area, falls on a universal curve (Fig. 10). As long as the heating area is

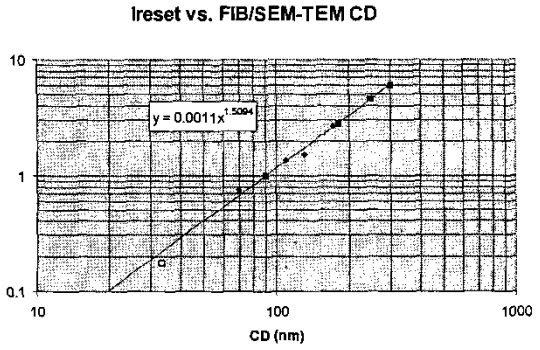

Figure 11: Ireset (in mA) as function of contact diameter

scaled with the cell area, the proximity effect will scale for different generations. Using the scaling of Ireset current with contact diameter (Fig. 11), the scaling of ovonics memory is evaluated. Table 1 shows one example of scaling under constant device voltage. The basic memory parameters scale directly with the smaller geometry. With an assumption of 10% vertical dimensional scaling of the diode parameters, the resistance of the memory cell goes up by over 50% per generation. While this increase reduces the signal level, it is judged that it is still well within the sense circuit capability of modern day memory technology design.

Conclusions

Phase change memory based on chalcogenide alloy has demonstrated the basic capability of high cycle, fast read and write, low voltage and moderate energy operation. It is also

Table 1: Phase change memory scaling based on assumption of constant voltage across memory and diode stack

		130 nm	90 nm	65 nm	40 nm	32 nm	22 nm	Scaling Percent	Comment
DRAM 1/2 Pitch	nm	130	90	65	45	32	22	-30%	Moore's Law
Electrode Contact Dimensio	nm	47	33	23	16	11	8	-30%	Sublitho Dimension Scales with Moore's Law
Ireset	μA	500	294	171	99	57	35	-41%	From actual data and extrapolated
Chal thickness	nm	60	50	40	30	30	30	-13%	Scale for AR, min 30nm for Spreading R
Rset Chal	KΩ	1.6	2.5	3.8	5.5	9.6	12.2	50%	Spreading resistance model
Rset Electrode Heater	KΩ	0.8	1.4	2.3	4.0	7.1	11.4	70%	1.4V heater voltage
Rset Total	KΩ	2.4	3.9	6.1	9.5	16.7	23.6	58%	Chal + Heater
Diode area	nm^2	18590	8910	4648	2228	1091	535	-51%	Cell diode area = 1.1 square features
Deep trench depth	nm	440	396	356	321	289	260	-10%	Process Assumption
Buried WL Depth	nm	390	351	316	284	256	230	-10%	Process Assumption
Shallow trench Depth	nm	200	180	162	146	131	118	-10%	Process Assumption
P+ Junction Depth	nm	120	108	97	87	79	71	-10%	Process Assumption
Vertical Diode Depth	nm	270	243	219	197	177	159	-10%	Buired WL-P+ junction
Wordline depth under trench	nm	190	171	154	139	125	112	-10%	Buried WL-Shallow trench
Diode J vertical	A/cm^2	2.69E+00	3.30E+00	3.68E+00	4.46E+00	5.19E+00	6.57E+00	20%	Increases with smaller diode area
Diode vertical IR drop	V	0.070	0.077	0.078	0.085	0.089	0.101	8%	Vertical scaling offsets current increase
Buired WL J lateral	A/cm^2	2.02E+04	1.91E+04	1.71E+04	1.59E+04	1.44E+04	1.42E+04	-7%	Decreases with I reset
Buried WL lateral IR drop	V	0.20	0.12	0.07	0.04	0.02	0.01	-41%	Decreases with smaller Cell
Dioide Forward Voltage Dro	V	1.37	1.30	1.25	1.22	1.21	1.21	-2%	Small change in Voltage drop

projected that the basic memory element can scaled to 22 nm node. The challenge is to demonstrate high volume manufacturability as well as reliability and this will be the focus of continuous development work.

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