11.8 Integrated Ultrasonic System for Measuring Body-Fat Composition

Hao-Yen Tang[1], Yipeng Lu[2], Stephanie Fung[2], David A. Horsley[2], Bernhard E. Boser[1]

[1]University of California, Berkeley, CA, [2]University of California, Davis, CA

An accurate, low-power, and highly integrated solution for accurate assessment of body fat is presented that addresses a growing consumer interest in economical and easy-to-use solutions for monitoring personal health and fitness. Unlike the prevalent present solution that estimates body fat percentage from an impedance measurement integrated in a weight scale and gives only a global index with accuracy compromised by a host of factors including skin moisture and metabolic activity, the reported approach uses ultrasound for an accurate measure of the actual thickness of the fat and muscle layers [1].

Figure 11.8.1 shows a block diagram the system comprising an ASIC and custom MEMS transducer. The latter consists of an array of AlN piezoelectric micromachined ultrasonic transducer (PMUT) array with 50µm diameter, 70µm spacing, 8MHz resonant frequency and Q=3 [2]. In the experiments reported here, the array is organized into 7 groups of 9×5 elements where each group is wired in parallel and actuated with 32V square-wave drive signals generated by the ASIC, which results in a 3nm peak membrane displacement. The total capacitance C_L of each group is 17.5pF and dominated by pad and wiring parasitics.

The ASIC has 7 identical channels each with 6b delay control with 5ns resolution for transmit beam-forming, high-voltage level shifters, and a receive/transmit switch that isolates the low-noise receiver from the high transmit voltage. Unlike previously published solutions [3] that rely on external high-voltage supplies, this design generates all the necessary voltage levels from a single 1.8V supply with on-chip 5V and 32V charge-pumps and is thus amenable to battery power or power from a smartphone.

Figure 11.8.2 shows the dynamic 32V level-shifter. The conventional solution exceeds the current capabilities of on-chip charge-pumps owing to the large crowbar current flowing during the switching transient. The dynamic shifter adds switches M_{sw+} and M_{sw-} to prevent a conducting path from the supply to ground. M_{sw+} is opened before the low-to-high transition of V_{i+} and closed after the output has settled. This effectively removes the pull-up M_{p+} from the output during the transition, thus enabling the use of a small NMOS pull-down M_{n+} with low input capacitance and permitting high-speed operation.

Switches M_{sw+} and M_{sw-} are high voltage transistors and thus require high-voltage controls themselves. This requirement is met with an auxiliary level-shifter. The primary and auxiliary shifters, Cells A and B in Fig. 11.8.2, are cross-coupled to generate all required control signal, as indicated in the timing diagram. The input to Cell B is delayed by t_d = 10ns with respect to the input control of Cell A. During reception, the transmitter is inactive. Charge leaking from V_{o-} could eventually turn on M_{p-}, resulting in crowbar current. Inactivity of more than 10ms turns on a bypass switch that ensures V_{o-} remains at HVV_{DD}. Since a small device can be used, the circuit has minimal impact on operating speed and power dissipation. An identical circuit is used for V_{o+}.

Figure 11.8.1 shows the connection of the level shifters to the output transistors. Leveraging the 5V intermediate output from the charge pump, a 5V voltage shifter is used for the output NMOS transistor to optimize the tradeoff between power dissipation, circuit area, and operating speed. The 5V boosted signal is also used in the 32V shifter for the PMOS, improving efficiency and circuit bandwidth compared to a design driven from a 1.8V input. The two gate drive signals are designed to be non-overlapped, preventing crowbar current.

Figure 11.8.3 shows the circuit diagram of the charge-pump. A two-stage design with a 5V intermediate voltage reduces the step-up ratio. Unlike a previous Dickson charge-pump published in [4] that relies on high-voltage fringe capacitors, this design employs a series-parallel architecture to stay within the breakdown limit of 5V MIM for their higher density and thus reduced bottom-plate capacitance. Two and seven cells are used, respectively, for the 5V and 32V pumps. Unlike [4], which employs a traditional ac-coupled switch-driving scheme, this implementation relies on the level-shifter described above to avoid the need for high-voltage capacitors and provide a rail-to-rail driving signal, resulting in smaller switches and improved efficiency.

The charge-pump requires non-overlapping control signals. Rather than generating all waveforms in the low-voltage domain with separate level-shifters, the outputs from the two cross-coupled level-shifters are combined in the high-voltage domain to generate all three required control signals. As indicated in the timing diagram, V_{clk_HV2} is the NAND of inputs V_{o+} and V_{o-}. A structure with individual controls for the NMOS and PMOS switches and delayed low-voltage inputs V_{2d} and V_{4d} are used rather than a static NAND to separate the rising/falling edge of pull-up and pull-down transistors to avoid crowbar current. The same approach is used for control signals V_{clk_HV} and $\overline{V_{clk2\ HV}}$.

The 32V pump is self-starting with a HV diode between input and output. For the 5V charge-pump, a startup circuit consisting of a static level-shifter and HV switch is used as it fails to start with the 1.8V supply reduced by a diode threshold drop. The charge-pumps use 250pF and 100pF series capacitors and operate at 2MHz and 60kHz, respectively, to deliver 91µA and 5µA, respectively, sufficient for performing a measurement every 5ms with 5 cycles of 8MHz rail-to-rail 32V pulses driving each transducer. Figure 11.8.4 shows the startup transient of the cascaded 5V and 32V charge pumps with 10nF bypass capacitors. The output reaches 90% of the final value after 37.6ms. With a 60kHz clock, the charge-pump achieves over 30% efficiency and delivers up to 160µW.

Figure 11.8.5 shows the results from evaluating the system with a phantom simulating human tissue [5]. The phantom consists of a 500µm-thick skin layer, a fat layer whose thickness is varied during measurements and a 5mm-thick skeletal muscle layer. A 2.5mm PDMS layer couples the transducer to the tissue phantom. To account for possible local-variation of tissue, a 2D rendering is first obtained by adjusting the transmitter delays to steer the beam over 17 discrete angles to find a coarse measurement of fat-muscle boundary. After the initial course measurement, beam-forming is used to focus the beam to maximize the signal strength. Since the fat-muscle boundary acts like a plane reflector, beam-forming at twice the boundary depth results ~3dB greater SNR compared to plane-wave transmission.

Figure 11.8.6 summarizes the system performance and shows the measured fat thickness versus phantom dimension with the beam focused at middle with 16mm depth. Each pulse-echo operation with all seven channels active takes 20µs and consumes 2.6µJ from the 1.8V supply. Thanks to the dynamic level-shifter, power loss within level-shifter is negligible and 89% of energy from the charge pump is delivered to drive the output transducers. The charge pump delivers 32.5% of the power from the 1.8V supply to the 32V charge pump output and hence dominates overall system efficiency. In this work, the transmitter is driven at 8MHz, although the level-shifter is capable of operation at up to 40MHz. 28ns latency is measured from input $pulse_{in}$ to output 17.5pF C_L.

Figure 11.8.7 shows the micrograph of the AlN transducer array and the ASIC fabricated in 0.18µm CMOS with 5V and 32V high-voltage transistors and 5V MIM capacitors. The chip area is 2.0mm² and includes the complete system except for the digital controller, ADCs, and two off-chip storage capacitors.

References:

[1] D. R. Wagner, "Ultrasound as a Tool to Assess Body Fat," *J. Obes.*, p. 280713, 2013.

[2] Y. Lu, H. Tang, S. Fung, B.E. Boser, and D.A. Horsley, "Short-Range and High-Resolution Ultrasound Imaging Using an 8 MHz Aluminum Nitride PMUT Array," *IEEE MEMS Conf.*, 2015.

[3] K. Chen, *et al.*,"Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE J. Solid-State Circuits,* pp. 2734-2745, Nov. 2013.

[4] Y. Ismail, H. Lee, S. Pamarti, and C.-K.K. Yang, "23.8 A 34V Charge Pump in 65nm Bulk CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 408-409, Feb. 2014.

[5] Syndaver Labs, Synthetic Human; Muscular Tissue Plate. http://syndaver.com/shop/syntissue/muscular-tissue-plate

 978-1-4799-6224-2/15/$31.00

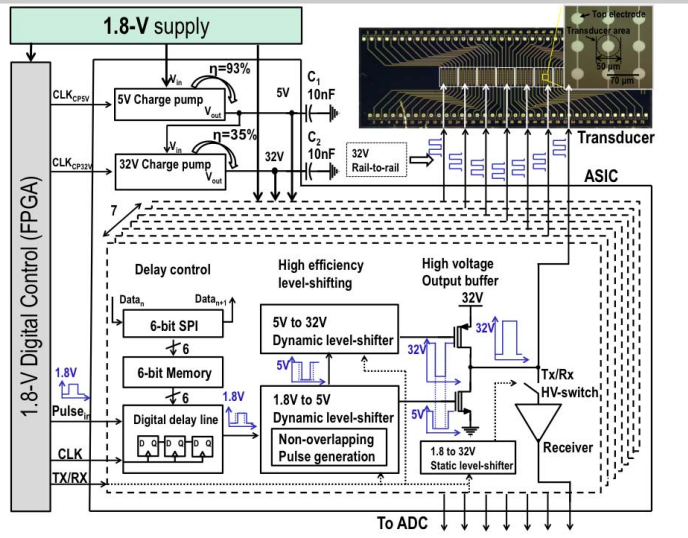


Figure 11.8.1: System diagram comprising the ASIC, ultrasonic transducer, and a controller realized with an FPGA.

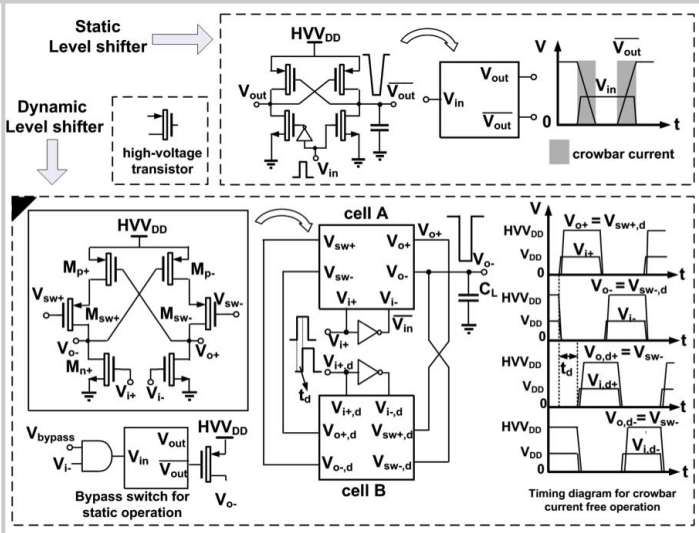
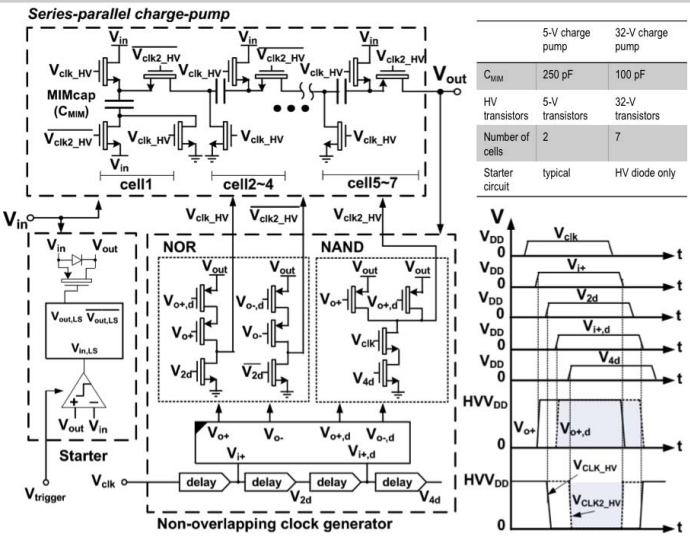


Figure 11.8.2: Conventional static and proposed dynamic 1.8V to 32V level-shifter design with crow-bar current suppression for low-power operation.



	5-V charge pump	32-V charge pump
C_{MIM}	250 pF	100 pF
HV transistors	5-V transistors	32-V transistors
Number of cells	2	7
Starter circuit	typical	HV diode only

Figure 11.8.3: Circuit diagram of the charge-pumps and clock generators. The same design is used for the 5V and 32V pumps.

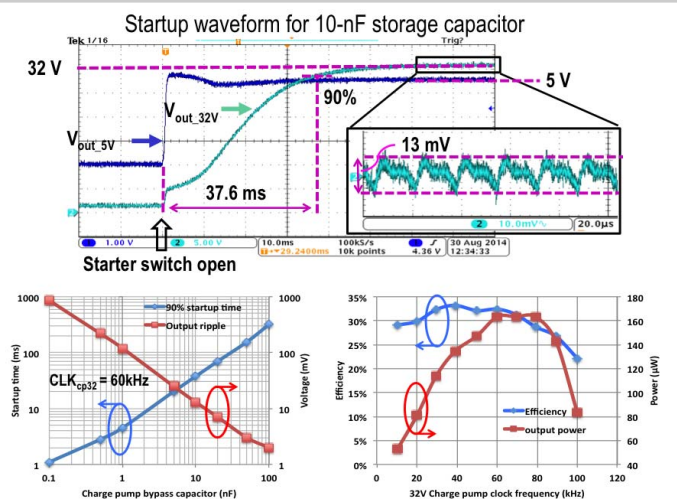


Figure 11.8.4: Measured charge-pump startup transient. The graphs show the tradeoff between ripple and startup time versus bypass capacitor size and efficiency and available power versus clock speed.

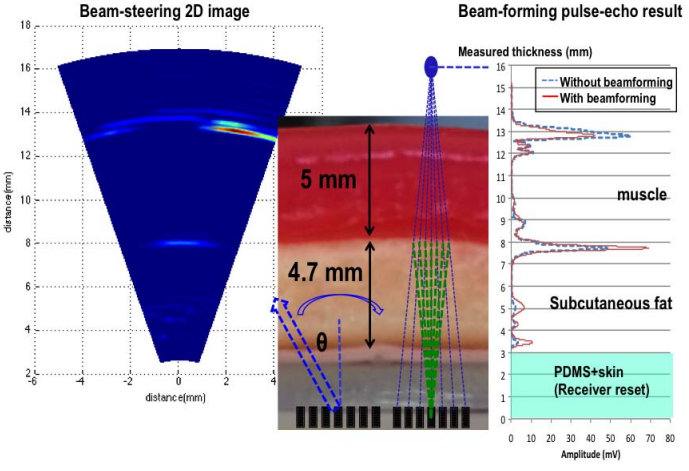


Figure 11.8.5: Received echo and 2D reconstructed image from a tissue phantom [5].

Output voltage	32 V
Supply voltage	1.8 V
Numbers of channel	7
Delay resolution	5 ns
Transducer load Per channel (C_L)	17.5 pF
Charge pump efficiency	32.5%
HV driver efficiency (From HVV_{DD} to C_L)	89%
Energy per measurement	2.6 µJ
Operating frequency	8MHz (nominal) 40MHz (maximum)* *with 8pF load
Channel latency	28 ns
Chip area (active)	2.0 mm²
Technology	TSMC 0.18um 32V

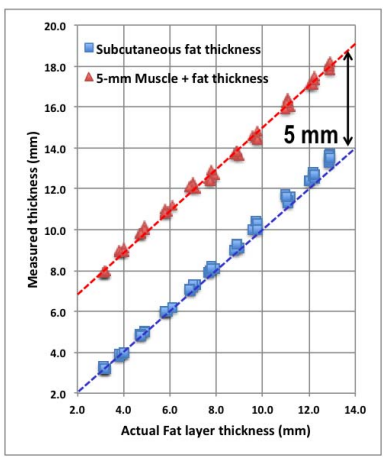


Figure 11.8.6: Performance summary and measured thickness of fat layer versus phantom

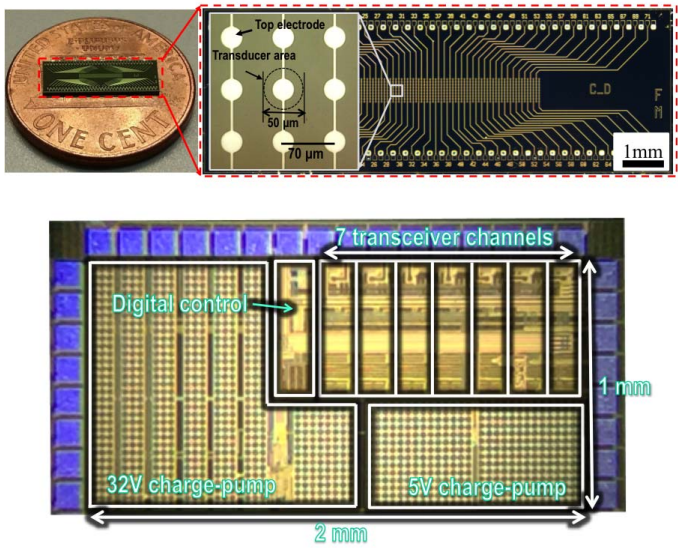


Figure 11.8.7: Die photo for AIN transducer array and ASIC.

978-1-4799-6224-2/15/$31.00