A 5.5mA 2.4-GHz Two-Point Modulation Zigbee Transmitter with Modulation Gain Calibration

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Abstract— **A 2.4-GHz two-point modulation IEEE 802.15.4 (Zigbee) compliant transmitter is presented. This sigma-delta fractional-N PLL based transmitter is optimized for both low-power and low-cost purposes. A novel closed-loop calibration scheme is proposed to minimize the gain mismatch between two modulation points, which is the main source of error in two-point modulation. Fabricated in a 0.15-µm CMOS process, the proposed transmitter achieves EVM less than 8% for 2-Mchips/s MSK modulated signal and consumes 5.5mA under a 1.55-V regulated power supply. The core area is 0.8×1.1mm^2.**

I. Introduction

With the ever-increasing demand for simple low-cost low-power short-range wireless connectivity in applications with low to moderate data rates, such as sensor network, industrial control and WPAN, the IEEE 802.15.4 [1] (Zigbee) protocol is established to provide a standard based solution. Zigbee specifies different channel spacing, data rate and modulation scheme for 868/915MHz and 2.4GHz ISM bands. The fully integrated transmitter (TX) described in this paper targets the 2.4-GHz applications only.

To relax the design requirements on PA, O-QPSK with half-sine pulse shaping (equivalent to MSK) is adopted as the modulation scheme for 2.4GHz Zigbee PHY [1]. Various approaches can be applied to generate MSK modulated signals in the transmitter. The traditional I/Q modulator [2-3] is more flexible and simpler in concept. However, it is not power and area efficient as it inevitably needs two RF up-converting mixers driven by a pair of baseband DACs+LPFs and qudrature LO buffers. Alternatively, due to the constant envelope of MSK modulation, it can also be implemented by direct modulating the VCO in open-loop [4] or closed-loop [5-6] PLL after MSK to FSK encoding [7]. Compared with I/Q modulator based TX, the mixer-less direct VCO modulated TXs are superior both in silicon area and power consumption as the modulated VCO can drive the PA directly and is free of VCO pulling issue. However, they have their own limitations. The open-loop approach suffers from the VCO frequency drift and unsuppressed VCO phase noise as the loop is broken during data transmission. In closed-loop architecture, the frequency drift is avoided and the modulation takes place at two points (as shown in Fig 1). Other than modulating the VCO through a DAC, the TX data also varies the feedback division ratio in the PLL by a sigma-delta modulator (ΣΔM). Unfortunately, inherent gain and phase (delay) mismatches always exists in between these two modulation points [8],

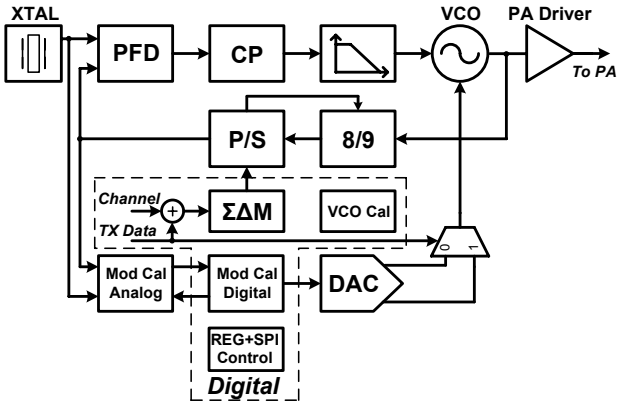

Fig.1 Proposed two-point modulation Zigbee transmitter

which may result in significant modulation distortion in terms of EVM loss, especially for the gain mismatch. In this paper, a novel mixed-signal closed-loop calibration method is developed to minimize the modulation gain mismatch so as to achieve satisfactory EVM result.

II. Two-Point Modulation Transmitter

A. Transmitter Architecture

Block diagram of the proposed two-point modulation Zigbee transmitter is depicted in Fig 1. The core building block is a ΣΔ fractional-N PLL which will also be configured as the LO synthesizer for receiver during RX mode (LO buffers not shown). After proper encoding, the Zigbee specified 2-Mchips/s MSK can be implemented as FSK with frequency deviation f_{dev}=±500kHz [7], relative to the channel frequency.

As shown in Fig 1, this FSK modulation is realized at two different points, by direct modulating the VCO and by controlling the divider ratio when the PLL is locked to the channel frequency. Modulation gain at the divider input can be accurately controlled by the ΣΔM, but band-limited by PLL bandwidth (around 100kHz in this work). On the other hand, as the loop is closed, the VCO modulation bears a highpass characteristic. Ideally, assuming that the modulation gain and phase of the lowpass and highpass paths are perfectly matched, the combined modulated VCO output is independent of loop bandwidth. However, considering that the capacitance of modulation varactor in the VCO can vary from chip to chip (up to 20-30%), gain mismatch between two modulation points always exists. As will be indicated in next section, this gain mismatch is the main source of EVM loss in practical

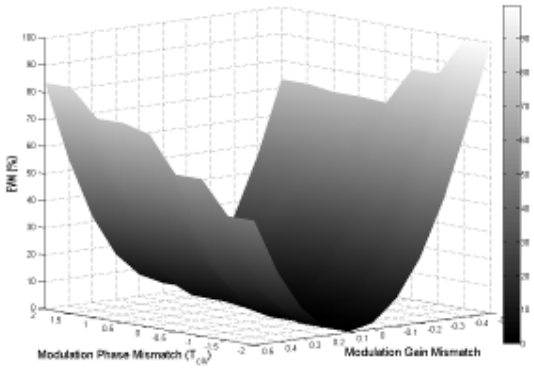

Fig. 2 Effects of modulation gain and phase mismatches on EVM

implementation. Therefore, efficient calibration is needed in order to match the highpass modulation gain to the lowpass one.

B. Effects of Modulaton Gain and Phase Mismatch

In reference [8], a theoretical model has been created to study the effects of gain and phase mismatch in two-point FSK modulation, but it only can be used to predict the error of frequency deviation in FSK, which is not directly related to the EVM degradation. Meanwhile, the delay is assumed to be a fraction of symbol duration (0.5μs for 2-Mchips/s MSK). However, in practical design, the delay/phase mismatch introduced by ΣΔM can be well compensated in digital domain. The remained mismatch caused by signal routing and other parasitic is in the order of only a few nano-seconds. Our study will show that such small delay mismatch has negligible effect on EVM performance.

In this work, a system-level model of the two-point modulation transmitter is developed in ADS. A Ptolemy simulation is performed to study the effects of modulation gain and phase mismatches on EVM performance. The gain mismatch is assumed to be up to ±50%, while the phase mismatch is up to ±2 reference clock (24MHz) cycles. The result is shown in Fig 2. Clearly, the EVM performance is quite sensitive to the gain mismatch, but insensitive to the small phase mismatch. To meet the specified <35% EVM in IEEE 802.15.4, the gain mismatch should be maintained within ±10% to leave enough design margin, considering that the circuit noise (phase noise, etc) is not included in the ADS model. According to the simulation, the EVM degradation due to a 20-ns phase mismatch is less than 1%, therefore the design requirement on the compensation circuit is greatly relaxed.

III. Modulatiln Gain Mismatch Calibraiton

A. Description of Calibration Circuit

The block diagram of the gain mismatch calibration circuit, together with the VCO, is shown in Fig 3. It consists of a modified PFD and an accurate charge pump to rectify and integrate the phase difference between reference clock and divider output, a pre-charged voltage reference, an 8-bit fully-differential DAC to provide the required modulation voltage

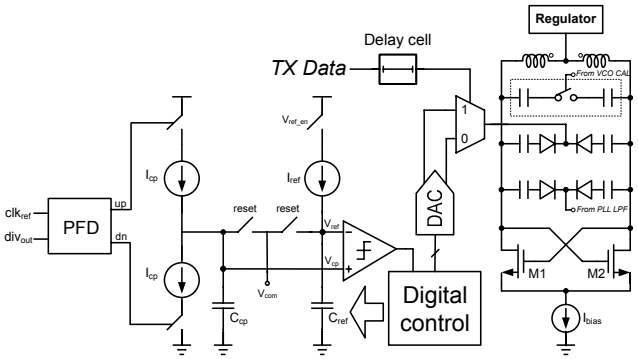

Fig. 3 TX Modulation gain calibration circuit

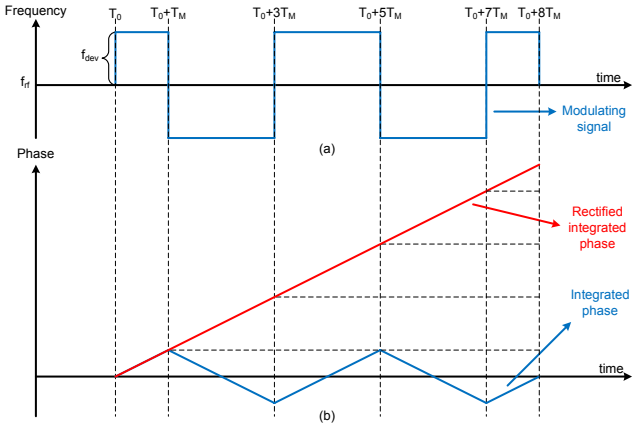

Fig. 4 Calibration theory

levels and a digital block to implement the calibration algorithm and provide the control signals. The calibration procedure can be summarized as follows.

Before the calibration starting, the PLL is programmed to an integer-N frequency which is closest to the channel frequency. After that, a set of pulses with pre-defined data rate and timing is used to modulate the VCO. The amplitude of the pulses is defined by the DAC. To understand the calibration mechanism intuitively, assuming that the data rate $1/T_M$ of the modulating pulses is much higher than the loop bandwidth, PLL does not intend to correct the frequency and phase change in the loop (we will justify this assumption in section III-B), and therefore the frequency-time characteristic at the VCO output can be illustrated as in Fig 4(a) during modulating. A modified PFD is then used to compare and rectify the phase difference between the divided VCO output and the reference clock, which is further integrated by the charge pump (shown in Fig 4(b)) and converted to a voltage level proportional to the modulation gain. A binary search SAR algorithm is applied to tune the modulation gain to the desired value.

B. Considerations on Non-Idealities

During the calibration, in the vicinities of $T_0 \pm nT_M$ (n is an even number), the phase difference can be too small to be detected accurately by PFD and charge pump, as shown in Fig 4(b). To relax the design requirements on PFD and charge

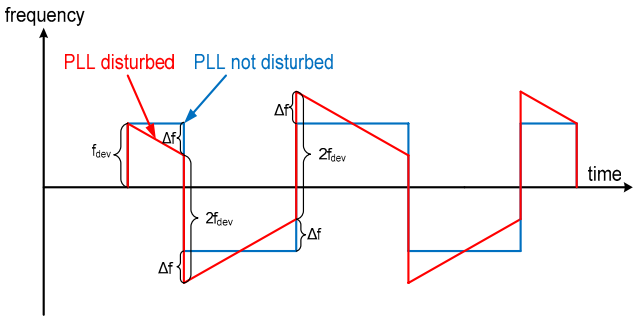

Fig. 5 Justification for undisturbed PLL during calibration

pump, the PFD is activated only when the phase difference is relatively large as in the vicinities of $T_0 \pm mT_M$, m is an odd number. Careful timing control must be conducted to realize such operation. Moreover, as illustrated in Fig 4(b), the initial phase difference is assumed to be zero. In practical design, this assumption is barely held due to the up- and down currents mismatch in the charge pump of PLL and the routing mismatch. Fortunately, the resulted phase offset can be tolerated to some extent as the offsets in positive and negative phase detection period cancel with each other. Careful design and layout are still required to maintain the offset within the tolerable level.

In section III-A, the PLL is assumed to be undisturbed during calibration. However, in closed-loop operation, the PLL always tries to correct the frequency and phase disturbance. The resultant VCO output during calibration is depicted in Fig 5 in which the waveform no longer has rectangle shape. The good news is that we are more interested in the integrated phase instead of instantaneous frequency. Even though the PLL is slightly disturbed, the integrated phase (area under the curve) remains almost unchanged as shown in Fig 5 with first-order varactor characteristic assumed. Another benefit is that larger charge pump current in PLL can be used to reduce the relative current mismatch.

IV. Some Building Blocks

A. VCO

The simplified schematic of the VCO is already given in Fig 3. Note that only NMOS cross-coupled pair is used for the negative-gm device to provide enough headroom across PVT due to the relatively high V_{th} of the PMOS. To maintain a reasonable K_{VCO} (around 60MHz/V in this work), 7-bit switched MIM capacitor array together with the control logic is used to realize the center frequency tuning. The size selection of the modulation varactor is a tradeoff between modulation sensitivity and PVT tolerance. The typical sensitivity is designed to about 5MHz/V.

B. 8-bit Low Power DAC

As shown in Fig 6, the 8-bit DAC is based on the current-steering approach and "6+2" segmentation architecture is adopted. The two LSBs are binary coded; while the remained 6 MSBs are thermometer (unary) coded employing row-column binary-to-thermometer decoding. Low power consumption is the main design requirement for this DAC during TX mode. To achieve low LSB current without biasing

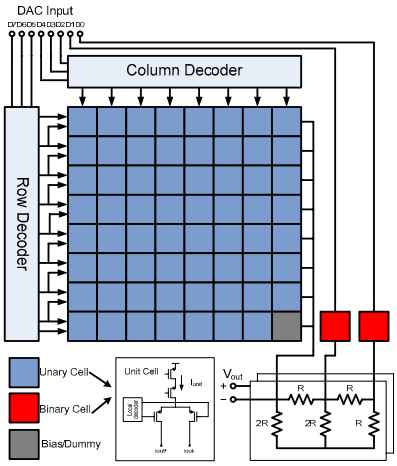

Fig. 6 8-bits low power DAC

the current source into subthreshold region, two R-2R ladders are used as the output loads, as well as the current splitter for binary cells. As a result, the unary and binary cells can employ the same transistor sizing and unit current (1uA), which simplifies the layout design. With the help of R-2R ladder, an effective LSB current of 0.25μA is achieved.

V. Experimental Results

The proposed two-point modulation 2.4-GHz Zigbee transmitter is fabricated in a 0.15-μm CMOS process and occupies $0.8 \times 1.1 mm^2$ core area. Fig. 7 shows the chip micrograph in which the main circuit blocks are identified. On-chip regulators are used to provide the required 1.55-V supply voltages, and to sustain the external supply input ranging from 1.7V to 3.7V.

During the TX mode, the PLL bandwidth is set to about 100kHz, as shown in the phase noise plot of Fig. 8 which is measured at 2.45GHz. The phase noise at 1-MHz offset is about -107.5dBc/Hz and the integrated phase noise over the range of 10kHz to 10MHz is about 2.66° rms. Fig 9 shows the transmitter output spectrum and signal constellation after modulation gain calibration. The side lobes of output spectrum at 2Mchips/s are well below the spectrum mask defined by IEEE 802.15.4 standard. The measured rms EVM is less than

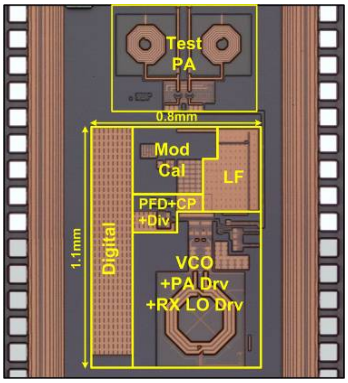

Fig. 7 Chip microphotograph

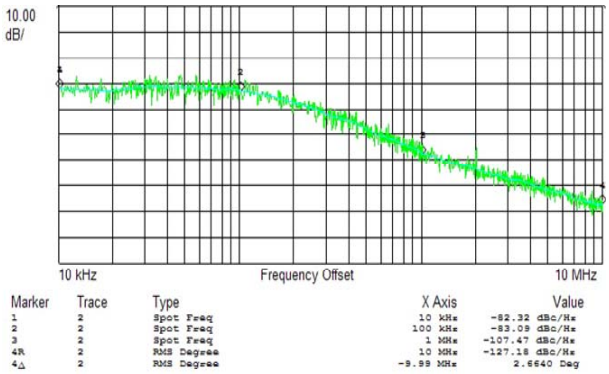

Fig.8 Measured PLL phase noise

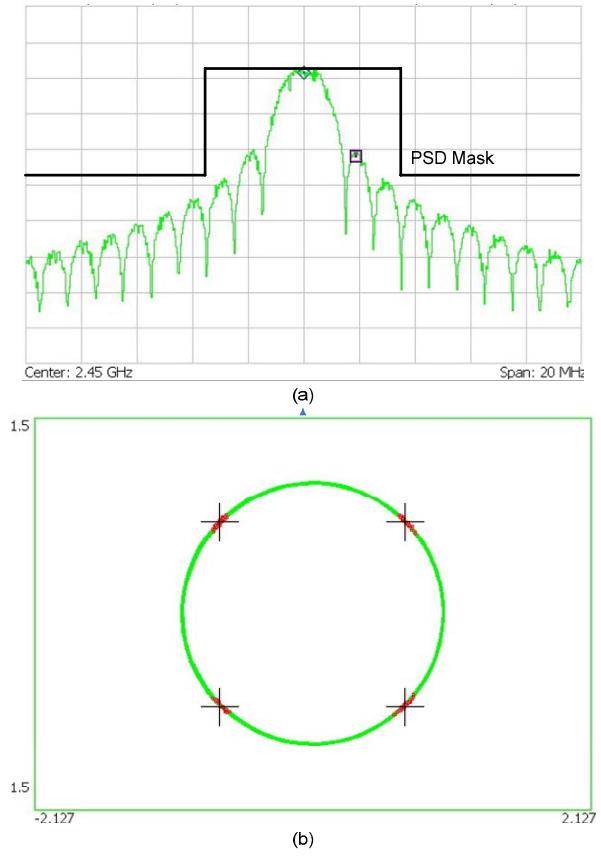

Fig. 9 Measured TX (a) output spectrum and (b) constellation

8% (minimum 5.8%) after calibration, which is far below the 35% rms EVM specified by IEEE 802.15.4. The designed transmitter consumes 5.5mA including the PA driver. The measured performance is summarized in Table1.

VI. Conclusion

This paper presents a fully-integrated 2.4-GHz Zigbee transmitter. Two-point modulation architecture is adopted due to its low-power and lost-cost potential. The EVM degradation caused by the modulation gain and phase mismatches between two modulating point are studied, indicating that the gain mismatch is more severe in practical implementation. A mixed-signal modulation gain mismatch calibration circuit is proposed to minimize its effects so as to achieve a good EVM performance. The 2.4-GHz Zigbee transmitter has been implemented in a 0.15-µm CMOS process and occupies $0.8\times1.1mm^2$ die area excluding the pad frame. This transmitter achieves rms EVM better than 8% at and consumes only 5.5mA including the PA driver.

Table 1 Performance summary

Process	0.15-µm CMOS	
Package	32-pin QFN	
Supply	1.55V	
Frequency Band	2.405GHz to 2.480GHz	
K_{VCO}	60MHz/V	
Modulation Sensitivity	5MHz/V	
Phase Noise	2..66 rms degree (10kHz-10MHz)	
EVM	<8% (5.8% minimum) @2Mchips/s	
Power Consumption	VCO core	1.6mA
	PA driver	0.9mA
	Other PLL blocks	2.2mA
	Modulation Cal	0.17mA
	Bias+Regulators	0.5mA
	Digital	0.12mA
	Total	5.5mA
Core Area	$0.8\times1.1mm^2$	

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