A 35-GHz Differential Distributed Loss-Compensation Amplifier

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Abstract-**The demand for 40+Gb/s broadband drivers and equalizers for electrical and optical links compels the use of distributed circuit techniques and on-chip loss compensation. A distributed loss-compensation scheme is presented for synthetic transmission lines. The distributed loss-compensated amplifier is implemented in a 120nm BiCMOS process using only NMOS devices. A 3dB bandwidth of 35GHz is measured with gain ripple of +/-1dB while consuming only 18mW.**

I. INTRODUCTION

Broadband silicon circuits enable high-speed electrical and optical chip-to-chip and chip-scale links for next-generation computer and network architectures. To generate the large signal swings necessary to drive optical modulators, distributed amplifiers have been suggested as broadband line drivers because of the intrinsic ability to trade-off delay for bandwidth. While delay does not substantially degrade high-speed link performance, bandwidth directly affects link capacity. Recent work has focused on silicon implementations of amplifiers for 40Gb/s optical communication [1][2] or ultrawideband (UWB) wireless communication [3][4]. In particular, UWB LNAs have been demonstrated to provide low noise figure over wide bandwidth[4]. Distributed structures also play a role for signal conditioning and are the basis for microwave-speed integrated equalizers [5][6].

Amplifiers have been demonstrated with bandwidth greater than 100GHz using III-V circuit technologies [7] and similar performance will soon be demanded in silicon CMOS. As a result, silicon circuit designers have grappled with ultra-broadband distributed design. Distributed loss mechanisms in silicon and silicon-germanium processes limit operation above 40Gb/s. Therefore, loss compensation circuits are necessary to accommodate the quality factors of on-chip passives and achieve higher circuit gain-bandwidth product. Recently, circuit techniques have been proposed to compensate for distributed circuit losses by tailoring the frequency response of the transconductance [2]. Other approaches include filter design using m- and k- derived filters [1] and inductive peaking in a cascode gain stage [3].

This paper describes a distributed loss compensation scheme for silicon broadband circuits and suggests a new distributed loss compensation amplifier for microwave broadband circuits. In Section II, distributed circuit limitations are reviewed and recent work on loss compensation is discussed in Section III. The implemented circuit technique is presented in Section IV. Section V presents S-parameter and time domain measurements of the frequency-dependent loss compensation scheme.

II. DISTRIBUTED DESIGN LIMITATIONS

Distributed structures absorb device parasitics into a synthetic transmission line and achieve a broadband response. A general synthetic transmission line is illustrated in Fig. 1, where each transconductance device is represented by its input capacitance, C. The impedance and bandwidth of the synthetic transmission line is characterized by Z_0 and the Bragg (periodic) cutoff frequency, ω_c.

$$Z_o = \sqrt{L/C} \qquad \omega_c = 2/\sqrt{LC} \qquad (1)$$

where L and C is the inductance and capacitance per section. Distributed amplifiers are constructed from two synthetic transmission lines that absorb the device parasitics into a gate and drain transmission line. The transconductance, g_m, of each device contributes to the overall gain. The voltage gain is additive for distributed structures because traveling waves combine constructively. The voltage gain of a distributed amplifier is

$$A_v = -N g_m \sqrt{Z_{\pi,g} Z_{\pi,d}}/2, \qquad (2)$$

where N is the number of sections and $Z_{\pi,g}$ and $Z_{\pi,d}$ represent the impedance of the pi-sections of the gate and drain transmission lines [9]. Notably, one-half of the voltage gain contributes to the generation of a backward traveling wave which must be absorbed into a termination and is lost. Assuming $Z_{\pi,g} = Z_{\pi,d} = Z_o$, the gain-bandwidth product, GBW, of the distributed amplifier is found by combining expressions from (1) and (2).

$$GBW = \frac{N}{2\pi}\frac{g_m}{C} \leq N \cdot f_T \qquad (3)$$

The analysis indicates that the gain-bandwidth product can be arbitrarily increased by adding additional stages. However, the synthetic transmission line introduces loss. In Fig. 1, the series dc resistance in the inductor as well as skin and dielectic losses
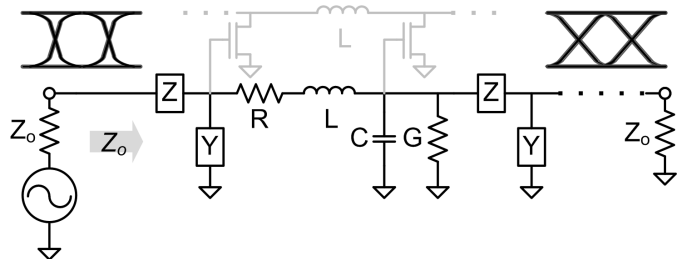

Fig. 1. Illustration of the effect of distributed losses in transmission lines.

of the transmission line at high-frequencies limit the unbounded gain-bandwidth of the distributed circuit. Also, drain-source conductance causes loss in the drain line and series gate resistance degrades the transfer characteristic of the gate transmission line. Consequently, a reasonable *GBW* limitation is $N \cdot f_{max}$ [7]. For each section of the line, the loss is

$$A_l = e^{-\alpha l} \qquad \text{where } \alpha = R / 2Z_o. \tag{4}$$

For skin and dielectric losses, the attenuation, α, is a function of frequency. Distributed losses reduce the voltage gain of consecutive stages and, hence, adding more sections diminishes the gain. Therefore, the optimum number of sections is

$$N_{opt} = \frac{\log(\alpha_g) - \log(\alpha_d)}{l(\alpha_g - \alpha_d)}, \tag{5}$$

where α_g and α_d are the gate and drain line attenuation [8]. In practice, the number of stages is typically limited to between six and eight. Clearly, the GBW product for a distributed amplifier is finite. If it were possible to reduce either the attenuation of the gate or drain line, the optimum number of stages is unbounded. High-performance 40Gb/s+ silicon distributed circuits might benefit from loss compensation to achieve the higher gain-bandwidth performance for a given technology.

III. LOSS COMPENSATION SCHEMES

To maximize performance, circuit designers have presented several compensation schemes. A simple approach uses the increase in the impedance near the Bragg cut-off frequency. The pi-section impedance is

$$Z_\pi = Z_o / \sqrt{1 - (\omega / \omega_c)^2}, \tag{6}$$

where Z_o is the low-frequency impedance in (1). Consequently, the gain increases near the Bragg frequency. This provides loss compensation when the Bragg frequency is related to the onset of frequency-dependent losses. For higher bandwidth circuits approaching 100GHz, the impedance increase occurs at frequencies significantly higher then the onset of skin and dielectric losses.

Therefore, active approaches might employed for loss compensation. Differential lines loaded with cross-coupled NMOS
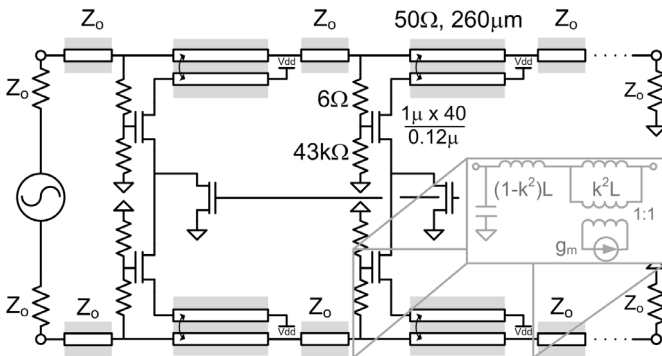
Fig. 2.   Schematic of differential distributed loss-compensation amplifier.
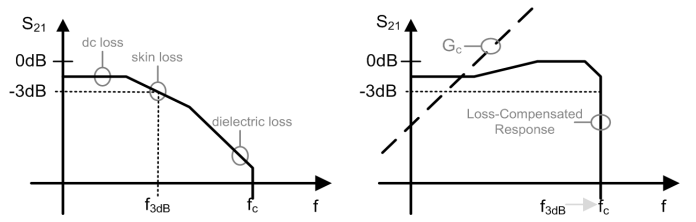
Fig. 3.   Loss mechanisms of distributed transmission lines and compensated response with common source coupled transmission line stage.

devices can compensate loss through a distributed negative resistance. Additionally, distributed amplifiers might use capacitive source degeneration to provide a frequency dependent response in the transconductance of the distributed device [2].

IV. PROPOSED COMPENSATION SCHEME

This work proposes a compensation scheme based on a coupled transmission line transformer. The schematic for the differential circuit topology is illustrated in Fig. 2 and consists of a common source device and coupled transmission line between the common source device and the bilateral transmission line. The common source NMOS transistor generates a current that is coupled at high-frequencies into the synthetic transmission line.

The operation of the suggested loss compensation scheme is illustrated in Fig. 3. While the loss along the transmission line reduces the 3dB bandwidth and, hence, voltage gain at high-frequencies, the feedforward amplifier can provide a compensating high-frequency gain, A_c. The combination of the synthetic transmission line losses and the amplifier gain push the inherent transmission line 3dB bandwidth towards the Bragg frequency. This broadband response makes it possible to cascade larger numbers of distributed stages limited only by the dc resistance of the line.

The small signal model of a single cell is inset in Fig. 2. The distributed compensation gain can be estimated to be

$$A_c = (1 + sk^2 Lg_m) / (1 + sL / Z_o). \tag{7}$$

The distributed line inductance introduces a pole with the line impedance while the transconductance provides a left-half plane zero. The product of the coupling coefficient and the transconductance determines the location of the zero. The coupling into the transmission line is, however, not unilateral and the feedback will impact the actual response. The gain of the compensation scheme must be greater than one at the onset of the frequency roll-off of the synthetic transmission line to improve the 3dB bandwidth. Consequently, this unity gain frequency trades the transmission line inductance, the strength of the feedforward coupling between the transmission lines and the transconductance.

The circuit is fabricated in the 120nm IBM BiCMOS 8HP process. The chip microphotograph for a 10-stage differential loss-compensation circuit is shown in Fig. 4. The chip mea-
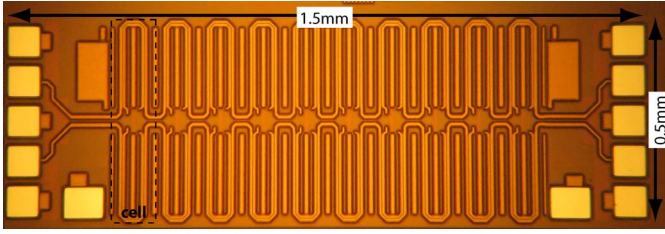
Fig. 4.   Chip microphotograph for 10-section differential loss-compensation circuit implemented in a 120nm BiCMOS process.

sures 1.5mm x 0.5mm by implementing dense transmission line packing. The active devices are located at the point where the serpentine transmission lines connect.

V. MEASUREMENT OF DISTRIBUTED LOSS COMPENSATION

Two port S-parameters are measured at different drain voltages with an Agilent E8361B network analyzer to show the distributed line amplification in Fig. 5. S_{21} reflects the forward voltage transfer function. When $V_{dd} = 0V$, the line loss causes a significant broadband frequency roll-off and the 3dB bandwidth of the amplifier is around 8GHz. As the drain voltage is increased, the midband frequency response remains basically unchanged while at high-frequencies the feedforward amplifier compensates the distributed losses. Therefore, the 3dB bandwidth increases dramatically and becomes limited by gain ripple and peaking at high-frequencies. The maximum broadband gain with ripple +/-1dB occurs for $V_{dd} = 0.6V$ and provides a bandwidth of around 35GHz. At this drain voltage, the drain current is $I_d = 30.2mA$ for the differential line and the total power consumption of the differential circuit is 18.1mW. This implies that each differential section of the transmission line consumes 1.8mW.

The return loss is plotted in Fig. 6. S_{11} remains under -10dB for small drain voltages up to 35GHz. For $V_{dd} > 0.4V$, the return loss increases but remains below 0dB at all frequencies and avoids instability in the distributed transmission line.
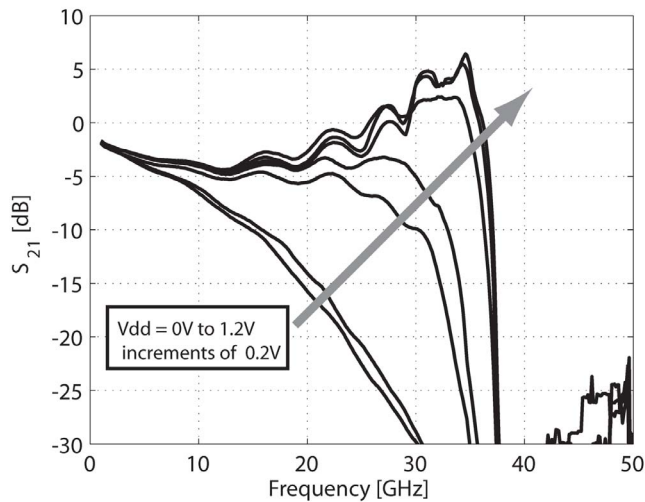

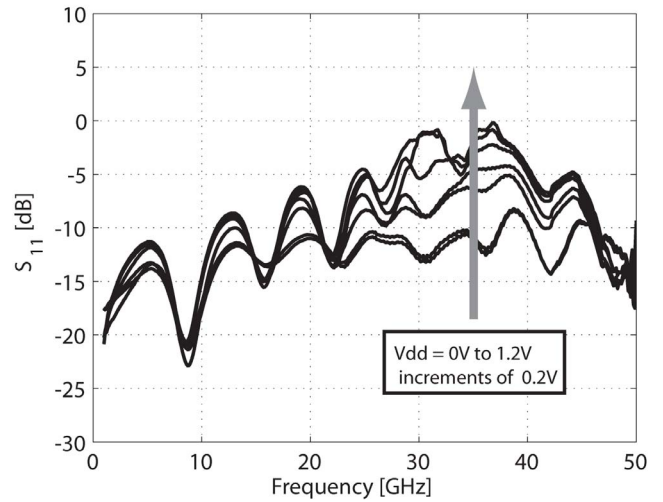Fig. 5. S_{21} measurement of line for a range of V_{dd} values with $V_g = 0.75$.

Fig. 6. S_{11} measurement of line for a range of V_{dd} values with $V_g = 0.75$.

Notably, the return loss approaches 0dB under conditions for which the forward gain of the distributed line is greater than 5dB. Maintaining low return loss and high forward gain is a problem of isolating the feedback path.

The Agilent N4903 bit-error rate tester (BERT) generates a 10Gb/s 2^{15}-1 PRBS sequence. A differential 1V swing is introduced to the line and the single-ended signal is recorded in Fig. 7 at two different drain voltages. The first condition shuts off the drain, $V_{dd} = 0V$, and the output signal is recorded using the Agilent 81600C communications analyzer with a 86117A 70GHz sampling head. The data eye is open but demonstrates the impact of skin-loss in the long rise time of the signal
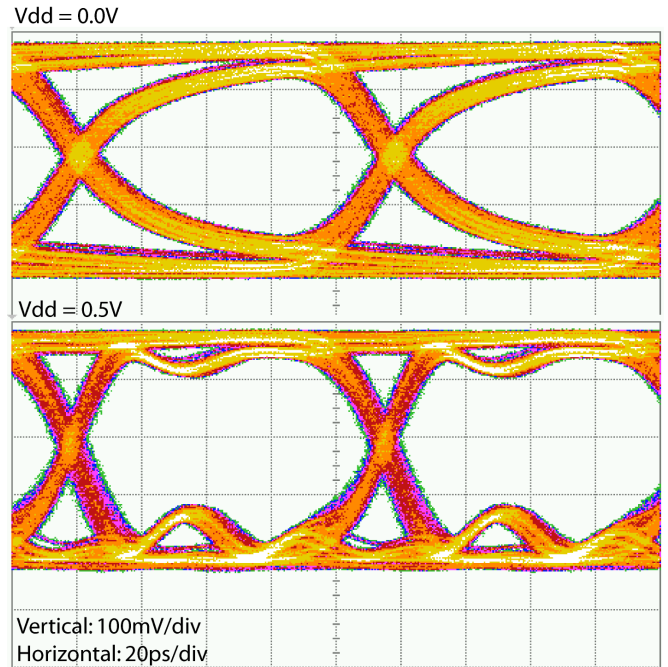

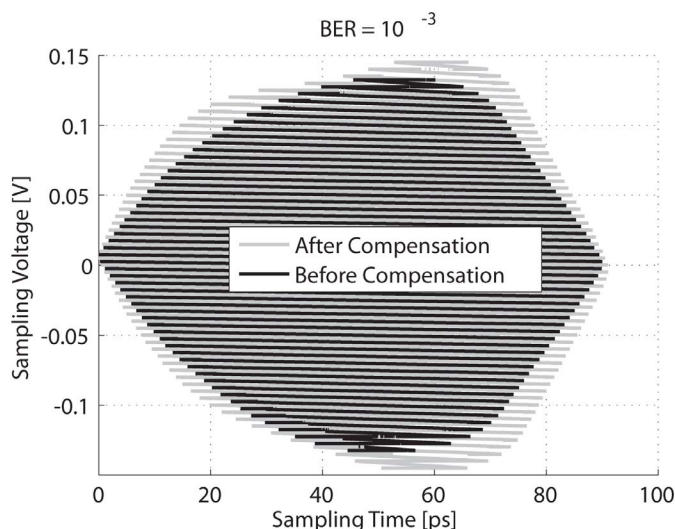Fig. 7.   10Gb/s data eye before (top) and after (bottom) line compensation.

Fig. 8.   Measured BER for NRZ data before and after loss compensation.

between the 80% and 90% voltage levels [10]. For data rates exceeding 20Gb/s, eye closure would be pronounced. The second data eye shown in Fig. 7 is recorded for $V_{dd} = 0.5V$. Here, the rise and fall times of the signal are greatly improved and the eye opening has increased. The S-parameters and measured signal integrity at 10Gb/s indicate that a data rate of 40Gb/s could be supported using the presented loss-compensation scheme.

The BER bathtub is recorded in Fig. 8. Before compensation the eye height is 245mV and the eye width is 85.3ps. After compensation, the eye height increases to 275mV and the eye width increases to 87.5ps, an increase of 12% in the voltage domain and 2.2% in the timing domain. More notably, the rise and fall time (measured at 10%-90% levels) decreases dramatically from 66ps to 24ps. The improved rise and fall times are
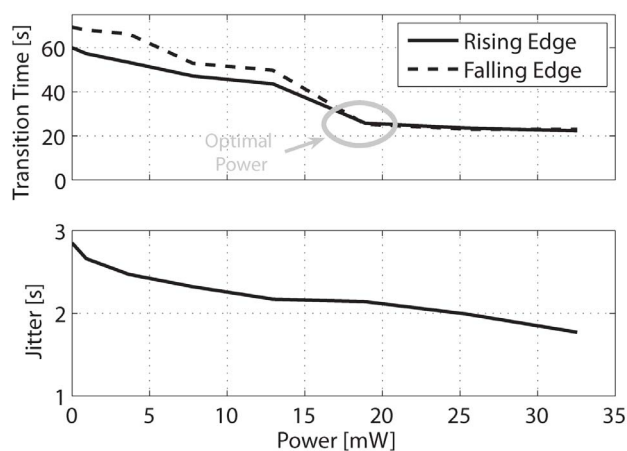

Fig. 9.   Rise/fall time measurements and rms jitter as a function of power consumption.

plotted in Fig. 9 as a function of the power consumption to find the optimum operation point. The rms jitter of the data eye is also recorded. The drop in the rms jitter is attributable to the decrease in the deterministic jitter [11].

VI. CONCLUSION

A distributed loss compensation amplifier is presented that improves the bandwidth of distributed structures through the introduction of feedforward compensation gain. The implemented circuit consists of ten amplifier stages and demonstrates broadband response of 35GHz with gain ripple of under +/-1dB. This new approach for distributed loss compensation can augment the performance of conventional distributed amplifier and equalizer topologies to improve the inherent gain-bandwidth limitations in synthetic transmission lines.

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