Towards Understanding the Origin of Threshold Voltage Instability of AlGaN/GaN MIS-HEMTs

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Abstract

GaN-power HEMTs with insulated gate structure suffer from threshold voltage drifts (ΔV_{th}) under forward gate bias stress. We present a systematical approach to characterize the phenomenon and understand the dominant physical mechanisms causing this effect. We found out that ΔV_{th} is caused by traps with a broad distribution of trapping and emission time constants. This distribution is analyzed using so called Capture Emission Time (CET) maps known from the study of bias temperature instability (BTI) in CMOS devices. Physical models, which could explain the broad distribution of time constants, are discussed.

Introduction

High efficient GaN-based high electron mobility transistors (HEMTs) for power applications require an insulated gate structure in order to suppress parasitic gate leakage currents. In such MIS-HEMTs, in contrast to Schottky devices, a drift of the threshold voltage under forward gate bias is an often observed but rarely investigated phenomenon and usually related to trapping at the dielectric/III-N interface [1]. Previous investigations of this interface based on photoassisted CV-measurements [2], admittance measurements [3] or DTLS-like measurements [4] are mainly focusing on determining the interface trap density. We present a detailed physical analysis of the trapping and detrapping phenomena at the dielectric/III-N interface responsible for threshold voltage instabilities of GaN MIS-HEMTs. The investigation of threshold voltage transients over five decades of time and analysis of its bias and temperature dependency suggests a broad distribution of trap time constants with similar tendencies as known from the bias temperature instability (BTI) phenomena on silicon MOS devices [5,6]. Our results reveal the dominant mechanism responsible for threshold voltage drift offering a tool for a systematical improvement of the gate bias overdrive stability.

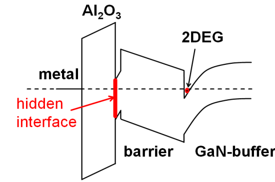

Fig 1. Band diagram showing the spatial separation of channel electrons from the "hidden" interface between gate oxide and GaN cap on top of the AlGaN barrier.

Devices & Experiments

Devices were fabricated on 4 inch GaN-on-SiC substrates with a gate length of 2 µm and a gate width of 200 µm. The barrier layer of the HEMT structure consisted of a 3 nm GaN cap and a 25 nm $Al_{0.25}Ga_{0.75}N$ layer (Fig. 1). The gate dielectric was provided using a 20 nm ALD-deposited aluminum oxide with an additional annealing step at 650°C. All characterizations have been carried out on an automated Keithley SCS 4200 system using consecutive stress and recovery sequences (Fig. 2a). Monitoring of the device threshold voltage drift ΔV_{th} is done at a single bias point ($V_{g,meas}$, $V_{d,meas}$) in the linear region of the transfer characteristic, where the drain current degradation and the threshold voltage shift can be correlated. This enables to measure also fast transient responses of ΔV_{th} (Fig. 2b). The threshold voltage drift is monitored during both, stress and recovery sequences. There is a delay of about 20ms between the end of the stress pulse and the first measured value of ΔV_{th}. During this delay there is already a recovery, which cannot be measured. Forward bias stress is applied to the gate contact, while drain and source are grounded. In

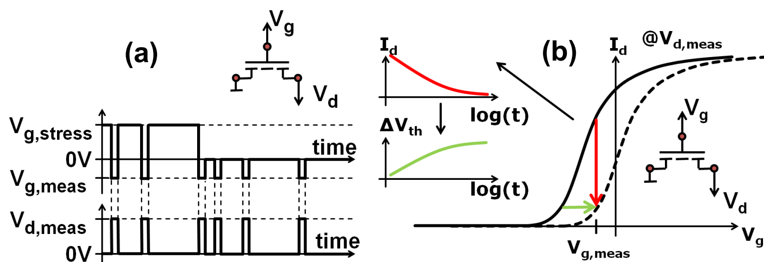

Fig 2 (a) Measurement scheme of a single stress-recovery sequence used to monitor ΔV_{th}. (b) Correlation between drain current degradation and ΔV_{th}. The bias point ($V_{g,meas}$,$V_{d,meas}$ = 5 V) is in the linear region of the transfer characteristic.

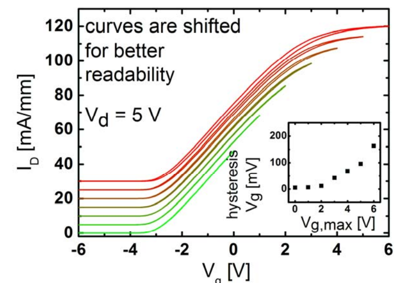

Fig 3. Consecutive transfer characteristics with increasing maximum gate bias $V_{g,max}$. The observed hysteresis starts at around 2 V and increases with $V_{g,max}$ (inset).

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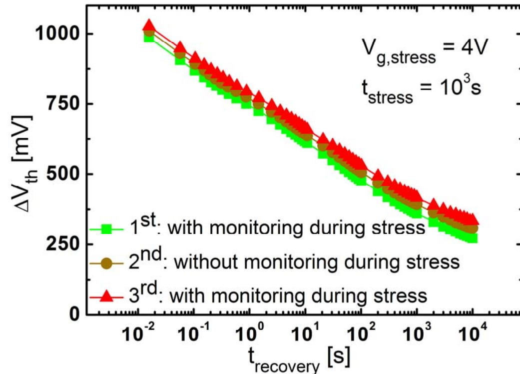


Fig 4 Recovery traces of ΔV_{th} from three consecutive stress-recovery sequences (stress not shown), where the first and the third stress sequence have been interrupted by monitoring measurements but not the second. The parallel shift of the consecutive traces is caused by traps with an emission time larger than the recovery time of 10^4s. The reproducibility of the results further indicates no creation of additional traps during the measurement.

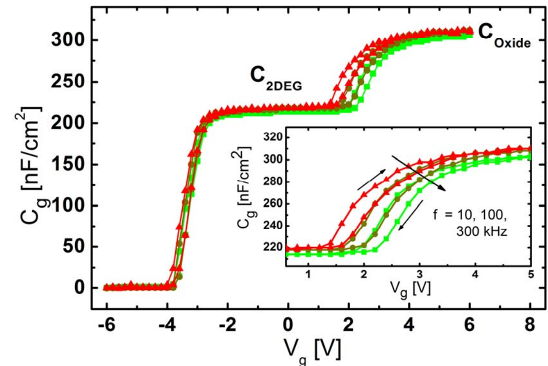
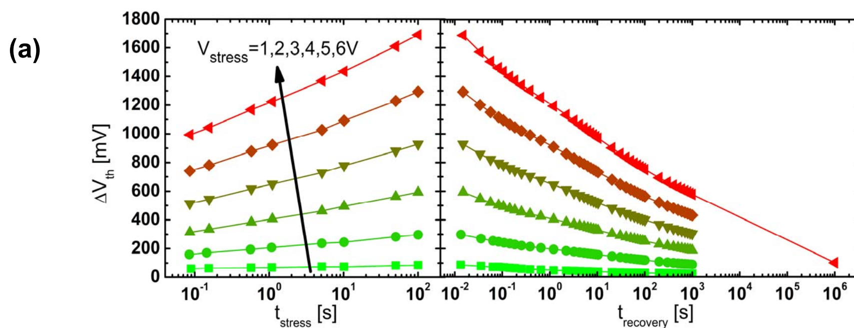


Fig 5. CV analysis: The increase of the capacitance at forward bias > 2 V suggests charge accumulation at the dielectric/III-N interface. The second capacitance plateau is consistent with the gate oxide capacitance. The hysteresis between forward and backwards sweeps for CV curves at different frequencies indicates trapping of charges with different time constants.

this case the intrinsic 2DEG acts as a counter electrode to the gate contact and a nearly homogenous electrical field distribution over the barrier is achieved. During recovery all contacts are grounded. In contrast to silicon MOS structures the V_{th} shift is not accompanied by a degradation of the transconductance (Fig. 3), because of remote trapping at the dielectric/III-N interface spatially away from the active channel (2DEG) which is therefore referred as "hidden" interface (Fig. 1). Thus the drain current degradation directly correlates with ΔV_{th} following the trend of the transfer characteristic. Comparing repeated stress-recovery sequences with and without monitoring at room temperature suggests that monitoring during stress has no significant influence and also no new traps are created during consecutive stressing sequences (Fig. 4). Further, dummy measurements without any stress between the monitoring measurements show an overall V_{th} drift stability of about 15 mV up to 10^5 s.

Experimental Results

In consistency with other authors [7], measurements of the transfer characteristic on our devices (Fig. 3) show no clear hysteresis up to 2 V maximum gate bias. The capacitance-voltage (CV) measurements exhibit a hysteresis around the second plateau, which is a hint on charge trapping (Fig. 5). Measurements of the threshold voltage drift over stress-recovery sequences show a quasi-linear characteristic on a logarithmic time scale, indicating a broad distribution of time constants for stress and recovery. Also a clear dependency on the gate bias is observed (Fig. 6). Due to this characteristic an extraction of time constants using conventional multiexponential fitting analysis is ambiguous (Fig. 7). A method to analyze such a broad distribution of characteristic time constants has been developed by Reisinger et al. [5] using so called capture emission time (CET) maps, which are extracted out of the recovery traces like that shown in Fig. 8a. The difference between two recovery traces of different stress times equals the threshold



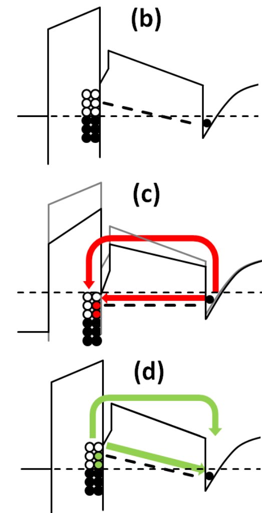


Fig 6 (a) Stress-recovery sequences over different gate bias show a quasi-linear behavior on a semi-logarithmic scale indicating uniformly distributed time constants. The slope of the stress/recovery curves increases/decreases with increasing gate voltage indicating a large amount of traps involved. Nearly full recovery is observed after a recovery time of 10^6 s. The conduction band together with the occupation of oxide traps is shown (b) under thermal equilibrium, where all electrons below the Fermi level are filled, (c) during stress, and (d) during recovery. Additionally a leakage path (potentially formed by a dislocation band) through the barrier is shown (dashed line). Open and filled circles indicate empty and filled traps, respectively.

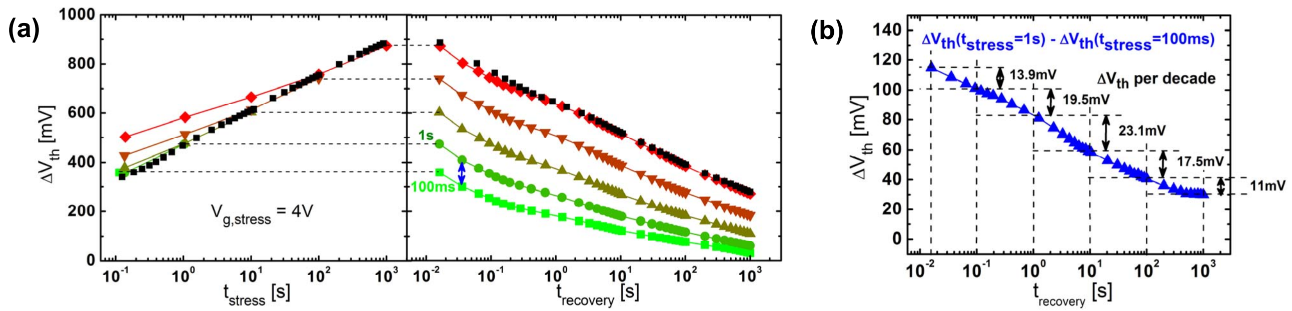


Fig 8 (a) Stress-recovery sequences with logarithmically increased stress times starting from 10^{-1} s to 10^{3} s at a fixed gate bias $V_{g,stress}$ = 4 V. The decreased trapping slope and the increased drift offset of the later stress sequences (colored curves) can be explained by traps with larger emission time constants than the recovery duration of 10^{3} s. Due to logarithmically increased stress time the recovery sequences follow the same trend as a single stress-recovery sequence (black dots). The recovery traces appear rather parallel in contrast to figure 6 indicating similar densities of traps with same emission time constants. (b) Difference between the recovery traces for stress times of 100ms and 1s.

voltage drift caused by traps with characteristic capture time constants within the corresponding stress decade. From the recovery trace of such a stress decade the portion of ΔV_{th} for each recovery decade is extracted, which is caused by traps with characteristic emission times within each recovery decade (Fig. 8b). The ΔV_{th} value can easily be translated into an interface trap density using the oxide capacitance. The procedure is repeated for every neighboring pair of logarithmically distributed recovery curves of Fig. 8a to extract the whole CET map (Fig. 9). Such CET maps typically show a broad distribution of emission time constants for each decade of capture time constants (equivalent to the rows in the CET map). It means that a certain stress pulse fills up a huge number of traps with logarithmically distributed emission time constants, which are magnitudes larger than the stress time. Further, the stress curves in Fig. 8a justify the use of logarithmically distributed stress times, because all stress curves follow the same trend after one decade of additional stress and thus pre-stress effects can be excluded for the recovery curves. Analyzing devices during stress sequences with additional pre-stress at relatively higher gate bias reveals parallel capture and emission to and from traps located at different energetic and/or local positions (Fig. 10). The result suggests parallel emission and capture of independent traps being activated under different gate bias conditions. Further it indicates again that the gate bias determines the overall number of accessible traps. Analysis of the temperature activation reveals a small increase of the V_{th} shift per decade during stress and recovery with increased temperature (Fig. 11). However, the real influence of the temperature could be shaded by the experiment, because of parallel acceleration of stress and recovery dynamics [5,6]. There seems to be a strong correlation between trap density and oxide quality as indicated by the comparison of the threshold voltage drift dependency on the gate bias stress

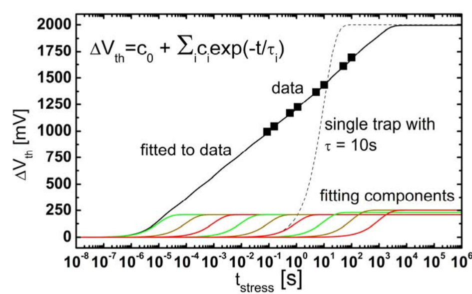


Fig 7 The stress curve at $V_{g,stress}$ = 6V from Fig. 6 is fitted to the sum of an arbitrary number of logarithmically equally distributed exponential functions. The obtained amplitudes c_i are nearly the same proving that the experimentally observed semilogarithmic charging is only explainable through a very large and logarithmically uniform distribution of time constants. Hence the measurement does not allow extracting individual trap densities or time constants.

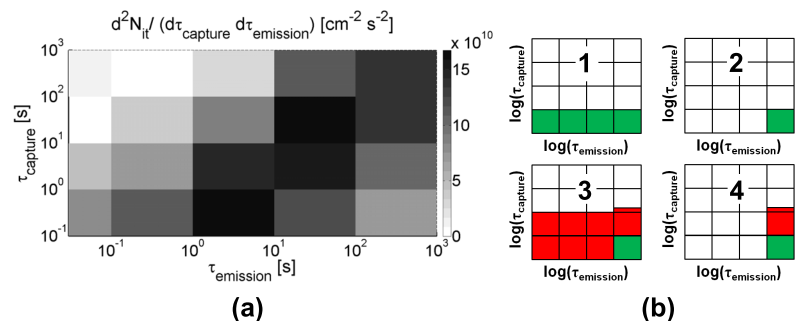


Fig 9 (a) CET map extracted out of the measurement from Fig. 8. The formula used to calculate N_{it} is given in the inset of Fig. 12. The result points out the strong correlation between capture and emission time constants with a relatively slower emission from traps. (b) Demonstration of the filling of the CET map: In the first stress recovery sequence all traps with a capture time constant smaller than the stress time are filled (1). After a certain recovery time all traps with a larger recovery time constant stay filled, all others are emptied (2). The remaining filled traps explain the initial stress offset visible in Fig. 8. A second stress recovery cycle with a ten times longer stress time (3) fills up the next decade in the CET map leading to an relatively increased filling level for emission time constants longer than the recovery time. (4) depicts the situation after another stress-recovery sequence.

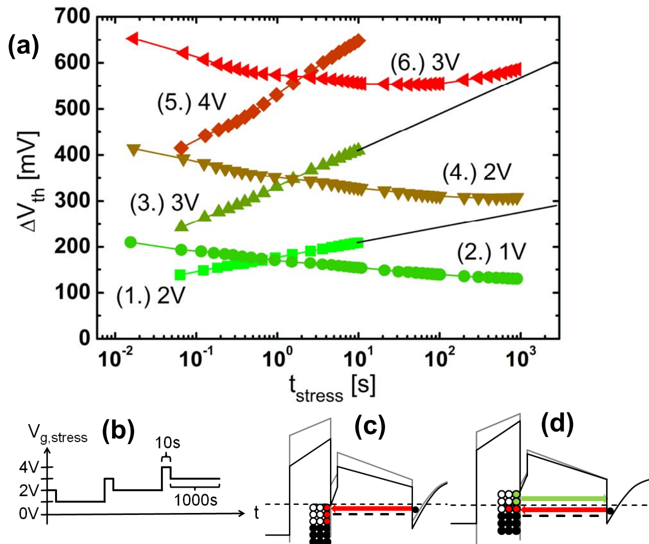


Fig 10 (a) Consecutive stress-stress sequences, where the first stress lasts for 10 s at a higher forward gate bias before the second stress with 1000 s duration, compare with (b). The 1000s stresses initially shows a recovery, followed by a quasi-saturation which starts to increase again continuing the stress characteristic from the prior 10 s stress at the same bias (dashed lines). In (c), capture of electrons during the 10s stress is shown. (d) sketches a parallel emission and capture process after stress shown in (c).

for annealed (densified) and not annealed gate oxides (Fig. 12).

Discussion & Conclusion

Although the microscopic nature of the defect states at the "hidden" interface cannot be clearly determined from our measurement, the behavior shows a strong similarity to bias temperature instability (BTI) in Si devices. Similar to BTI we found a broad distribution of time constants, which are represented by the CET map (Fig. 9). The CET map can be used to calculate device behavior under different stress/recovery conditions offering a tool for lifetime predictions [5,6]. However, the almost linear behavior of ΔV_{th} over V_g (Fig. 12) stands in contrast to silicon BTI results typically following a power law with an exponential coefficient of about three [5]. In addition, we present hypotheses which can explain the broad distribution of time constants: (1) a distribution of capture cross sections due to the disordered nature of oxide states at or near the "hidden" interface, (2) a distribution of tunneling distances between the interface and border traps [8,9], (3) spatially distributed leakage paths (dislocations bands) in the GaN/AlGaN barrier structure with varying magnitude of leakage current [10], which connect the 2DEG channel and traps at/near the "hidden" interface, (4) additional lateral trapping at the dielectric/III-N interface plane due to carrier hopping and thus a transport mechanism between the interface/border states. Mechanisms (2)-(4) can act as a common rate limiting process, which could explain the observed correlation between capture and emission processes (Fig. 9). In addition to the trap related behavior of our findings, we have to consider that even in an ideal dielectric bilayer charge is accumulated at the interface in order to maintain a constant steady-state current density. This is due to the different conductivities of each layer and is known as Maxwell-Wagner instability [11]. In summary, our characterization approach, using the concept of CET maps, has demonstrated its suitability for the investigation of the threshold voltage instability of gate insulated GaN HEMTs and provides a useful tool for their development.

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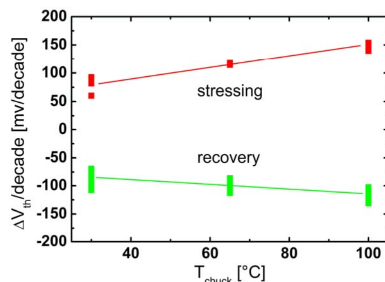

Fig 11 Slopes of stressing and recovery curves at increased temperatures showing weak temperature activation. The gate bias during stress was 3 V. The connecting lines are only a guide for the eyes.

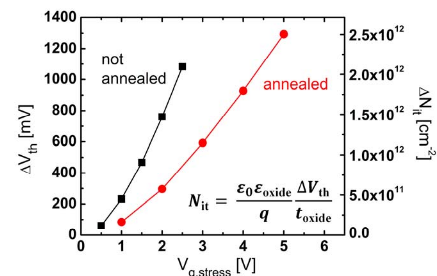

Fig 12 The threshold voltage drift over gate bias measured after 100s of stress shows a nearly linear relation. The two curves reflect a comparison between the standard process (i.e. annealed) and another wafer without the additional annealing step at 650°C after the ALD deposition.