A Four-Level Modular Multilevel Converter with Self Voltage Balancing and Extremely Small DC Capacitor

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***Abstract*—The modular feature of modular multilevel converter (MMC) makes it stand out for medium/high voltage applications. However, as the number of sub-modules increases, the control complexity of voltage balance of each sub-module sharply increases. Conventionally, the MMC sub-module voltage cannot be balanced without voltage monitoring and control. This paper mathematically proofs that four-level MMC has the merit of self voltage balancing by nature. This merit eliminates the voltage monitoring and control for MMC. The four-level MMC simulations are provided for verification purpose. In addition, since the sub-module capacitor voltage tends to converge to nominal value, the low frequency voltage ripple is greatly reduced, which allows the sub-module capacitance to be extremely small. The proposed four-level MMC is 1/8th -1/6th the capacitance compared to conventional MMCs.**

***Keywords*—Modular Multilevel Converter (MMC); voltage balancing; submodule capacitor**

I. INTRODUCTION

Modular multilevel converter (MMC) was proposed in [1] in 2003. MMCs have two inherent properties:

1) bulky dc capacitor is needed to absorb the fundamental-frequency ripple power in each sub-module;
2) feedback control and numerous voltage sensors are needed to coordinate the dc capacitor voltage of each sub-module.

These two properties result in poor power density for MMC and computational inefficiency for control algorithms, especially as the number of sub-modules increases in high-voltage/-power applications.

Many existing literatures have attempted to resolve the capacitor voltage balancing problem [2]-[18]. They can be classified into the following categories,

1) Each sub-module has a fast dc voltage controller to prevent the individual voltage from deviation. A slower upper controller balances the over-all arm voltages [2]-[3];
2) The sub-modules are sorted continuously in order of capacitor voltage value by the controller. The controller determines which sub-module(s) to be inserted, or by-passed, at each switching cycle [4]-[15];
3) The switching patterns are swap among the sub-modules in an arm within a fundamental cycle to guarantee the sub-modules with an equalized exposure to the loading conditions [16]-[18].

Among the three categories, 1) and 2) require sub-module voltage measuring and sophisticated closed-loop control on capacitor voltage; whereas 3) has the potential for sensorless voltage balancing. However, none of the literatures mathematically proves that MMCs do not need voltage balancing control.

Four-level MMCs are mathematically proved that they have the self voltage balancing merit in this paper. Two case studies are given for verification purpose. The low-frequency voltage ripples on dc capacitors can be greatly reduced. Since the capacitor voltages tend to converge to its nominal value, the low-frequency ripple on dc capacitors is greatly reduced. Therefore, smaller capacitors can be utilized in MMC sub-modules.

II. THREE-LEVEL MMC CAPACITOR VOLTAGE BALANCING

Fig.1 shows a three-level MMC with all possible sub-module patterns. For a three-level MMC, there are two, and only two, out of four sub-modules at inserting mode at a time. The other two sub-modules are at by-pass mode meanwhile. If the voltage drop on arm inductors could be neglected, the sum of the voltages of the two inserting-mode sub-modules are clamped to the dc source voltage. The capacitor voltage of Fig.1(a)-(f) could be formulated as,

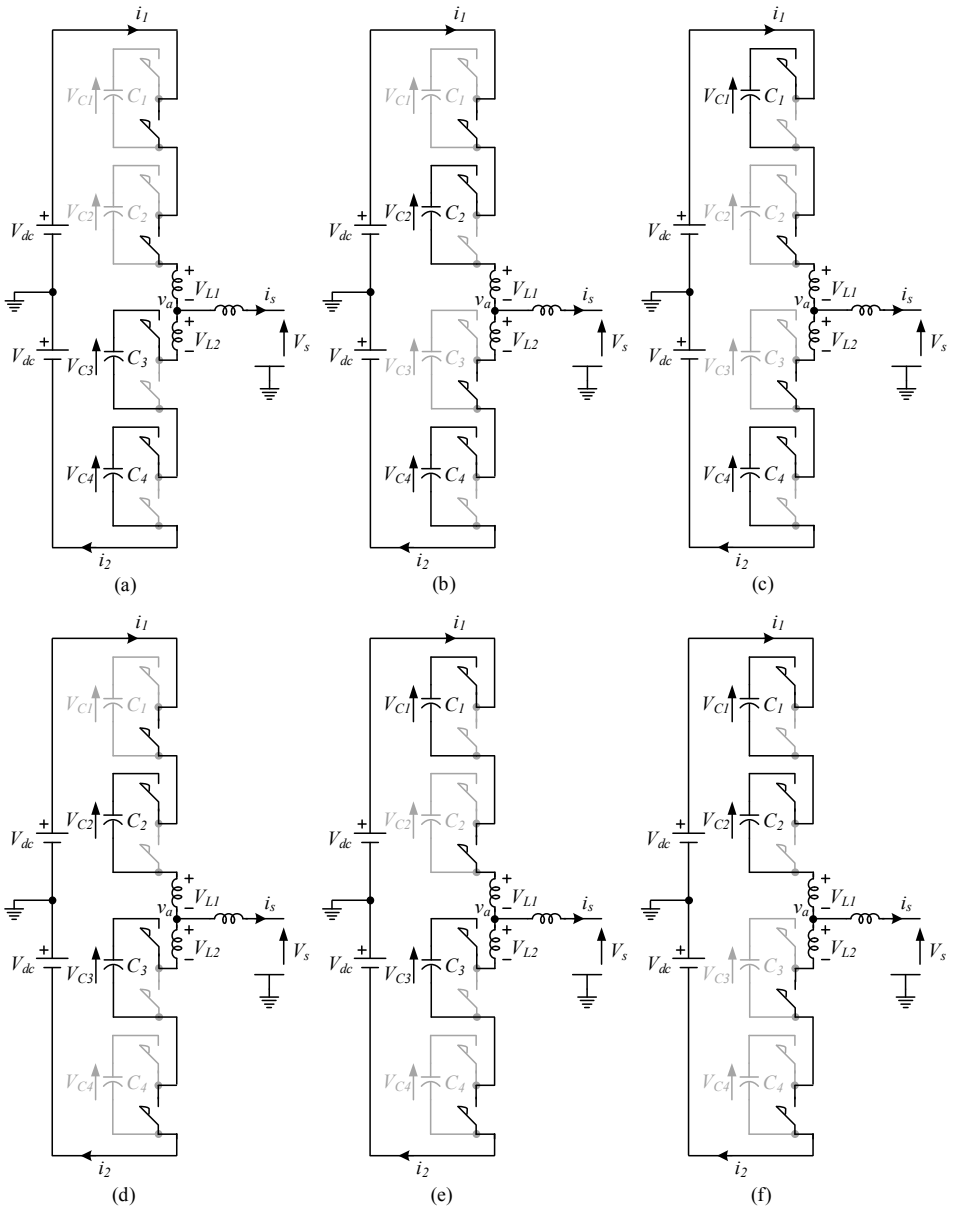

Fig.1. Three-level MMC with pole voltage of (a) V_{dc} (Level 1); (b)(c)(d)(e) zero volt (Level 2); and (f) $-V_{dc}$ (Level 3).

$$\begin{cases} 2V_{dc} = V_{C3} + V_{C4} \\ 2V_{dc} = V_{C2} + V_{C4} \\ 2V_{dc} = V_{C1} + V_{C4} \\ 2V_{dc} = V_{C2} + V_{C3} \\ 2V_{dc} = V_{C1} + V_{C3} \\ 2V_{dc} = V_{C1} + V_{C2} \end{cases}. \tag{1}$$

Re-write (1) into matrix form,

$$\begin{bmatrix} 2V_{dc} \\ 2V_{dc} \\ 2V_{dc} \\ 2V_{dc} \\ 2V_{dc} \\ 2V_{dc} \end{bmatrix} = \left[\begin{array}{cccc} 0 & 0 & 1 & 1 \\ \hline 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 \\ \hline 1 & 1 & 0 & 0 \end{array}\right] \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_1 \\ \hline \mathbf{Y}_2 \\ \hline \mathbf{Y}_3 \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix}, \tag{2}$$

$\mathbf{Y_1}$ contains the sub-module pattern when pole voltage v_a is at Level 1. $\mathbf{Y_2}$ contains all the possible sub-module patterns when pole voltage v_a is at Level 2. $\mathbf{Y_3}$ contains the sub-module pattern when pole voltage v_a is at Level 3. When MMC visits one of sub-module patterns, one equation of equation set (1) is

satisfied at a time. We can regard visiting a sub-module pattern as solving an equation of (1).

Now we need to check how many equations of (1) we need to guarantee a unique solution for all capacitors' voltages. Due to THD considerations, MMC pole voltage jumps between two adjacent levels at a time. Therefore, checking the rank of two adjacent levels complies with practical sense.

The ranks of $[\mathbf{Y_1}\ \mathbf{Y_2}]^T$ and $[\mathbf{Y_2}\ \mathbf{Y_3}]^T$ are all 4, which guarantees that $[\mathbf{Y_1}\ \mathbf{Y_2}]^T$ and $[\mathbf{Y_2}\ \mathbf{Y_3}]^T$ have four linearly independent rows each. Hence, we could find no more than one set of solutions for all capacitors' voltages if combining any two adjacent levels. There is one intuitive set of solutions for (1),

$$\begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} = \begin{bmatrix} V_{dc} \\ V_{dc} \\ V_{dc} \\ V_{dc} \end{bmatrix}. \tag{3}$$

Since (1) has no more than one solution, Eq.(3) must be the unique solution. Therefore, the three-level MMC has its capacitors' voltages balanced by nature.

III. Four-Level MMC Capacitor Voltage Balancing

For a four-level MMC, there are three, and only three, out of six sub-modules at inserting mode at a time. The other three sub-modules are at by-pass mode meanwhile. If the voltage drop on arm inductors could be neglected, the sum of the voltages of the three inserting-mode sub-modules are clamped to the dc source voltage. The capacitor voltage could be formulated as,

$$\begin{bmatrix} 3V_{dc} \\ \vdots \\ 3V_{dc} \end{bmatrix}_{20\times1} = \mathbf{Y}^{(4)} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{C6} \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_1^{(4)} \\ \mathbf{Y}_2^{(4)} \\ \mathbf{Y}_3^{(4)} \\ \mathbf{Y}_4^{(4)} \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{C6} \end{bmatrix} = \left[\begin{array}{cccccc} 0&0&0&1&1&1 \\ \hline 0&0&1&0&1&1 \\ 0&1&0&0&1&1 \\ 0&0&1&1&0&1 \\ 0&1&0&1&0&1 \\ 1&0&0&1&0&1 \\ 0&1&0&1&1&0 \\ 1&0&0&0&1&1 \\ 1&0&0&1&1&0 \\ \hline 0&0&1&1&1&0 \\ 1&0&1&0&1&0 \\ 1&1&0&0&1&0 \\ 1&0&1&1&0&0 \\ 1&1&0&1&0&0 \\ 1&0&1&0&0&1 \\ 0&1&1&0&1&0 \\ 0&1&1&0&0&1 \\ 0&1&1&1&0&0 \\ 1&1&0&0&0&1 \\ \hline 1&1&1&0&0&0 \end{array}\right] \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{C6} \end{bmatrix}. \tag{4}$$

$\mathbf{Y}^{(4)}$ contains all the possible sub-module patterns. When MMC visits one of sub-module patterns, one equation of equation set (4) is satisfied at a time. We can regard visiting a sub-module pattern as solving an equation of (4).

Now we need to check how many equations of (4) we need to guarantee a unique solution for capacitors' voltages. Due to THD considerations, MMC pole voltage jumps between two adjacent levels at a time. Therefore, checking the rank of two adjacent levels complies with practical sense.

The ranks of any two adjacent levels are all 6, which guarantee that (4) have six linearly independent rows. Hence, we could find no more than one set of solutions for all capacitors' voltages if combining any two adjacent levels. There is one intuitive set of solutions for (4), which is

$$\begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{C6} \end{bmatrix} = \begin{bmatrix} V_{dc} \\ V_{dc} \\ \vdots \\ V_{dc} \end{bmatrix}. \tag{5}$$

Since (4) have no more than one solution, Eq.(5) must be the unique solution. Hence, the four-level MMC has its capacitors' voltages balanced by nature.

IV. Y-Matrix Modultaion for Four-Level MMC

The pole voltage v_a of a four-level MMC can either be $1.5V_{dc}$, $0.5V_{dc}$, $-0.5V_{dc}$, or $-1.5V_{dc}$ if all capacitor voltages are V_{dc}. Assume the expected ac-side voltage to be v^*_s. The pole voltage v_a follows the level-shifted modulation strategy. The relationship of v^*_s and v_a is plotted in Fig.2.

The four-level Y-matrix modulation (YMM) can be explained with the aid of Fig.3. When the pole voltage v_a is determined to be at second level by level-shifted modulation, the level pointer is pointed to Level 2. The gating signal generator is going to grab the current row of $\mathbf{Y}_2^{(4)}$ that the Y-matrix pointer in level two is pointing to. After feeding the Y-matrix command to gating signal generator, the level two pointer will point to the next row and wait for the next call from level pointer. A MATLAB/Simulink simulation is conducted to demonstrate the YMM based three-level MMC.

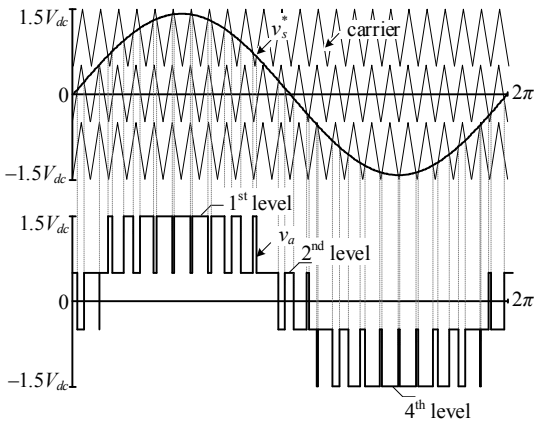

Fig.2. Relationship of ac-side voltage v^*_s and pole voltage v_a.

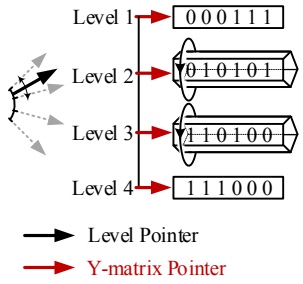

Fig.3. Y-matrix modulation strategy for four-level MMC.

V. CASE STUDIES

A. YMM Based Four-Level MMC

The simulation topology is shown in Fig.4. The key parameters of the four-level MMC are summarized in Table I. This four-level MMC simulation uses all sub-module patterns of four-level MMC. This guarantees a full rank of any two adjacent levels.

The load voltage and current are shown in Fig.5. The mid-point voltage is shown in Fig.6. The mid-point voltage of four-level MMC has seven levels. Although the mid-point voltage of any single phase, v_a v_b or v_c, is four levels, the differential voltage of any two phases, v_{ab} v_{bc} or v_{ca}, has seven levels. The

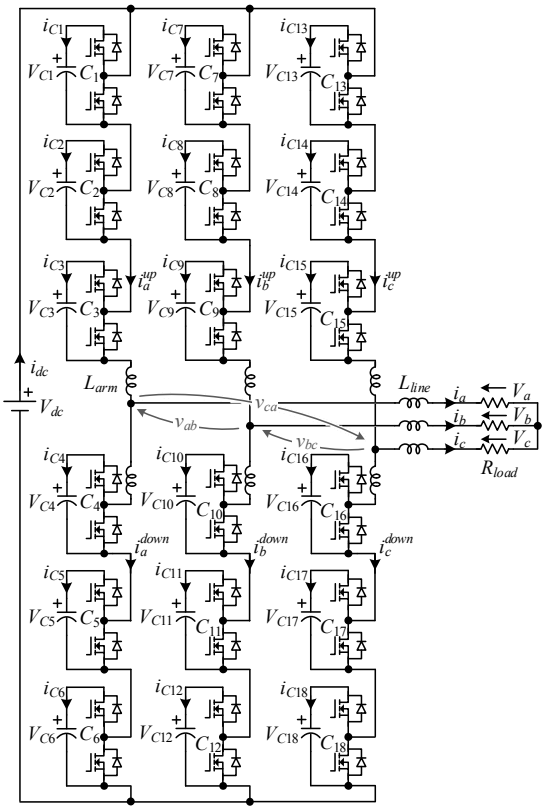

Fig.4. Four-level MMC simulation topology

TABLE I. FOUR-LEVEL MMC SIMULATION KEY PARAMETERS

Apparent Power, S	150 kVA
Fundamental Frequency, f_0	60 Hz
Switching Frequency, f_{sw}	30 kHz
DC-Bus Voltage, V_{dc}	3000 V
Phase Voltage, V_a, V_b, V_c	964 V
Line Current, I_a, I_b, I_c	52 A
Load Resistance, R_{load}	18.6 Ω (100% p.u.)
Line Inductance, L_{line}	1 mH
Arm Inductance, L_{arm}	0.1 μH
Sub-Module Capacitance, C_i	171 μF (1.2 p.u.)
Number of Sub-Modules per Arm	3

where i = 1, 2, …, 18.

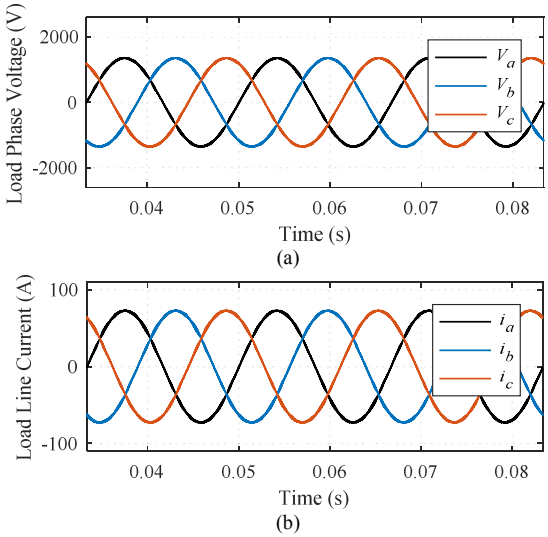

Fig.5. Four-level MMC (a) load voltage and (b) load current.

sub-module capacitor C_3 and C_4 voltages are shown in Fig.7. Fig.8 shows all capacitor voltages in phase-A. All capacitor voltages are well balanced and converging to nominal value (1000 V).

The capacitor voltage ripple is within 5%. The capacitor current consists mainly of fundamental component and switching-frequency harmonics. Note that the sub-module capacitance is only 1.2 p.u.. The total capacitor energy in respect to MMC power rating is 10.26 kJ/MVA in this simulation. Typically, to have a voltage ripple within 5%, the MMC needs to have sub-module capacitors energy to be 60 – 80 kJ/MVA[19]. Normally, the capacitor energy storage capability is proportional to the capacitor size. The proposed four-level MMC has only 1/8th -1/6th the capacitor volume compared to conventional MMC.

B. YMM Based Four-Level MMC with Non-Full Rank **Y**

In this case study, a non-full rank **Y** is selected for the four-level MMC. The capacitor voltages are expected to be unbalanced according to analysis. Together with Section V-A, the necessity of full-rank **Y** is emphasized. All the MMC parameters are the same as Section V-A, which are summarized in Table I. The **Y** in this case study are as follows,

$$\mathbf{Y}_1^{(4)} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}, \quad (6)$$

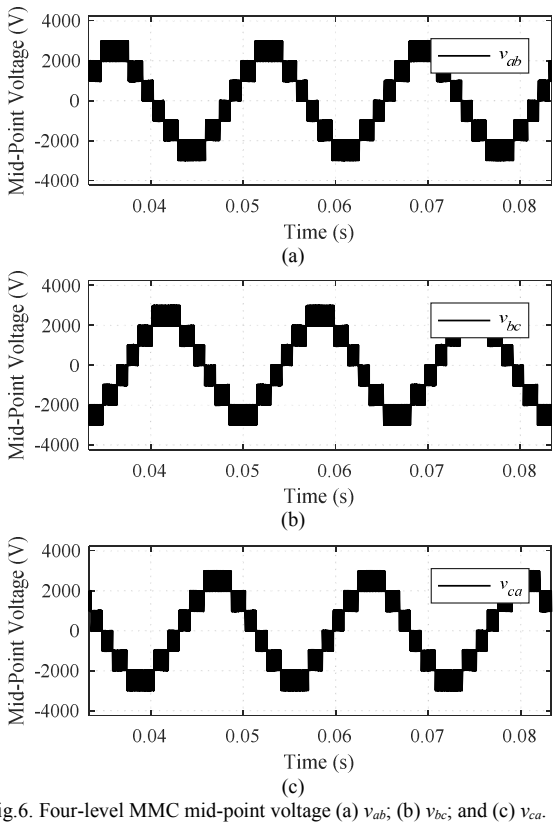

Fig.6. Four-level MMC mid-point voltage (a) v_{ab}; (b) v_{bc}; and (c) v_{ca}.

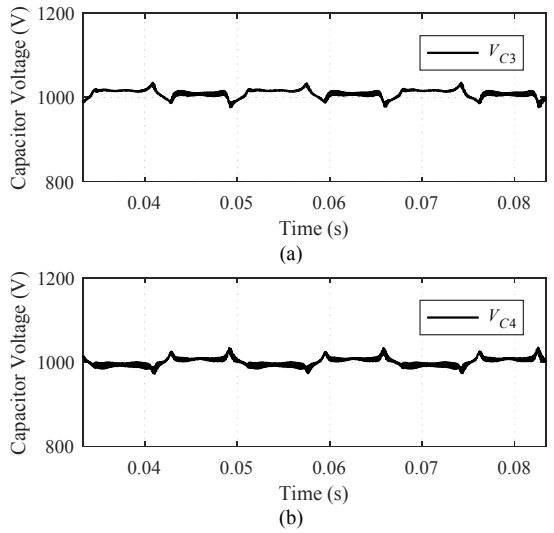

Fig.7. (a)Sub-module capacitor C_3 voltage; and (b)sub-module capacitor C_4 voltage.

$$\hat{\mathbf{Y}}_2^{(4)} = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}, \tag{7}$$

$$\hat{\mathbf{Y}}_3^{(4)} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \end{bmatrix}, \tag{8}$$

$$\mathbf{Y}_4^{(4)} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}. \tag{9}$$

The ranks of (7) and (8) are both four. The ranks of any two adjacent matrices are all five.

The load voltage and current are shown in Fig.9. The mid-point voltage is shown in Fig.10. The mid-point voltage of four-level MMC has more than seven levels as the capacitor voltage deviates from its nominal value. The sub-module capacitor C_3 and C_4 voltages are shown in Fig.11. The capacitor voltages have deviated from its nominal value over 30% after five fundamental cycles. Fig.12 shows all capacitor voltages from phase-A. The initial voltage of all capacitors is 1000 V. Capacitor voltage V_{C1} and V_{C6} are gradually reduced to 0 while V_{C2} to V_{C5} end up in 1500 V.

VI. Conclusions

This paper explores the self voltage balancing feature of four-level MMC. Mathematically, four-level MMC sub-module voltage can be self balanced if utilizing all sub-module patterns. The four-level MMC simulations verify the

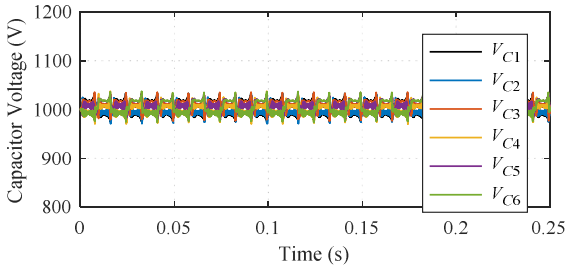

Fig.8. All sub-module capacitor voltages in phase-A.

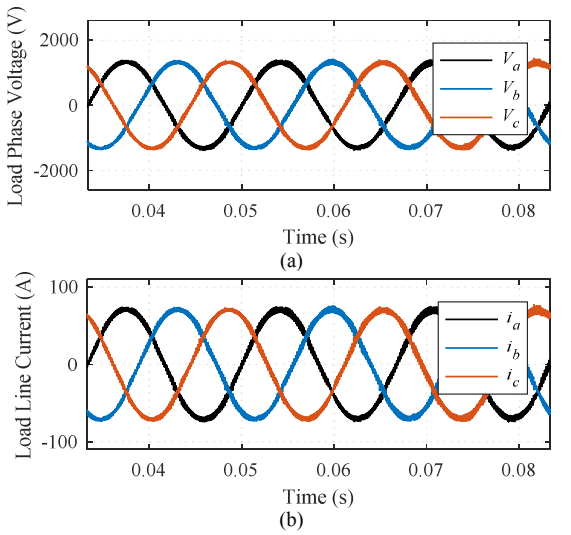

Fig.9. Four-level MMC (a) load voltage and (b) load current.

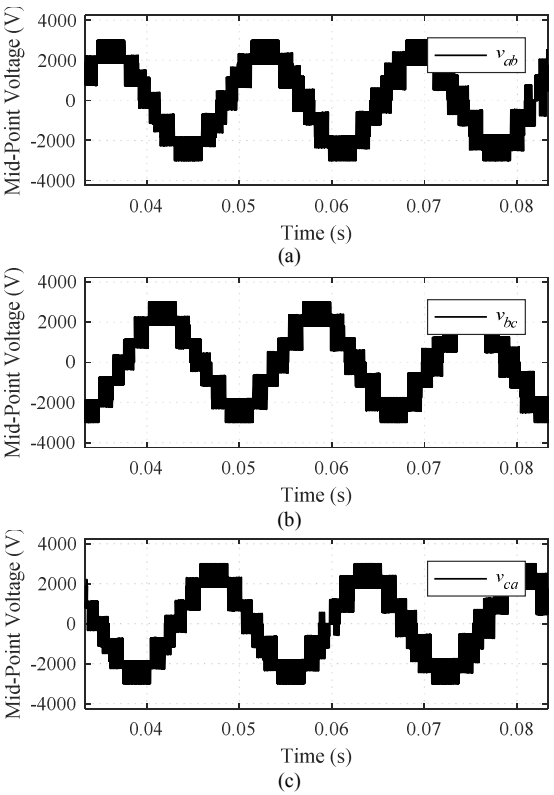

Fig.10. Four-level MMC mid-point voltage (a) v_{ab}; (b) v_{bc}; and (c) v_{ca}.

mathematical proof.

This self voltage balancing feature allows MMC to have a sensorless operation. Compared to the conventional MMCs, the proposed four-level MMC is 1/8th -1/6th the capacitor volume.

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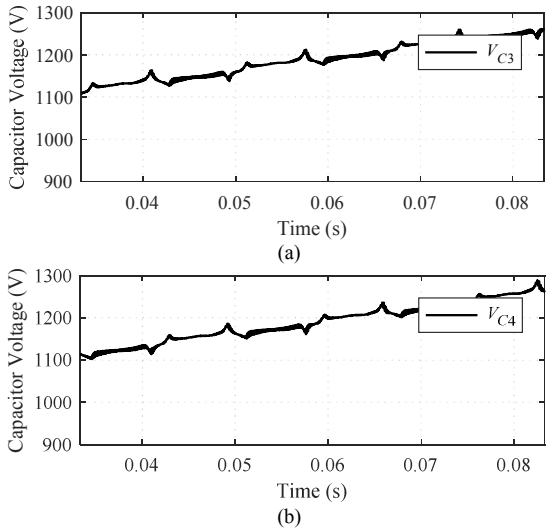

Fig.11. (a)Sub-module capacitor C_3 voltage; and (b)sub-module capacitor C_4 voltage.

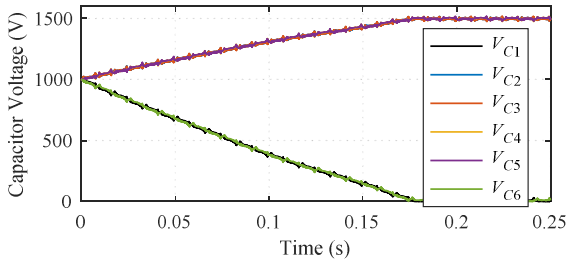

Fig.12. All sub-module capacitor voltages in phase-A.

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