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Automotive 130 nm Smart-Power-Technology including embedded Flash Functionality

Ralf Rudolf, Cajetan Wagner, Lincoln O'Riain, Karl-Heinz Gebhardt, Barbara Kuhn-Heinrich, Birgit von Ehrenwall, Andreas von Ehrenwall
Infineon Technologies AG
01099 Dresden, Germany
Ralf.Rudolf@infineon.com

Marc Strasser, Matthias Stecher, Ulrich Glaser, Stefano Aresu, Paul Kuepper, Alevtina Mayerhofer
Infineon Technologies AG
81726 Munich, Germany
Marc.Strasser@infineon.com

***Abstract*—In this paper a 130 nm BCD technology platform is presented. The process offers logic-devices, flash-devices and high voltage devices with rated voltages up to 60 V. There are HV analog devices with variable channel length and HV power devices with low on-resistances. To ensure the safe operation of the power devices, a superior robustness against high energetic pulses of different length and repetitions could be achieved. The isolation of the different voltage stages is ensured by deep trenches and highly doped buried layers.**

I. Introduction

The suppression of parasitic diodes, bipolar-transistors, and thyristors within a BCD technology is a major challenge which becomes even more important with further shrinkage. Therefore, new isolation concepts superior to the pn-isolation concepts have to be developed. One solution to this problem is an SOI based BCD process. The drawback of SOI is its limited capability to build large power stages. Due to the buried oxide, a weak thermal connection to the substrate is the main drawback of this concept. Hence, the maximal drive current of power stages is limited in the range of 1A. Nevertheless, there are many applications in the area of the automotive electronics where larger current capabilities up to 10A are needed. If the decision is made by choosing a bulk based BCD technology, the suppression of the parasites below the flash-, logic- and analog-areas is of utmost importance. This can be realized by an extremely highly doped n-buried-layer in combination with a low-resistive sinker connection and deep-trench isolation. This allows the integration of 8bit up to 16bit micro-controllers and large power devices within the same BCD chip.

II. The BCD-Process

The presented BCD process integrates logic, analog, memory and power switching functions into one chip. Typical voltages range between 1.2 V up to 60 V and currents from some µA up to 15 A are managed. A basic ULSI-process was extended with power-transistors up to typical breakdown voltages of 75 V at room temperature. For the combination of a ULSI logic/flash process with power devices, the logic areas have to be embedded into a pseudo-substrate (Fig.1). This p-

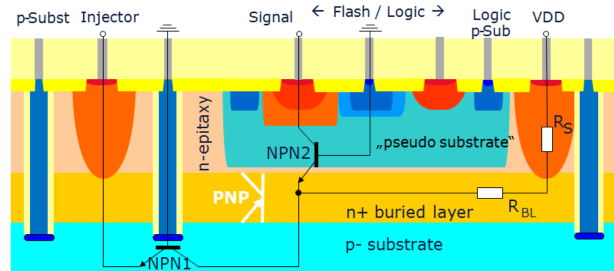
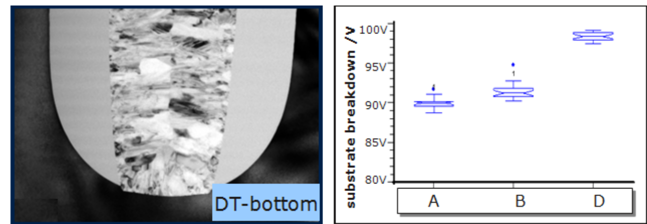


Fig. 1: Schematic cross-section of logic/flash and power areas embedded in silicon with deep trench isolation. The substrate is grounded at each device to minimize EMI.



(a) (b)

Fig. 2: (a) TEM picture of DT-bottom, (b) breakdown voltage from "buried layer" to substrate with different implant doses and thermal budgets.

well is located in the n-doped epitaxial layer. A very high doped n-buried-layer isolates this "pseudo substrate" from the real p-substrate of the wafer. This construction ensures insensitivity of logic blocks to parasitic disturbances coming from the power areas. The power devices are directly embedded into the n-epitaxial wells and are also robustly isolated from each other. One key factor for this robustness is the low gain of the vertical parasitic npn-transistor. The high base doping suppresses the current gain to less than 2%. Deep trench isolation ensures the lateral isolation of the epi-wells. This isolation technique consumes less area and makes far better physical isolation than the former approach of junction isolation achieved. Whilst the current gain of the lateral parasitic substrate-npn (NPN1) has been reduced by fifty percent, the breakdown voltage from buried-layer to substrate

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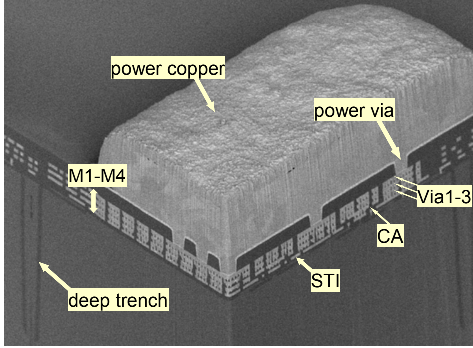

Fig. 3: Micro-image of a typical layer stack.

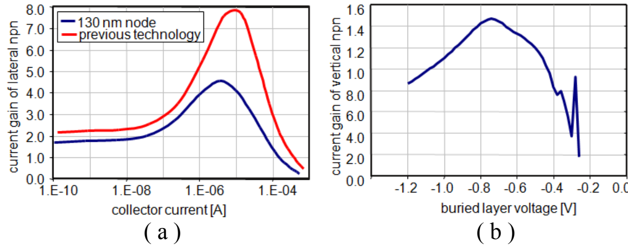

Fig. 4: current gain (a) of the lateral parasitic transistor (NPN1) and beta (b) of the vertical npn (NPN2) according to Fig.1

has been adjusted to be well above 90 V at room temperature. Additional experiments showed the direction for further improvement by adjusting the thermal budget and doping concentration at the pn-junction (Fig.2b). In contrast to fully isolating trenches, presented for different technologies [e.g. 10], a new trench isolation concept was chosen. It allows the connection of bulk substrate from the top of the wafer. The oxide liner has been removed from the deep trench bottom and the poly-fill directly connects the silicon substrate (Fig. 2a). These connections increase the EMI robustness and lead to a less complicated package since in case of isolated trenches the substrate has to be connected from the backside of the chip.

The BCD process presented also offers a three layer dual-damascene copper metallization and a single-damascene copper layer with tungsten plugs. This metal stack, suitable for high packing densities, is combined with a thick copper layer on top to enable thermal and mechanical robustness of the assembled chips (Fig. 3).

III. Suppression of Parasites between Power- and Logic/Analog/Flash-circuit Blocks

One of the major concerns in smart power circuits is the operation of large N-LDMOS stages below substrate-GND. This can appear in different applications e.g. in bridge-drivers or high-side switches during each switching cycle or in failure modes due to wire harness shorts [9]. During these operation modes, large electron currents are injected into the substrate. If they do not recombine in the substrate or at the bottom of the wafer, this electron current causes a voltage drop along "buried layers" and sinker connections. If the resistivity of these regions is not sufficiently low and the current gain of the lateral parasitic NPN-transistor is not small enough, then the "buried layer" becomes negative and the vertical parasitic NPN-transistor is turned on. Depending on the current gain of

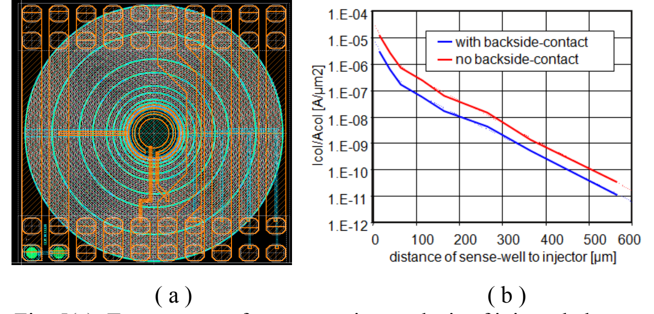

Fig. 5(a): Test structure for propagation analysis of injected electron current, if the injector in the middle is forced below ground; (b) collected current density versus distance of sense well, if a current of 1 A is injected into substrate

device	voltage class	RonA [mΩxmm^2]	Vtrigger [V]
N-LDMOS	30 V	33	50
	45 V	50	65
	60 V	70	80
P-LDMOS	30 V	75	55
	40 V	130	75
	60 V	200	85

Tab. 1: List of available power DMOS devices with respective on-resistances and SOA trigger voltages (@E_{OX}=|2.7 MV/cm|, TLP-measurement with 100ns pulses)

this transistor, a malfunction of circuit blocks could be the consequence. To analyze this effect in conjunction with our process/device concept, a special detection structure was created. Large detectors were placed circularly around a single injector (Fig. 5a). The main finding after measurement is the correlation of collected current in logic/flash-areas versus distance to the injector. The existence of a back side contact is of minor significance.

IV. Devices

The smart power process presented offers logic-devices (1.5 V class), flash-devices of medium voltage (5 V class) and high voltage devices (up to 60 V class). For the high voltage power devices, the lateral DMOS concept of charge compensation is used. As the underlying logic/flash process is based on STI isolation, the field plates of the power devices are now located on STI instead of field oxide as in previous technologies. Tab.1 gives the list of available power DMOS devices and shows their very low on-resistances [7][8]. As a measure of the robustness of the devices the trigger voltage is added to the table (see also Fig. 7). Due to the higher mobility of electrons N-LDMOS-transistors are preferred compared to P-LDMOS in output stages of BCD technologies. Nevertheless, the EMI requirements have been increased in recent years so drastically that high-side power stages realized with N-LDMOS stages in conjunction with charge pump circuits have become unattractive. Hence, this BCD-technology combines power N-LDMOS for different voltage classes and the corresponding P-LDMOS transistors. Also, high voltage analog MOS devices with variable channel

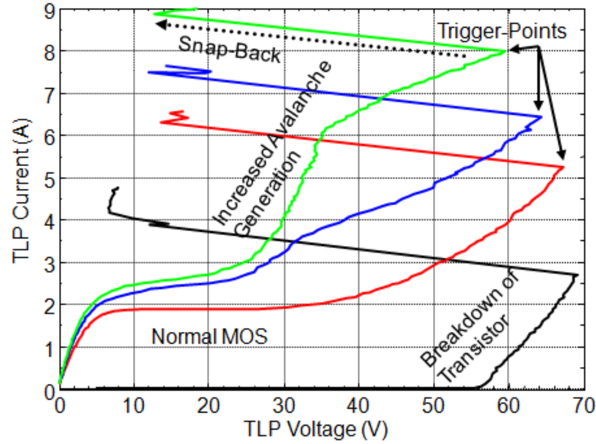

Fig. 6: Typical electrical SOA of integrated lateral 45V N-LDMOS device, measured by TLP for different gate voltages.

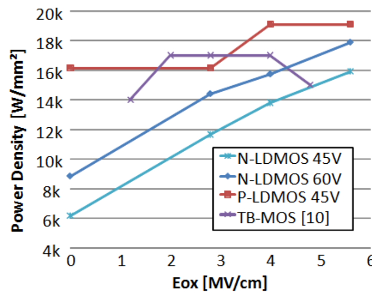

Fig. 7: e-SOA-comparison between lateral DMOS-Transistors and a Trench-Based MOS (TB-MOS) presented by [10]

length, diodes, bipolar transistors, resistors and capacitors are available for the presented smart power technology platform.

V. Electrical Device-Robustness

All integrated power-transistors have to be robust against high energetic pulses. In some applications these devices may be connected directly to the cable harness within cars. Demanding ESD-requirements have to be fulfilled, not only for automotive applications. The measure of this robustness is the electrical safe-operating-area (e-SOA) shown as example of the N- and P-LDMOS-transistor (Fig. 6 and 8). The e-SOA has been analyzed with TLP pulses having a pulse width of 100ns and a rise-time of 10ns. During these events the gates were biased to substantially higher voltages than in normal operations. The higher the snap-back voltages and currents ("trigger points") the better is the e-SOA. The ESD-performance can be calculated directly from this characteristic. The calculated power density for the 45V-N-LDMOS can be given from 6kW/mm² to 16kW/mm² depending on the gate bias (Fig.8). For the 60V-N-LDMOS the power density is roughly 2kW/mm² higher for all gate voltages compared to the 45V-device. The P-LDMOS exhibits an almost constant power-density independent of the gate voltage at around 17.5kW/mm². For comparison, the lateral and vertical MOS-transistors reported in [10] show much lower power densities, only a special trench based MOS-transistor reaches the power density of 17W/mm² as a

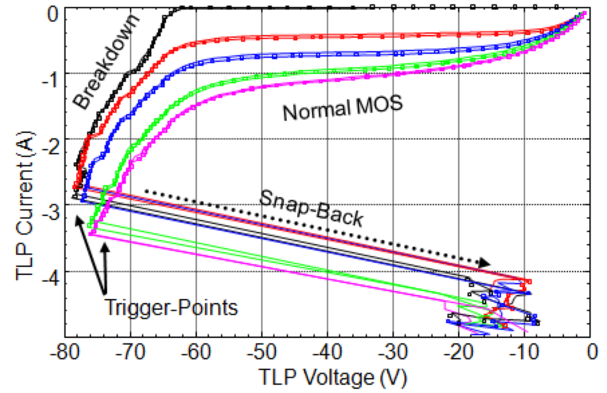

Fig. 8: Typical electrical SOA of integrated power 40V P-LDMOS device, measured by TLP for different gate voltages.

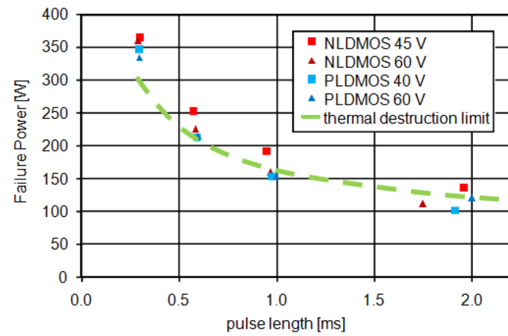

Fig.9: Power dissipation limit of the LDMOS at maximum

maximum value. To obtain this excellent result for our lateral DMOS-transistors, the parasitic internal bipolar transistors of the MOS devices had to be suppressed. This could be realized by optimization of doping profiles and device layouts [4][5].

It is known that lateral DMOS transistors are strongly affected by hot carrier injection in the silicon oxide interface [9]. Moreover, with the introduction of STI instead of field oxide a potential risk arose for device reliability at extreme operative conditions (i.e. high electric field, high power, high temperature swing). However, it was possible with cautious optimized processes to have a significant low drift of the device parameters over the complete lifetime.

VI. Thermal Device-Robustness

In case of disturbance-pulses of several micro-seconds the electro-thermal-SOA has to be evaluated to predict the robustness of the power stages against electrical overstress (EOS). The pure thermal SOA (thermal destruction limit) indicates when a destructive temperature of 500 °C is reached depending on pulse length and dissipated power (see Fig. 9). This superior thermal-SOA could be reached by using a several µm thick copper metallization layer on top of the chip (see Fig. 3). This so called Power-Copper metallization layer increases the thermal capacitance of the output stage [4]. Furthermore it improves the repetitive clamping robustness in applications like ABS and magnetic valve switching within combustion machines. Here, the electro-thermo-mechanical robustness of the signal metallization is significantly improved

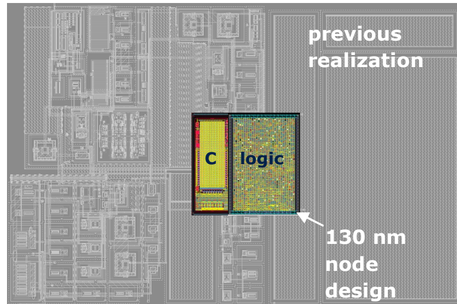

Fig. 10: Area saving by feature shrinks to 130 nm node and replacement of the analog control circuitry by an area-efficient digital based switched capacitor circuitry.

due to the cooling effect of the heat buffering Power-Copper layer [11]. Depending on the device characteristics of the transistor, i.e. its parasitic bipolar and its TCP, the electro-thermal failure behavior can deviate from the pure thermal one. Fig. 9 also shows the electro-thermal-SOA of the presented 45V N-LDMOS and 40V P-LDMOS devices. Except for long pulses, where the thermal boundary conditions of the package and introduced uncertainties become important, the devices perform better than thermally expected. In combination with an electro-thermal FEM simulator the optimum layout can be found to ensure device integrity even for the most critical pulses in application [15].

VII. System Benefits

New ULSI technologies such as the BCD-process presented will have a major impact on future IC-designs and circuit concepts. The huge packing density of the logic blocks will allow new features without remarkable cost adders. Also, analog circuits may be replaced by logic blocks with an extreme area reduction. To enable the efficient replacement of analog control circuits by logic ones, lateral metal-metal capacitances are included. Fig.10 shows the shrink capability for a switched capacitor circuitry. The combination of microcontroller, flash-memory and power devices is the key for system integration with improved reliability and flexibility. Beside the pure silicon costs, the expenses for packaging and test are the main driver for the overall system costs. Higher degrees of integration and digitalization will also help to reduce these costs further.

VIII. Results

The ULSI-BCD automotive power technology platform presented allows for efficient design shrinks. For power MOS device design, an optimum balance of on-resistance, breakdown voltage, HCS- and SOA-behavior was achieved. The devices show very competitive on-resistances. The use of STI instead of field oxides shows no draw-back in terms of increased HCS drift effects. The SOA of the devices is optimized to ensure sufficient headroom for ESD protection. Moreover, the electro-thermal behavior of the power devices is understood. Thus, predictive dimensioning can prevent EOS for critical pulses. Due to the copper dual damascene metallization in combination with a thick copper heat buffer layer, the mechanical robustness of the metal stack in repetitive pulsing is increased by more than one order of magnitude in lifetime compared to conventional aluminum metallization.

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