Parallel Loopback Test of Mixed-Signal Circuits

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Abstract

Parallel testing of mixed-signal circuits has been considered a difficult task due to the limited resources in generating and analyzing multiple analog signals. A number of methods have been proposed to perform parallel testing of mixed-signal circuits using built-in test circuitry; however, these techniques are vulnerable to fault masking issues which may degrade the test accuracy. This paper presents an efficient parallel test algorithm for mixed-signal circuits based on a loopback test method. Multiple DUTs (Devices Under Test) are loopbacked externally on a loadboard which is loaded with a simple analog adder and an RMS detector. The performance parameters of each DUT are calculated separately from the composite responses, while removing the effect of fault masking. Parallelism is increased by sharing common test equipment and a DUT loadboard among the multiple DUTs. The mathematical theory and simulation results are presented to validate our algorithm.

1. Introduction

The trend of increasing performance and speed of mixed-signal devices, along with the complexity of these devices, results in increased test cost and test time. In recent integrated circuit development, test cost represents a significant portion of the overall production cost [1]. Thus, reducing the test cost becomes one of the most important issues in mixed-signal IC development.

There has been substantial research effort to reduce test time and cost by examining various aspects of test [4]. One way to reduce test cost is to increase the test throughput by testing multiple DUTs in parallel [2], [3]. This method of *parallel testing* or *multi-site testing* has been widely used in memory and digital test areas and has recently gained popularity in the mixed-signal test area [3], [5]. However, due to limited I/O pin count and complexity of analog test components inside a mixed-signal tester, the number of mixed-signal devices that can be tested simultaneously has been restricted to a small number. The ITRS (International Technology Roadmap for Semiconductors) report indicates that memory testers can support up to 512 parallel tests, while the mixed-signal testers can support up to 8 by year 2007 [1], [6].

In order to increase the degree of parallelism beyond the level limited by the tester, various DFT (Design-For-Test) and BIST (Built-In Self Test) techniques have been proposed in mixed-signal circuit test area [3]-[4], [7]-[14]. These techniques can be divided into two categories; one is to share the tester resources among multiple DUTs and the other is to implement tester functionality on the chip. In the first approach, efforts have been made to share test equipment among multiple DUTs using various multiplexing algorithms [3], [7], [8]. These techniques require less test equipment than the number of DUTs tested in parallel. Thus, test throughput can be increased while test cost can be reduced. In the second approach, various techniques have been proposed to implement tester functions such as analog waveform generation, digitization and signal processing on chip [10]–[13]. These functions can be implemented by reusing existing modules on chip or designing separate built-in test circuitry. For example, analog waveforms can be generated on chip using a DAC (Digital-to-Analog Converter) or oscillator, and digitization can be implemented using an ADC (Analog-to-Digital Converter), and signal processing can be done using an on-chip DSP. By using on-chip test circuitry, we can replace analog test inputs or outputs with digital signals. Considering that digital signals are easier to generate and replicate than analog signals, these techniques can help increase the parallelism by sharing digital I/O pins in a mixed-signal tester or digital tester [14].

These techniques, however, are vulnerable to fault masking which may lead to considerable yield loss and low test accuracy [18]. Fault masking occurs when the test response from one DUT is corrupted by interactions from other modules which share the same functional path with the DUT. This leads to misinterpretation of the test response observed at the output node, thus, a pass/fail decision based on this observation may be wrong. In parallel test methods described above, erroneous operations

of on-chip test circuitry may corrupt the test response of the DUT. Also, there can be fault masking among multiple DUTs sharing common test equipment. In such cases, fault masking can cause a normal DUT to be discarded or a faulty DUT to escape the test [4].

We present an efficient parallel test algorithm, called *parallel loopback test* which increases the level of parallelism in mixed-signal test without suffering from the fault masking problem. Our algorithm is targeted to parallel testing of multiple mixed-signal circuits in loopback mode. We use the example of testing a DAC and an ADC in loopback mode. In parallel loopback test, multiple sets of the ADC/DAC pairs are tested in parallel using a common DUT loadboard which consists of a simple analog adder and an RMS detector. Outputs of the DACs are connected to inputs of the ADCs through the loadboard to form the loopback path. The resulting test setup has digital inputs and digital outputs, so expensive analog waveform generators and digitizers are not required in our algorithm. The test input comes from a digital signal generator which can be shared among multiple DUTs. The individual performance parameters of the DUTs are calculated by measuring loopback responses captured at the output of the ADCs. The analog adder and the RMS detector on the loadboard are used to extract the performance parameters of multiple DUTs separately and to suppress the effect of fault masking. The presented algorithm can help reduce the cost and time of testing mixed-signal circuits without compromising the test accuracy.

This paper is organized as follows. Section 2 reviews previous work and issues of parallel test, while Section 3 presents the proposed testing procedure, detailing its topology and mathematical theory. In Section 4, the simulation results to illustrate the effectiveness of our method are presented, and we conclude this paper in Section 5.

2. Parallel Test of Mixed-Signal Circuits

2.1. Previous Work on Parallel Test

The authors in [7] used both time-domain and frequency-domain multiplexing algorithms to share one digitizer among multiple stereo DACs. They implemented multiplexing logic on a DUT board and showed that test time as well as test cost can be reduced by sharing a common digitizer. Recently, Kwan *et al.* [8] proposed an algorithm to test two current steering DACs used in an RF CODEC with one digitizer. The outputs of these DACs are combined using resistor loads and sent to a single digitizer to characterize overall performance. Also, Jin *et al.* [9] presented a technique to test high-resolution DACs on chip using flash ADCs. In their algorithm, high speed on-chip data acquisition and digitization is achieved using ADCs, and thus external equipment is not required.

On the test input generation side, many research groups have proposed on-chip analog signal generation schemes to reduce the need for an AWG (Arbitrary Waveform Generator). The work presented in [12] developed an on-chip signal generator for frequency-domain testing of ADCs. It used a static RAM to generate a digital sine wave and used a $\Sigma\Delta$ generator to convert a digital sine wave into an analog signal. In [13], the authors presented an on-chip ramp generation scheme for time-domain testing of analog circuits and ADCs. Their design requires only a system clock and voltage reference as inputs to a ramp generator; therefore, a complex analog waveform generator is not required. Pan *et al.* [11] proposed a BIST scheme for testing linear analog circuits in which test input generation and response analysis are all done on chip. A LFSR (Linear Feedback Shift Register) and DAC are used to generate test stimulus, and an on-chip DSP and ADC are used to analyze output responses.

2.2. Issues in Parallel Test of Mixed-Signal Circuits

As mentioned in previous section, parallel test methods described above suffer from the fault masking problem. For example, a faulty on-chip signal generator can fail a good DUT or pass a faulty DUT by supplying the DUT with faulty test inputs. Also, an on-chip digitizer can cancel out errors in DUTs due to its own quantization error.

Fault masking issues have been well researched in the loopback test area [15]–[18]. Notable among them are the loopback test methods using an external loadboard [18]–[20]. Components on the loadboard such as an analog filter [18] or RF transformer [19] are used to extract the performance parameters of DUTs from the composite output response. This method looks promising since it does not require built-in test circuitry to observe the internal loopback path, and it maintains good test accuracy, since a pre-characterized loadboard is used for testing. However, there are some issues that hamper this method being applied for parallel mixed-signal test. This method requires dedicated loadboard components for each loopback pair and this will increase the area and power consumption of the loadboard. A commercial tester can normally accommodate multiple DUTs, but this does not consider the increased area and power overhead associated with the loadboard. Thus, having dedicated loadboard components for each loopback pair can cause problems due to limited pin count and insufficient power. Also, the loadboard components have less flexibility, since design parameters of those components should be decided based on the frequency of input tone to the DUT. This means that the loadboard components have to be modified every time a test setup requires different input frequencies to the DUT. This may increase the test cost in reconfiguring the loadboard for different test setups.
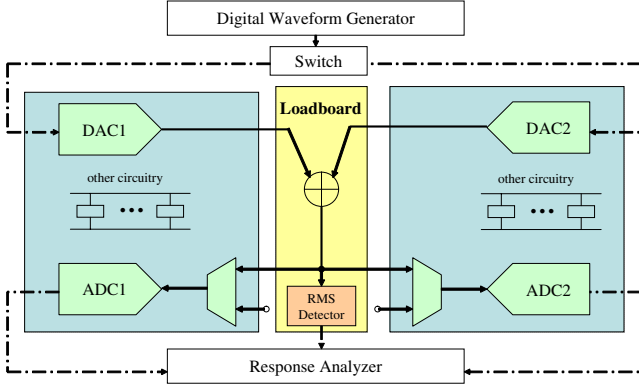
Fig. 1. Proposed Parallel Loopback Test Scheme

The authors in [15] presented an algorithm to test multiple data converters with analog switches and an adder. While this algorithm showed the possibility of performing accurate parallel test of mixed-signal circuits, the authors assumed that the harmonic amplitudes created by the DAC are negligible, which may not be true in practical situations especially when there are faults in the DAC. Also, the noise power calculation was not considered in their algorithm.

3. Parallel Loopback Test Method

The previous section discussed issues related to parallel test of mixed-signal circuits. This section will present the parallel loopback test algorithm and discuss how it can be used to find the performance parameters of the multiple DUTs in parallel. It will also be shown that this algorithm can solve the fault masking problem with a common DUT loadboard whose components are shared among multiple DUTs, and can be used in general for different types of DUTs.

3.1. Harmonic Distortion Calculation

In this section, we describe the parallel loopback test algorithm to characterize the harmonic distortion of DUTs. We first start with two sets of ADC/DAC pairs and later extend the algorithm to test more than two sets of ADC/DAC pairs. Figure 1 shows the parallel loopback test setup where two sets of ADCs and DACs are externally connected to the loadboard. In manufacturing test, we can use a DUT board or probe card as the loadboard as shown in Figure 1. The loadboard has a simple analog adder and an RMS detector which can be characterized prior to use. Outputs of both DACs are connected to the adder and the output of the adder is routed to both ADCs. Thus, DUTs share a common loopback path and there is one module, the analog adder, placed on the loopback path. Since the analog adder can be easily designed to have good linearity [24], we can assume that the harmonic distortion

introduced by the adder is negligible[1]. The input to each DAC is illustrated in Figure 2. We use the t notation in the digital domain for simplicity. It can be seen that the input to both DACs are the same except for the interval where there is no input to the DAC2 (time interval $\mathcal{A}$) and the DAC1 (time interval $\mathcal{B}$). Thus, we can use one waveform generator and a switch to route the input signal to each DAC.

To find the harmonic distortion parameters, first a sine wave input, $A\cos(\omega t)$, with amplitude A is applied to the DAC1 while the input signal path to the DAC2 is disconnected at the switch (time interval $\mathcal{A}$). The amplitude can have any value as long as it does not saturate the ADCs during the time interval $\mathcal{C}$. Figure 2(a) shows the test setup during the time interval $\mathcal{A}$. The outputs of the loopback path I and II are as follows.

$$\hat{y}_{lb1}(t) = y_{lb1}(t) + n_{lb1}(t), \; \hat{y}_{lb2}(t) = y_{lb2}(t) + n_{lb2}(t) \quad (1)$$

where $n_{lb1}(t)$ and $n_{lb2}(t)$ are output noise of loopback path I and II respectively. $y_{lb1}(t)$ and $y_{lb2}(t)$ are Taylor series expansions which can be expressed as follows.

$$y_{lb1}(t) = \delta_{11}A\cos(\omega t) + \delta_{12}A^2\cos^2(\omega t) + \delta_{13}A^3\cos^3(\omega t)$$
$$= (\delta_{11}A + \frac{3\delta_{13}}{4}A^3)\cos(\omega t) + \frac{\delta_{12}}{2}A^2\cos(2\omega t) + \frac{\delta_{13}}{4}A^3\cos(3\omega t)$$
$$(2)$$

$$y_{lb2}(t) = \delta_{21}A\cos(\omega t) + \delta_{22}A^2\cos^2(\omega t) + \delta_{23}A^3\cos^3(\omega t)$$
$$(3)$$

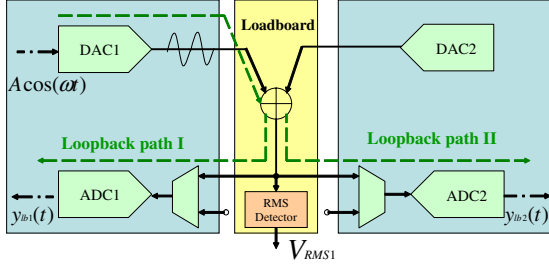where the constants δ_{11} - δ_{23} are as follows.

$$\begin{aligned}
\delta_{11} &= \alpha_1\gamma_1, \quad \delta_{12} = \gamma_1\alpha_2 + \gamma_2\alpha_1^2, \\
\delta_{13} &= \gamma_1\alpha_3 + 2\gamma_2\alpha_1\alpha_2 + \gamma_3\alpha_1^3, \\
\delta_{21} &= \alpha_1\theta_1, \quad \delta_{22} = \theta_1\alpha_2 + \theta_2\alpha_1^2, \\
\delta_{23} &= \theta_1\alpha_3 + 2\theta_2\alpha_1\alpha_2 + \theta_3\alpha_1^3
\end{aligned} \quad (4)$$

In the above equations, α_i, γ_i and θ_i are the ith harmonic distortion coefficients of the DAC1, ADC1 and ADC2 respectively[2]. Since we already know the value of the input amplitude, A, we can find the values of δ_{11} - δ_{23} by measuring the frequency response at ω, 2ω and 3ω. Next, the sine wave input is applied to the DAC2 while the input signal path DAC1 is disconnected (time interval $\mathcal{B}$). The Taylor series expansion of the output of loopback path III, shown in Figure 2(b), is as follows.

$$y_{lb3}(t) = \delta_{31}A\cos(\omega t) + \delta_{32}A^2\cos^2(\omega t) + \delta_{33}A^3\cos^3(\omega t)$$
$$(5)$$

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[1]Even if the adder introduce some nonlinearity, this can be readily characterized since the adder is implemented on the loadboard.
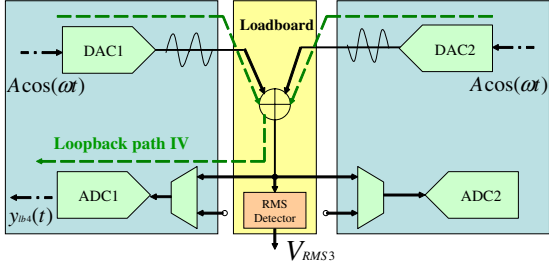
[2]In this paper we consider harmonic distortion up to the third order. However, our method itself is not limited to the third order and it is straightforward to extend to higher orders.

(a) Time Interval $\mathcal{A}$: Test input to DAC1 only
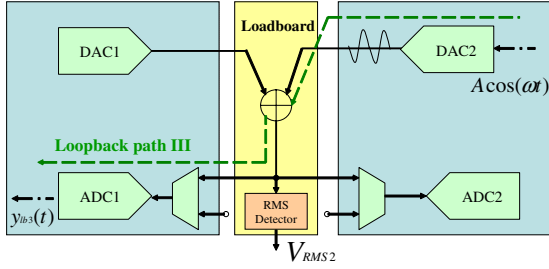
(b) Time Interval $\mathcal{B}$: Test input to DAC2 only

(c) Time Interval $\mathcal{C}$: Test input to DAC1 & DAC2

Fig. 2. Test Setup for Three Time Intervals

where the constants δ_{31}, δ_{32} and δ_{33} are as follows.

$$\begin{aligned} \delta_{31} &= \beta_1\gamma_1, \quad \delta_{32} = \gamma_1\beta_2 + \gamma_2\beta_1^2, \\ \delta_{33} &= \gamma_1\beta_3 + 2\gamma_2\beta_1\beta_2 + \gamma_3\beta_1^3, \end{aligned} \quad (6)$$

and β_i are the ith harmonic distortion coefficients of the DAC2. Finally, the sine wave input is applied to both DACs during time interval $\mathcal{C}$. Then, the Taylor series expansion of the output of loopback path IV is as follows.

$$\begin{aligned} y_{lb4}(t) &= \delta_{41}A\cos(\omega t) + (\delta_{12} + \delta_{32} + 2\delta_{42})A^2\cos^2(\omega t) \\ &\quad + (\delta_{13} + \delta_{33} + \delta_{43})A^3\cos^3(\omega t) \end{aligned} \quad (7)$$

where three constants δ_{41}, δ_{42} and δ_{43} are as follows.

$$\begin{aligned} \delta_{41} &= (\alpha_1 + \beta_1)\gamma_1, \quad \delta_{42} = \gamma_2\alpha_1\beta_1, \\ \delta_{43} &= 3\gamma_3\alpha_1\beta_1(\alpha_1 + \beta_1) + 2\gamma_2(\alpha_1\beta_2 + \beta_1\alpha_2) \end{aligned} \quad (8)$$

Using Equations 4, 6 and 8, we can formulate 11 linearly independent equations. This means that we do not have sufficient equations to find the values of all 12 harmonic distortion coefficients, α_{1-3}, β_{1-3}, γ_{1-3} and θ_{1-3}. Instead of finding absolute values of all 12 coefficients directly, we can first express 11 coefficients in terms of the 1 remaining coefficient called the *reference variable*. In this paper, we use α_1 as the reference variable. After several steps of calculations, we can formulate the following equations from Equations 4, 6 and 8.

$$\begin{bmatrix} \alpha_1 & \beta_1 \\ \alpha_2 & \beta_2 \\ \alpha_3 & \beta_3 \end{bmatrix} = \begin{bmatrix} 1 & C_{\beta_1} \\ C_{\alpha_2} & C_{\beta_2} \\ C_{\alpha_3} & C_{\beta_3} \end{bmatrix} \begin{bmatrix} \alpha_1 & 0 \\ 0 & \alpha_1 \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} \gamma_1 & \theta_1 \\ \gamma_2 & \theta_2 \\ \gamma_3 & \theta_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{\alpha_1} & 0 & 0 \\ 0 & \frac{1}{\alpha_1^2} & 0 \\ 0 & 0 & \frac{1}{\alpha_1^3} \end{bmatrix} \begin{bmatrix} C_{\gamma_1} & C_{\theta_1} \\ C_{\gamma_2} & C_{\theta_2} \\ C_{\gamma_3} & C_{\theta_3} \end{bmatrix} \quad (10)$$

where the values of $C_{\alpha_{2-3}}$, $C_{\beta_{1-3}}$, $C_{\gamma_{1-3}}$ and $C_{\theta_{1-3}}$ can be expressed as Equation 11 shown in next page. Now, if we can find the value of the *reference variable* (α_1), all the harmonic distortion coefficients can be calculated using Equations 9, 10 and 11. In our algorithm, we use an RMS detector to find the value of the reference variable, α_1. Using current technology, the RMS detector can be designed to operate at speeds up to a few GHz while the detection error can be held less than 5% [21], [22]. Also, the output of the RMS detector has a DC value, and thus it can be measured using low-cost test equipment.

The DC values measured at output of the RMS detector during the time interval $\mathcal{A}$, $\mathcal{B}$ and $\mathcal{C}$ can be expressed as follows.

$$\begin{aligned} V_{RMS1} &= [(\frac{1}{2}A^2 + \frac{3}{8}(C_{\alpha2}^2 + 2C_{\alpha3})A^4 \\ &\quad + \frac{5}{16}C_{\alpha3}^2A^6)\alpha_1^2 + \overline{v_{DAC1}^2}]^{0.5} \end{aligned} \quad (12)$$

$$\begin{aligned} V_{RMS2} &= [(\frac{1}{2}C_{\beta1}^2A^2 + \frac{3}{8}(C_{\beta2}^2 + 2C_{\beta3})A^4 \\ &\quad + \frac{5}{16}C_{\beta3}^2A^6)\alpha_1^2 + \overline{v_{DAC2}^2}]^{0.5} \end{aligned} \quad (13)$$

$$\begin{aligned} V_{RMS3} &= [(\frac{1}{2}(1 + C_{\beta1})^2A^2 + \frac{3}{8}(C_{\alpha\beta2}^2 + 2C_{\alpha\beta3})A^4 \\ &\quad + \frac{5}{16}C_{\alpha\beta3}^2A^6)\alpha_1^2 + \overline{v_{DAC1}^2} + \overline{v_{DAC2}^2}]^{0.5} \end{aligned} \quad (14)$$

Where $C_{\alpha\beta2} = C_{\alpha2} + C_{\beta2}$ and $C_{\alpha\beta3} = C_{\alpha3} + C_{\beta3}$. Also, $\overline{v_{DAC1}^2}$ and $\overline{v_{DAC2}^2}$ are the output noise power of the DAC1 and DAC2, respectively. We assume that output noise of DAC1 and DAC2 is uncorrelated. Equations 12-14 are linearly independent, while there are three unknown variables, α_1, $\overline{v_{DAC1}^2}$ and $\overline{v_{DAC2}^2}$, in these equations. So, we can find the value of α_1 using Equations 12-14,

$$C_{\gamma_1} = \delta_{11}, \quad C_{\beta_1} = \frac{\delta_{31}}{\delta_{11}}. \quad C_{\theta_1} = \delta_{21}, \quad C_{\gamma_2} = \frac{\delta_{11}\delta_{42}}{\delta_{31}}, \quad C_{\alpha_2} = \frac{\delta_{12} - C_{\gamma_2}}{C_{\gamma_1}}, \quad C_{\beta_2} = \frac{\delta_{32} - C_{\beta_1}^2 C_{\gamma_2}}{C_{\gamma_1}},$$

$$C_{\theta_2} = \delta_{22} - C_{\theta_1} C_{\alpha_2}, \quad C_{\gamma_3} = \frac{\delta_{43} - 2C_{\gamma_2}(C_{\beta_2} + C_{\beta_1} C_{\alpha_2})}{3C_{\beta_1}(1 + C_{\beta_1})}, \quad C_{\alpha_3} = \frac{\delta_{13} - C_{\gamma_3} - 2C_{\gamma_2} C_{\alpha_2}}{C_{\gamma_1}}, \quad (11)$$

$$C_{\beta_3} = \frac{\delta_{33} - C_{\beta_1}^3 C_{\gamma_3} - 2C_{\gamma_2} C_{\beta_2} C_{\beta_1}}{C_{\gamma_1}}, \quad C_{\theta_3} = \delta_{23} - C_{\theta_1} C_{\alpha_3} - 2C_{\theta_2} C_{\alpha_2}$$

and successively find the remaining values of harmonic distortion coefficients, α_{2-3}, β_{1-3}, γ_{1-3} and θ_{1-3}, using Equations 9, 10 and 11.

The adder and the RMS detector used in our algorithm can work with different input frequencies without changing the configuration. This means that our algorithm can be flexibly applied to various test setups without reconfiguring the loadboard, and thus help reduce the test cost.

3.2. Noise Power Calculation

In this section, we describe the algorithm to find the noise power of DUTs using the parallel loopback test.

First, assume that $\sqrt{K_{\alpha\gamma}}$ is the overall gain of the loopback path which consists of DAC1 and ADC1 (loopback path I at time interval $\mathcal{A}$). The value of $\sqrt{K_{\alpha\gamma}}$ can be calculated using harmonic distortion coefficients found in the previous section. Also, assume that $n_\alpha(t)$ and $n_\gamma(t)$ are the output referred noise of the DAC1 and ADC1 respectively. Then, output of the loopback path I can be expressed as follows.

$$\hat{y}_{lb1}(t) = y_{lb1}(t) + \sqrt{K_{\alpha\gamma}} n_\alpha(t) + n_\gamma(t) \quad (15)$$

where $y_{lb1}(t)$ is given in Equation 3 and two noise components, $n_\alpha(t)$ and $n_\gamma(t)$, are assumed to be uncorrelated with each other. By performing frequency analysis at the output of the loopback path I, we can extract the noise components from the signal tone and its harmonics, and calculate the noise power [23]. The calculated noise power, $\overline{v_{lb1}^2}$, can be expressed as follows.

$$\overline{v_{lb1}^2} = \int_0^\infty K_{\alpha\gamma} N_\alpha(f) df + \int_0^\infty N_\gamma(f) df \quad (16)$$

where $N_\alpha(f)$ and $N_\beta(f)$ are the Power Spectral Density (PSD) of the output referred noise of the DAC1 and ADC1 respectively. Applying similar approaches to the loopback path II at time interval $\mathcal{A}$, the loopback path III at time interval $\mathcal{B}$ and the loopback path IV at time interval $\mathcal{C}$, we can formulate the following equations.

$$\overline{v_{lb2}^2} = \int_0^\infty K_{\alpha\theta} N_\alpha(f) df + \int_0^\infty N_\theta(f) df \quad (17)$$

$$\overline{v_{lb3}^2} = \int_0^\infty K_{\beta\gamma} N_\beta(f) df + \int_0^\infty N_\gamma(f) df \quad (18)$$

$$\overline{v_{lb4}^2} = \int_0^\infty [K_{\alpha\gamma} N_\alpha(f) + K_{\beta\gamma} N_\beta(f)] df + \int_0^\infty N_\gamma(f) df \quad (19)$$

where $N_\beta(f)$ and $N_\theta(f)$ are the noise PSD of the DAC2 and ADC2 respectively, and $\overline{v_{lb2}^2}$, $\overline{v_{lb3}^2}$ and $\overline{v_{lb4}^2}$ are the output noise power of the loopback paths II, III and IV respectively. Also, $K_{\alpha\theta}$ and $K_{\beta\gamma}$ are the overall gain of the loopback paths consisting of DAC1/ADC2 and DAC2/ADC1, respectively. Now, using the Equations 16 - 19, and given $K_{\alpha\gamma}$, $K_{\alpha\theta}$ and $K_{\beta\gamma}$, the noise power of each DUT can be calculated as follows.

$$\int_0^\infty N_\alpha(f) df = \frac{\overline{v_{lb4}^2} - \overline{v_{lb3}^2}}{K_{\alpha\gamma}}$$

$$\int_0^\infty N_\beta(f) df = \frac{\overline{v_{lb4}^2} - \overline{v_{lb1}^2}}{K_{\beta\gamma}}$$

$$\int_0^\infty N_\gamma(f) df = \overline{v_{lb1}^2} + \overline{v_{lb3}^2} - \overline{v_{lb4}^2} \quad (20)$$

$$\int_0^\infty N_\theta(f) df = \overline{v_{lb2}^2} - \frac{K_{\alpha\theta}}{K_{\alpha\gamma}}(\overline{v_{lb4}^2} - \overline{v_{lb3}^2})$$

Now that we have found the harmonic distortion parameters and the noise power, we can calculate the performance parameters of each DUT such as SNR, SNDR, THD, etc. [4]. Also, these results can be used to characterize the amplitude mismatch between different ADCs or different DACs which is an important parameter in RF/Audio CODEC where there are normally two sets of the ADCs and DACs used for the I and Q channels.

3.3. Parallel Loopback Test Algorithm for Multiple DUTs

So far, we have presented the parallel loopback test algorithm which can test two sets of ADC/DAC pairs in parallel using a common test equipment including a loadboard. This algorithm can be easily extended to the case where there are more than two sets of ADC/DAC pairs. In this section, we describe the extension of the parallel loopback test algorithm that can be used to test multiple DUTs with a common test equipment.

Figure 3 shows the case where there are N sets of ADC/DAC pairs tested in parallel ($2N$ DUTs total). The maximum number of DUTs that can be tested in parallel depends on the driving capacity of the analog adder. In this paper, we assume that the adder can drive N DUTs in parallel. Also, note that, although we used the same number of the DACs and ADCs in this section, this number does not have to be same in our algorithm.
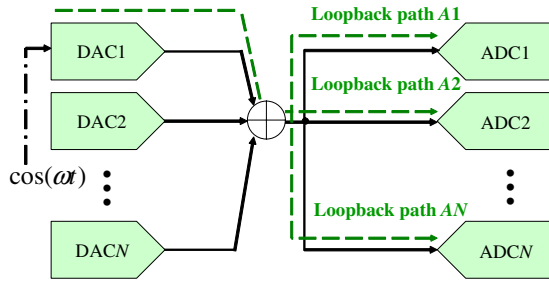
(a) Test Setup for ADCs
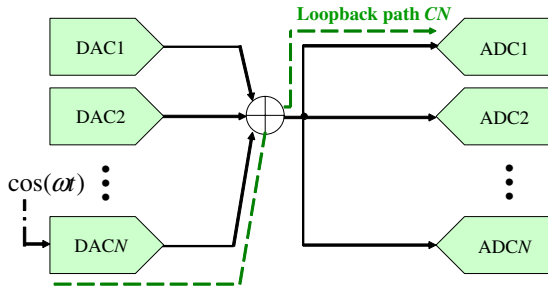
(b) Test Setup for DACs

Fig. 3. Application of the Parallel Loopback Test to Multiple DUTs

First, the harmonic distortion coefficients and the noise power of the DAC1, DAC2, ADC1 and ADC2 are measured using the procedure described in the previous sections. Next, we can measure the harmonic distortion coefficients of all the remaining ADCs by examining the measured output response at each ADC during time interval $\mathcal{A}$. Note that this step does not require additional test inputs to the DUTs. For example, the following equation describes the output of the ADCN at time interval $\mathcal{A}$.

$$
\begin{aligned}
y_{lbN}(t) =& \alpha_1 \rho_1 \cos(\omega t) + (\rho_1 \alpha_2 + \rho_2 \alpha_1^2) \cos^2(\omega t) \\
&+ (\rho_1 \alpha_3 + 2\rho_2 \alpha_1 \alpha_2 + \rho_3 \alpha_1^3) \cos^3(\omega t)
\end{aligned}
\quad (21)
$$

where ρ_i are the ith harmonic distortion coefficients of the ADCN. Since we already know the value of the α_1, α_2 and α_3, we can calculate the harmonic distortion coefficients of the ADCN from Equation 21. The output noise power of the loopback path AN shown in Figure 3(a) can also be calculated and expressed as follows.

$$
\overline{v_{lbN}^2} = \int_0^\infty K_{\alpha\rho} N_\alpha(f) df + \int_0^\infty N_\rho(f) df \quad (22)
$$

Now using the values of $\int_0^\infty N_\alpha(f) df$, $\overline{v_{lbN}^2}$ and $K_{\alpha\rho}$ which we already know, we can calculate the noise power of the DACN, $\int_0^\infty N_\rho(f) df$. The same approach can be applied to all the remaining ADCs.
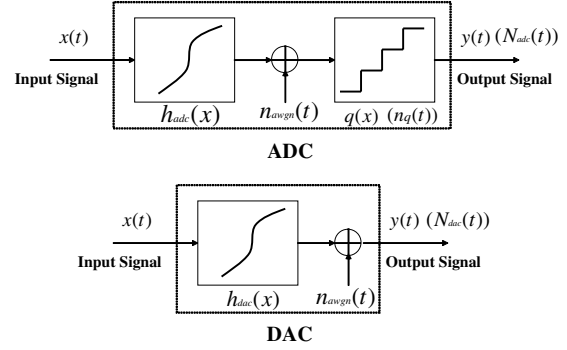

Fig. 4. Nonlinear ADC and DAC Model

We can use a similar approach to find the harmonic distortion coefficients and the noise power of the remaining DACs. The difference is that, this time, a digital sine wave input, $\cos(\omega t)$, should be applied to the DAC that we want to test. For example, to find the performance parameters of the DACN shown in Figure 3(b), the sine wave input is applied to the DACN and the output of the loopback path CN, $y_{lbCN}(t)$, is captured at the ADC1. Now, by post-processing the output, $y_{lbCN}(t)$, we can formulate the Taylor series expansion and noise equation similar to Equations 21 and 22. Since we already know the harmonic distortion coefficients (γ_1, γ_2 and γ_3) and the noise power ($\int_0^\infty N_\gamma(f) df$) of the ADC1, we can use this information to find the harmonic distortion coefficients and the noise power of the DACN.

4. Simulation Results

The method described in this paper was applied to a 14-bit DAC and a 14-bit Sample and Hold ADC (S/H ADC) with MATLAB simulation. We modeled the ADC and the DAC as shown in Figure 4. The ADC is divided into two blocks: the first block models the dynamic nonlinearity of the ADC which is represented as $h_{adc}(x)$, and the second block models the quantization process which is represented as $q(x)$. Also, we assumed a noisy ADC and added white Gaussian noise, $n_{awgn}(t)$, to the output of the nonlinear circuit. Then the output noise $N_{adc}(t)$ consists of Gaussian noise, $n_{awgn}(t)$, and the quantization noise, $n_q(t)$, generated during the quantization process. The DAC is modeled similar to the ADC, except that there is no quantization block in the DAC module.

For simulation, we generated 100 ensembles of the ADC and the DAC models by introducing statistical variations with a Gaussian distribution in parameters of nonlinear functions, $h_{adc}(x)$ and $h_{dac}(x)$, and power of the additive noise, $n_{awgn}(t)$ described in Figure 4. Two sets of ADC and DAC pairs were used to set up the parallel loopback scheme as shown in Figure 1 and three performance parameters, *Signal-to-Noise Ratio* (SNR), *Total Harmonic*

TABLE II. Mean and Standard Deviation of Performance Parameter Prediction Error

Parameter		DAC1	DAC2	ADC1	ADC2
SNR	Mean	0.37dB	0.38dB	0.41dB	0.45dB
	STD	0.65dB	1.13dB	1.07dB	0.90dB
THD	Mean	0.31dB	0.32dB	0.40dB	0.34dB
	STD	0.40dB	0.48dB	0.60dB	0.43dB
SNDR	Mean	0.21dB	0.19dB	0.19dB	0.24dB
	STD	0.37dB	0.31dB	0.29dB	0.35dB

Distortion (THD) and *Signal-to-Noise-and-Distortion Ratio* (SNDR), were measured using the proposed algorithm.

Figure 5 shows the plots of the predicted versus the actual values of each DUT performance parameter. Table II summarizes the mean and standard deviation of error between predicted values and actual values of performance parameters. It can be seen from the results that prediction errors were less than 2dB in all cases.

Next, we applied our algorithm to the case where there are 10 DUTs (5 ADCs and 5 DACs). Figure 6 shows the mean and the standard deviation of prediction errors. We can see that the prediction errors did not increase compared to the case where there were 4 DUTs and this means that our algorithm works well with the increased number of DUTs. It can also be seen that there was no considerable variation in estimation errors among the different DUTs, and this shows that the test order among different DUTs does not affect the test accuracy.

Finally, we changed the resolution of DACs and ADCs, and ran simulations to see how these changes affect the test accuracy. This is important since the resolution of the loopback response is limited by the resolution of data converters and this can affect the test accuracy. We changed the resolution from 10 bits to 14 bits and measured the performance parameters of each DUT. We used a test setup with two DACs and two ADCs to run the simulation. Table I summarizes the mean and standard deviation of prediction errors in various cases. The values in Table I are averaged values across the four DUTs (two ADCs and two DACs). The results indicate that prediction errors are less than 3dB while maximum error occurred when the DAC had 10 bit resolution. It also indicates that the resolution of the DAC is more critical for the accuracy than the resolution of the ADC.

5. Conclusions

In this paper, an efficient parallel test methodology for mixed-signal circuits has been discussed. The algorithm presented in the paper can be used to characterize performance parameters of DUTs accurately using digital test equipment and a DUT loadboard shared among multiple DUTs. A single tone digital sine wave is applied to the DUTs in loopback mode and the resulting digital output response is used to characterize the performance of
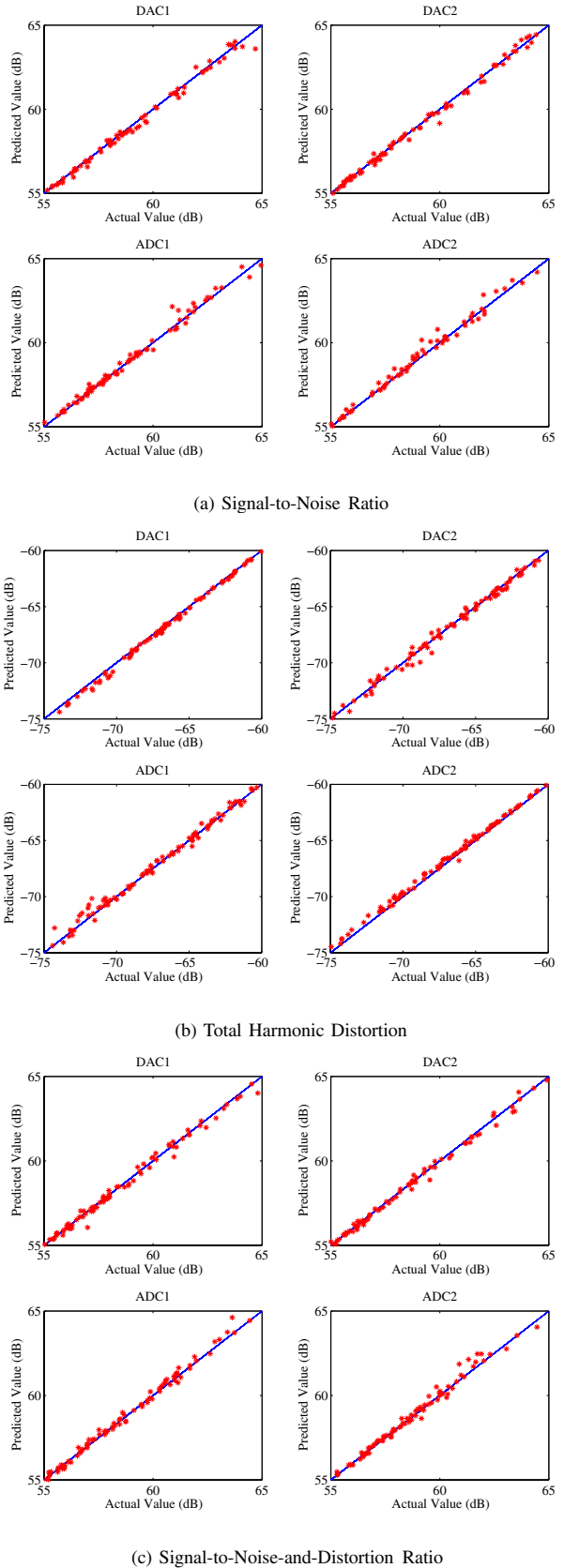

(a) Signal-to-Noise Ratio

(b) Total Harmonic Distortion

(c) Signal-to-Noise-and-Distortion Ratio

Fig. 5. Comparison of Actual and Predicted Performance Parameters

TABLE I. Prediction Error of Parallel Test in Various ADC/DAC Resolution

| Resolution		SNR		THD		SNDR	
ADC	DAC	Mean	STD	Mean	STD	Mean	STD
12bit	14bit	0.35dB	0.73dB	0.34dB	0.50dB	0.16dB	0.20dB
14bit	12bit	0.57dB	0.79dB	0.38dB	0.55dB	0.34dB	0.39dB
12bit	12bit	0.60dB	0.98dB	0.39dB	0.54dB	0.36dB	0.46dB
10bit	14bit	0.30dB	0.55dB	0.45dB	0.70dB	0.19dB	0.28dB
14bit	10bit	0.92dB	1.94dB	0.87dB	1.07dB	0.79dB	1.06dB
10bit	10bit	0.90dB	1.41dB	0.90dB	1.19dB	0.77dB	1.00dB
10bit	12bit	0.51dB	0.61dB	0.35dB	0.38dB	0.29dB	0.27dB
12bit	10bit	1.16dB	1.71dB	0.88dB	0.92dB	0.89dB	1.11dB
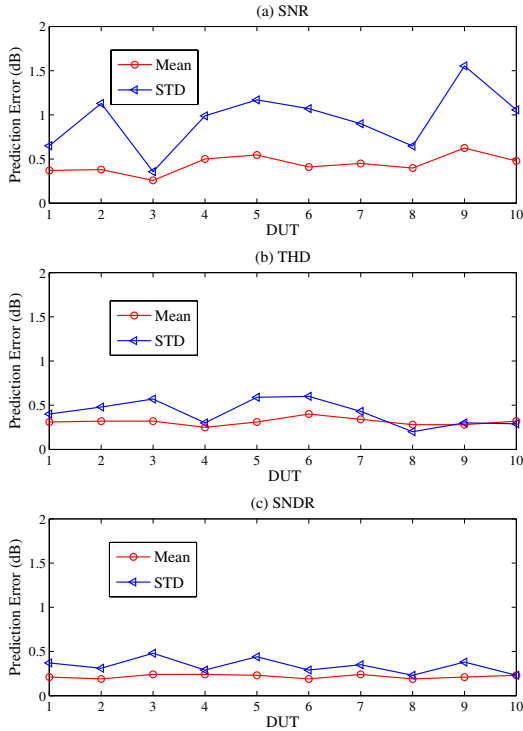
Fig. 6. Prediction Error of Testing 10 DUTs in Parallel

each DUT separately. A DUT loadboard which contains a simple analog adder and an RMS detector is used to estimate the performance parameters of the multiple DUTs accurately without being affected by fault masking. Our algorithm does not depend on the type of circuit being tested, and can thus be applied to general mixed-signal circuits to help reduce the test cost and time. Mathematical derivations and simulation results show the validity of the proposed algorithm.

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