11.1 A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography

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Intracardiac echocardiography (ICE) is an ultrasound sonogram that visualizes the anatomical structure of the heart in real time, with a mm-scale catheter inserted through the intracardiac vessels, and guides surgical intervention for atrial septal defect (ASD) closure. To achieve high-quality medical imaging, an ICE system must meet stringent power consumption requirements with low-noise operation. Since an ASIC and ultrasound transducers are tightly bonded through flip-chip or direct integration, an ultrasound unit TRX channel must be pitch-matched to each transducer channel [1,2]. A piezoelectric Micromachined Ultrasound Transducer (pMUT) is a suitable ultrasound transducer for implantable sensor applications, since it does not need high (~200V) bias that is a must in capacitive MUTs (cMUT) [3]. However, pMUT devices suffer from process variation, which leads to low image quality, and to date, no work addresses this issue for both TX/RX in real time. To meet all these requirements at once, we present a 6×6 TRX pitch-matched pMUT ASIC with a standard CMOS-compatible 13.2V HV pulser, on-chip per-pixel calibration scheme, and a Dynamic Bit-Shared (DBS) ADC for portable ICE applications.

Figure 11.1.1 shows the proposed ICE system. The catheter is 1.5m in length and 3mm in diameter; it integrates a 2D 6×6 5MHz 250μm-pitch pMUT array [3] and a pitch-matched 6×6 TRX ASIC in the tip. To ensure signal integrity even with a long wire, an on-chip DBS ADC digitizes the results on each channel prior to being transmitted. To prevent any tissue damage from overheating, low power consumption is a must, which also opens the door to further implantable ultrasound imaging systems.

Figure 11.1.2 shows the ASIC architecture. It consists of a 36-channel ultrasound TRX, a digital controller, a calibration block, a PMU, and a PLL. The unit ultrasound TRX channel is composed of a Charge-Recycling HV (CRHV) pulser, a TX/RX switch, an LNA, a time-gain compensation (TGC) amplifier, an analog delay cell, and a 10b SAR ADC. In order to reduce power consumption and compensate for pMUT process variation (aberration), 3 key features are proposed: (1) standard CMOS-compatible CRHV pulser, (2) a 4-channel 10b DBS SAR ADC, and (3) a large-dynamic-range TGC amplifier with automatic *per-pixel* calibration. An on-chip aberration compensation block is integrated into the calibration block to compensate for phase inequalities due to unsymmetrical geometry and velocity distribution of the pMUT array [4]. Moreover, the Received Signal Strength Indicator (RSSI) dynamically adapts the TGC gain depending on its input signal magnitude.

Figure 11.1.3 shows a schematic diagram of the CRHV pulser, along with its cross-sectional view. Previous works adopt HV process technology to facilitate HV operation, which increases the process cost, occupies a bulkier physical area with additional parasitic components, and most importantly, is not compatible with the most advanced process nodes [5]. In contrast, the CRHV pulser is fully compatible with standard CMOS, where the stacked I/O transistors always operate within its normal operation voltage range. By stacking M_1-M_6 transistors with staggered well potentials, stress to each transistor is dispersed, thereby compatible with standard CMOS process. The CRHV pulser operates in 2 phases: In the charging phase, the pMUT's outer and inner electrodes are connected to V_{HIGH} and ground, respectively. In the redistribution phase, the outer and the inner electrodes are shorted, re-using theoretically half the charge from the previous phase; this reduces the TX power, which dominates the unit TRX channel power consumption, by 32.8%. pMUTs inherently suffer from mismatch, and their acoustic pressure varies even with an identical excitation voltage, resulting in aberration [4]. To equalize the TX acoustic pressures, the gate voltage of M_1 and M_6 are controlled by the DAC with a 3b digital code, resulting in the real-time *per-pixel* calibration of TX channels by up to $3.3V_{pp}$. As a result, the standard variation of pulse-to-echo (P2E) maximum amplitude is reduced from 0.0304 to 0.0037, corresponding to an 87.8% reduction in aberration (Fig. 11.1.3).

Noting that the majority (~90%) of power dissipation in the RX path comes from the ADC, we propose a DBS SAR ADC (Fig. 11.1.4) to save power. As adjacent ultrasound pixels receive similar echo results with phase delay, they share a coarse ADC after subarray delaying. The 10b DBS SAR ADC shares 0/2/4/6 MSB with adjacent 2×2 channels; the coarse ADC pre-defines the switch polarity of the fine ADC, therefore there is a greater reduction in power consumption as more bits are shared. The analog delay cells perform subarray beamforming with 5ns resolution, and the remaining delay difference <5ns between channels changes the number of sharable bits of the coarse ADC by inverse proportion. The SNDR is measured to be 56.85dB with 9.15b ENOB. The DBS-ADC consumes 0.85mW with 6 shared coarse bits (vs. 1.23mW without bit-sharing), where up to 30.9% power reduction can be achieved.

Figure 11.1.5 shows the circuit schematic for closed-loop RX path with attenuation-adaptive gain/noise control. The RSSI is composed of 10 amplifier-rectifier (AR) cells and 9 bias filters. It measures the magnitude of input signals in a log scale to control the gain and noise [6]. The required dynamic range of the RX is 90dB to penetrate 4cm in human body The signal attenuation is roughly 40dB as the acoustic signal penetrates the body with an attenuation rate of 1dB/cm/MHz and the minimum display resolution is 50dB. As 90dB dynamic range is power consuming for the RX path, the TGC adaptively changes its gain and noise based on the signal magnitude measured by the RSSI. The RSSI can measure an input signal from -105dBm to -35dBm logarithmically and consumes 0.66mW; the RSSI is shared throughout 36 channels.

Figure 11.1.6 shows the B-mode image result of a phantom and the comparison table with other recent ultrasound ASIC works. An imaging phantom is constructed with polydimethylsiloxane (PDMS), where 3 wires are inserted inside. The phantom is placed on the top of the transducer array, and three wires are located 25mm, 28mm, and 35mm above from the bottom. The 36-channel pMUTs insonify 5MHz ultrasound pulse with $5V_{pp}$ to the phantom, and pulse-to-echo signals are recorded from -30° to +30° beam steering angle with 5° spacing. The recorded digital RX data shows clear echo signals when the beam is steered towards the wire. A B-mode imaging in the lateral direction with 60° field of view shows the presence and the position of the 3 wires in the phantom.

Figure 11.1.7 shows the chip micrograph and the performance summary. The ASIC in standard 180nm 1P6M CMOS occupies $11.75mm^2$ area, and TX consumes 3.31mW and 9.26mV for $5V_{pp}$ and $13.2V_{pp}$ mode, respectively. With the DBS ADC, ADC and RX power consumption are reduced by 30.9%, 28.6%, respectively, which is only 0.95mW per channel. The automatic calibrated TGC with RSSI adapts its gain and noise corresponding to its input signal magnitude. Compared to the previous ultrasound systems shown in the comparison table (Fig. 11.1.6), the proposed ultrasound ASIC achieves the highest integration scale which integrates *all* TX, RX, and ADC into $250×250μm^2$ unit channel, and the lowest power consumption (5.37mW with $5V_{pp}$ TX), which effectively prevents the tissue overheating.

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References:

[1] M. Chen, et al., "A Pixel-Pitch-Matched Ultrasound Receiver for 3D Photoacoustic Imaging with Integrated Delta-Sigma Beamformer in 28nm UTBB FDSOI," *ISSCC Dig. Tech. Papers*, pp. 456-457, Feb. 2017.
[2] C. Chen, et al., "A 0.91mW/element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes," *ISSCC Dig. Tech. Papers*, pp. 186-187, Feb. 2017.
[3] B.E. Eovino, et al., "Broadband Ring-Shaped pMUTS Based on an Acoustically Induced Resonance," *IEEE MEMS*, pp. 1184-1187, Jan. 2017.
[4] J. Tillak, et al., "A 2.34μJ/scan Acoustic Power Scalable Charge-Redistribution pMUT Interface System with On-Chip Aberration Compensation for Portable Ultrasonic Applications," *IEEE ASSCC*, pp. 189-192, Nov. 2016.
[5] G. Jung, et al., "Single-Chip Reduced-Wire Active Catheter System with Programmable Transmit Beamforming and Receive Time-Division Multiplexing for Intracardiac Echocardiography," *ISSCC Dig. Tech. Papers*, pp. 188-189, Feb. 2018
[6] J. Jang, et al., "A 540μW Duty Controlled RSSI with Current Reusing Technique for Human Body Communication," *IEEE TBioCAS*, vol. 10, no. 4, pp. 893-901, Aug. 2016.

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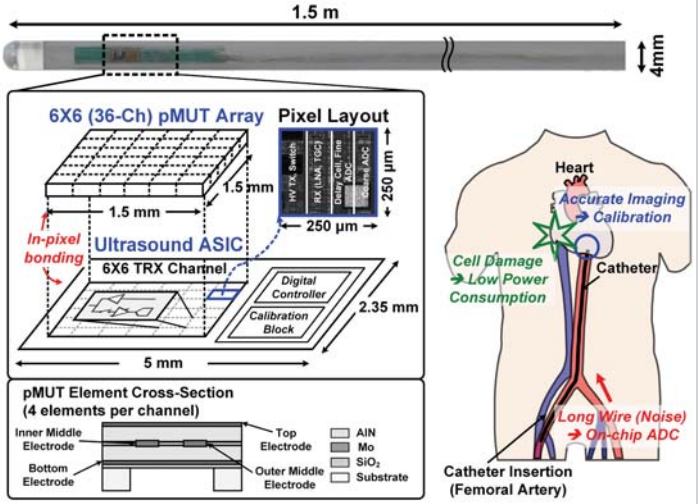


Figure 11.1.1: Proposed intracardiac echocardiography (ICE) system.

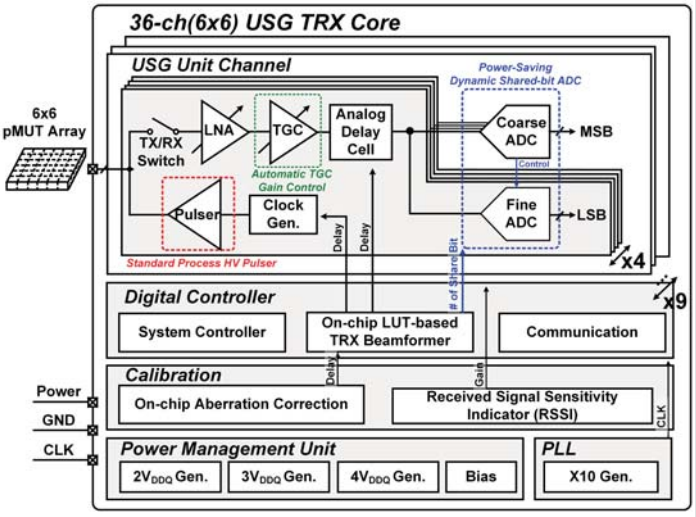


Figure 11.1.2: Overall architecture of ICE ASIC.

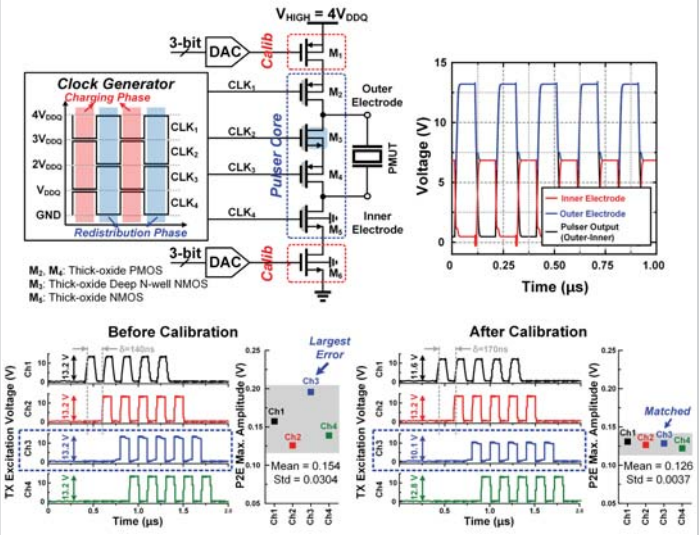


Figure 11.1.3: $4V_{DDQ}$ Charge Recycling High Voltage (CRHV) pulser with standard CMOS process.

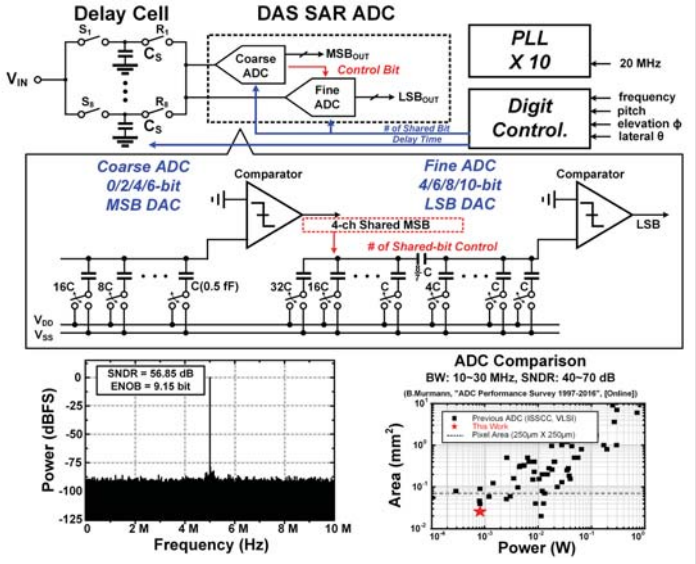


Figure 11.1.4: Power saving 4-channel Dynamic Bit-Shared (DBS) SAR ADC.

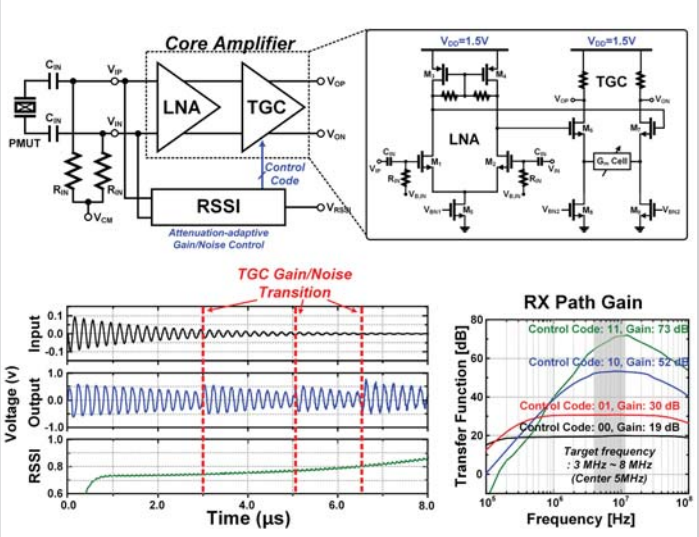
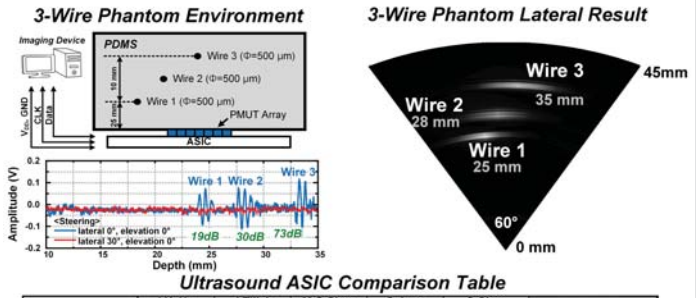


Figure 11.1.5: 90-dB dynamic range RX with attenuation-adaptive gain/noise calibration.

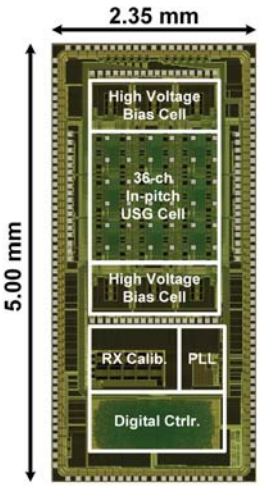


Ultrasound ASIC Comparison Table

	J.Y. Um ISSCC'14	J.Tillak ASSCC'15	M.C.Chen JSSC'17	G.Jung ISSCC'18	C.Chen ISSCC'18	This Work
Process	0.13 µm	65 nm	28 nm	0.18 µm HV	0.18 µm	0.18 µm
Transducer	2D CMUT	PMUT	2D CMUT	PZT / CMUT	2D PZT	2D PMUT
Pitch-Matched	No	No	Yes (250 µm)	No	Yes (150 µm)	Yes (250 µm) *
TX/RX per ch.	Only RX	TX / RX	Only RX	TX / RX	RX	TX / RX
ADC per ch.	X	X	O	X	X (1ADC/4ch)	O
Area/ch.	0.303 mm²	0.13 mm²	0.0625 mm²	0.45 mm²	0.026 mm²	0.0625 mm²
Max. TX Voltage	-	6 V	-	60 V	-	13.2 V
TX Power/ch.	-	N/A	-	N/A	-	3.31 mW ($5V_{pp}$) 9.26 mW ($13.2V_{pp}$)
RX Power/ch.	17.81 mW	N/A	17.5 mW	N/A	0.91 mW	0.95mW **
Total Power/ch.	17.81 mW	N/A	17.5 mW	6.26 mW	0.91 mW	5.37 mW (TX $5V_{pp}$) 10.33 mW (TX $13.2V_{pp}$)
TRX BF	RX	TX	RX	TX	RX	TX / RX
TRX On-chip Cal.	No	Yes	No	No	No	Yes

*This work is the *only* ASIC which integrated both TX & RX in a pitch-matched channel **6 shared coarse bit

Figure 11.1.6: B-mode imaging result of 3-wire phantom and ultrasound system comparison table.



Process			180 nm 1P6M Standard CMOS
Die Size			2.35 x 5.0 mm^2
Supply Voltage			1.5 V
Transducer			2D PMUT
TX		Frequency	1/2/5/10 MHz
		Power	3.31 mW ($5V_{pp}$)
			9.26 mW ($13.2V_{pp}$)
		Amplitude	Max. 13.2 V_{pp}
RX	LNA+ TGC	Gain	29 / 30 / 42 / 53 dB
		BW	3 ~ 13 MHz
		Power	82.2 µW
	Delay Cell	Delay min.	5 ns
		Delay max.	1.28 µs
	ADC	Sampling Rate	20 MHz
		SNDR	56.85 dB
		Power	0.85 mW (6-bit shared)
			1.23 mW (0-bit shared)
	RSSI	Dynamic Range	-105 ~ -35 dBm
		Power	0.66 mW
Digital Controller		Frequency	20 MHz / 200 MHz
		Power	4.38 mW

Figure 11.1.7: Chip micrograph and ASIC performance summary.

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