Through-Silicon Via and Die Stacking Technologies for Microsystems-integration

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Introduction

The highest integration density of microsystems can be obtained using a 3D-stacking approach, where each layer of the stack is realized using a different technology, which may include sensors, imagers, rf and MEMS technologies. A key challenge is however to perform such stacking in a cost-effective manner. In this paper, a novel 3D TSV and 3D stacking technologies will be presented. Application examples are MEMS packaging and heterogeneous integration of imaging devices.

3D-Heterogeneous Microsystems packaging approach

The growing technological capability of silicon 3D-integration technologies are of high interest to the heterogeneous integration of microsystems.[1-3] In particular the development of micro-bump technologies for fine pitch face-to-face bonding of die and the possibility of realizing electrical through-Si via connections are of key importance. A first application combines devices that consist of a large pixel array, directly bonded with a fine pitch bumping technology to a Si device. This device is part of a larger array of modules that cover a larger area. Therefore the actual CMOS device is somewhat smaller than the detector array and through Si-via connections are used to electrically connect the module:

A second application field is the integration and packaging of MEMS devices, as shown in fig. 1. Most MEMS devices are characterized by a fragile surface after fabrication that requires hermetic encapsulation. This can be achieved effectively by bonding a capping the fragile MEMS devices at the wafer level, immediately after finalizing the MEMS fabrication.[4-5] Both Die-to-Wafer and Wafer-to-Wafer bonding can be used. Hermetic sealing is performed using metallic micro bump connections, discussed in more detail in the next section. The resulting wafer stack has no external connections at this point. The micro-bump joining technique allow for simultaneous realization of hermetic sealing rings as electrical cap-to-MEMS point bumps connections (micro-bump connections). This enables the use of an "active" capping wafer, e.g.; integrating driver electronics or passive circuit elements

Traditional MEMS packaging technology would consist of dicing or etching the capping wafer in such a manner as to reveal the bonding pads on the MEMS-wafer, surrounding the capped area. This requires the generally small MEMS device to be considerably larger than required by its function (e.g.: adding 200 μm space to the perimeter of a 1x1 device, increases the effective device area by 100%).

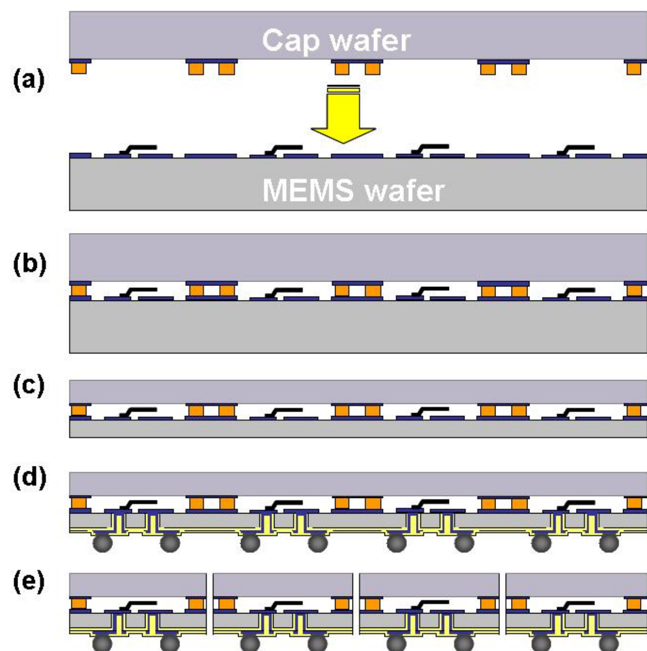


Figure 1: Schematic representation of a 3D-MEMS packaging solution. The MEMS devices are first capped by a wafer-to-wafer bonding process, creating hermetic cavities and electrical connections.(a and b) In a next step, One or both wafers are thinned by back grinding (c) and through-Si vias and redistribution interconnect technology are realized (d). Finally the MEMS devices are separated by dicing (e).

A more effective solution, as shown schematically in fig. 1, is to realize the electrical connections using through-Si via, TSV, technology. This typically requires the capping or MEMS wafer to be thinned first to enable a cost-effective 3D-TSV process. The technology used for this 3D-TSV is described in more detail below.

Finally, after finalizing the capping and the 3D-TSV connections, solder balls may be added to the wafer stack and the wafer may be diced in individual components. For small die devices with a low number of connections;, these solder balls may relatively large, in the order of 200-300µm, effectively realizing a wafer-level chip-sized package (WL-CSP) that does not require any further packaging steps. This results in a very compact MEMS component, which reduces the cost of the device and enhances the reliability of assembled devices.

Microbump interconnect technology

Traditional flip-chip interconnects use spherical solder joints. When scaling down the size of the solder balls, the intermetallic compounds formed between the solder and the pad metallization become dominant. An alternative approach is to deposit metal pad layers covered with relatively thin solder joints (fig. 2).

These structures may take the shape of metal pillars or rings. Such ring shapes may be used to create hermetic enclosures for MEMS devices. Simultaneous bump and ring connections may be realized. An example of a MEMS-capping test structure is shown in fig. 3. In this case two 150 mm wafers were bonded, forming a variety of bonded cavities. After dicing the wafers and performing leak testing, an excellent yield of the bonding process was observed.

In order to obtain a high interconnect reliability and bonding yield, an excellent control of the height of the metal seal structures is required. Such control is difficult using electroplating technologies a feature size and proximity effects limit the achievable height control across wafers to some 5%. It is therefore recommended to perform a planarization process of the microbumps after plating. A novel technique consists of high precision diamond cutting (milling) of the wafer to planarize the structures.[6] This technique also allows creating very flat Cu surfaces that can be used to bond die or wafers using Cu-Cu thermo-compression at lower temperatures, down to 250°C. Examples of such Cu-Cu thermo compression joints are shown in fig. 4.

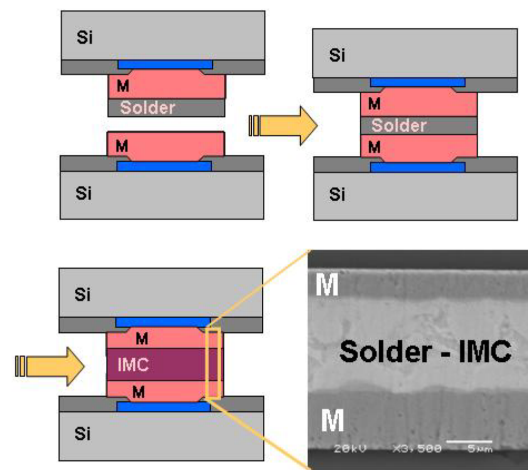
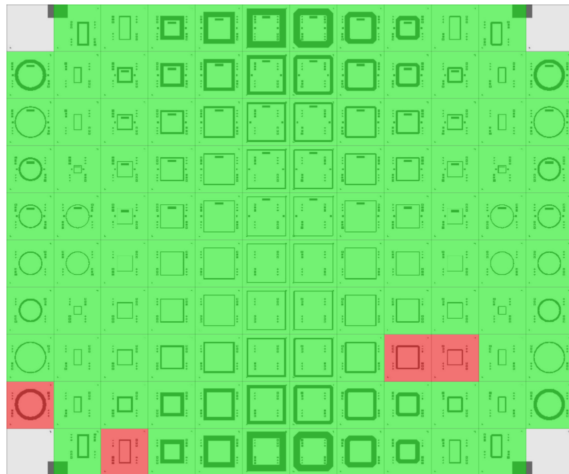


Figure 2: Principle Microbump, Transient liquid phase, solder connection.



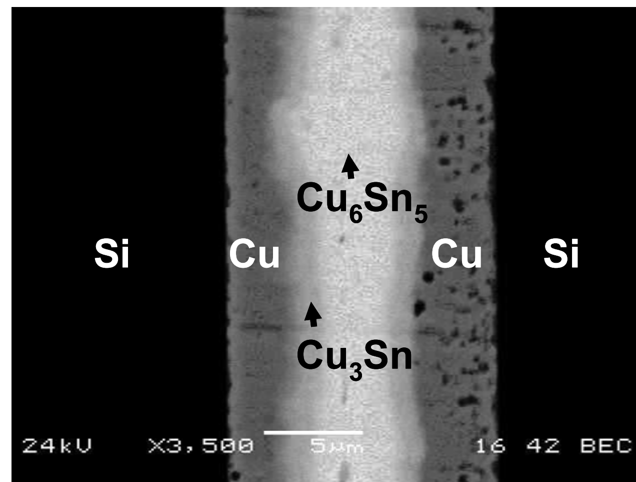


Figure 3: 150 mm wafer-level MEMS capping experiment. The test pattern consists of a variety of cavities metal seal rings with widths ranging from 50µm to 800µm and diameters from 1mm to 5mm. On both wafers, 5µm thick Cu rings capped with a 3µm Sn layer were applied by electroplating. The two wafers were bonded using an EVG IQ aligner and an EVG 520 bonder. During bonding, a pressure of 4.62MPa was applied for 20 minutes at 260°C. After processing the wafer was diced in individual units that were subjected to leak testing. A high yield of 96,5 % was obtained (green in figure). A shear strength of min. 400 KgF/cm2 was obtained. On the left, a typical cross-section of the structure is shown, illustrating the complete transformation of the Sn-layers into CuSn intermetallic compound

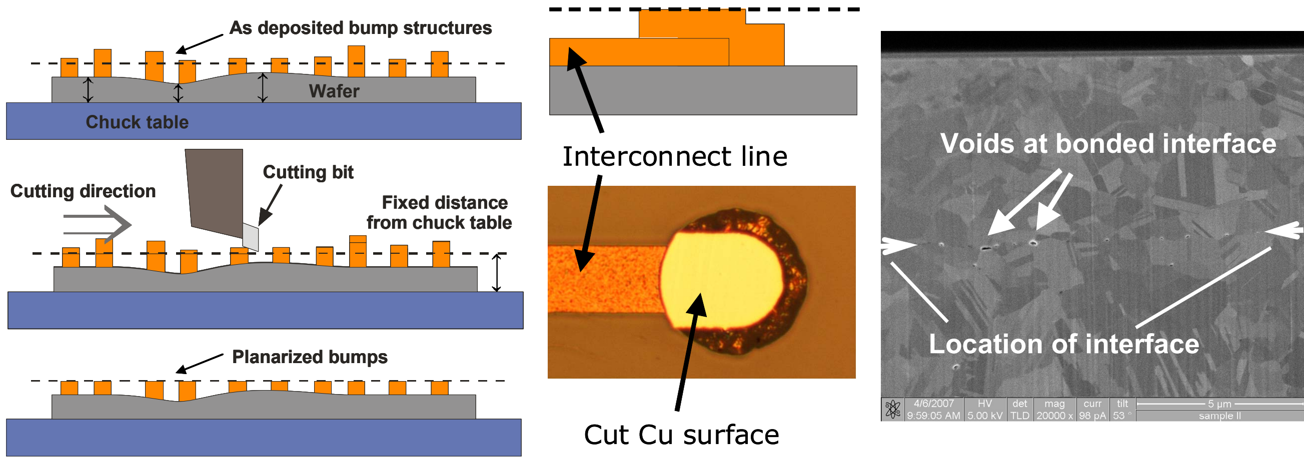


Figure 4: Principle of diamond bit cutting for planarizing metallic layers. Example of of Cu bumps, (Roughness after planarization Ra ~ 9nm / Rz ~ 50nm). This allows for effective Cu-Cu thermocompression bonding at 250°C (right SEM cross-section view.

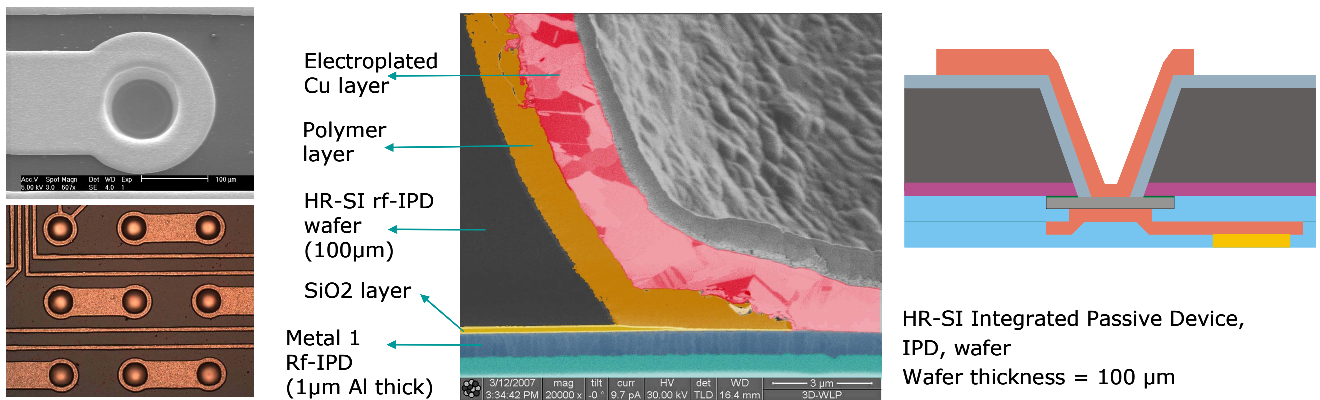


Figure 5: Through Si-via technology for relatively large via diameters and larger Si-wafer thickness, using a conformal polymer and metal coating of the low aspect ratio 1:1 via.

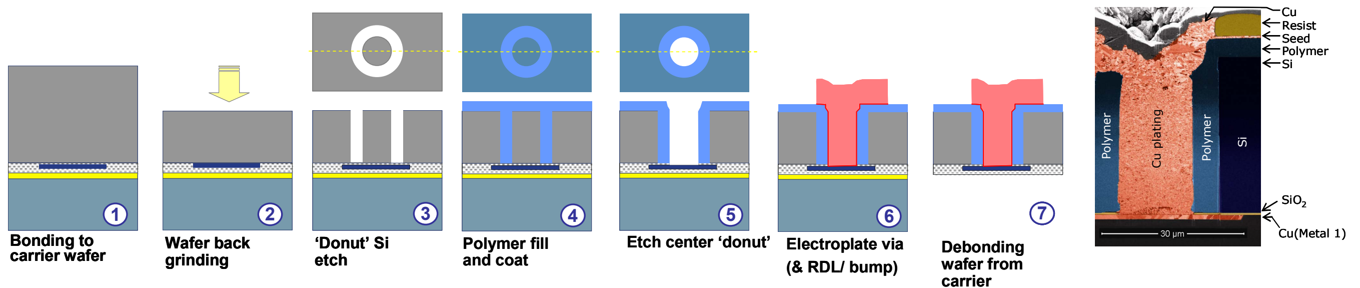


Figure 6: Through Si-via technology for small via diameters and small Si thickness, using an annular ring polymer isolation layer and a fully filled Cu via

Through Si-via technology

The Through Si via technology proposed here uses a via-last approach. The TSV process is performed after back grinding the Si and realizes a contact to the bottom layer of the device stack. Two different process flows are shown in fig. 5 and 6. A specific aspect of the proposed flow is the use of a polymer as a dielectric layer between the TSV metal and the Silicon allowing for low mechanical stress and low parasitic capacitance of the TSV structure. The dimensions of these TSV's are compatible with the IC bond-pad scaling roadmaps.

In order to have a cost effective process for these TSV structures, a low AR has to be maintained, typically 2-3.[7] For large diameter TSV structures in thick Si wafers, plating times for fully filled TSV's may approach 3 hours per wafer, resulting in an uneconomical process. In that case, it is preferable to use a conformal Cu-plating in an open TSV structure as shown in figure 5.[7] In this case the Cu-plating time can be reduced to a few minutes.

This conformal Cu-TSV is however not scalable to very tight interconnect pitches. For the higher density 3D-WLP TSV structures, a fully filled TSV structure is required. The IMEC approach to a 3D-WLP fully filled Cu-TSV is shown schematically in figure 6. First the wafers are bonded to a temporary carrier wafer, followed by wafer thinning down to 50 µm. The next step is to etch a circular trench, "donut", in the Si, stopping at the front side oxide layer. This circular trench is about 5 µm in width. This circular trench is filled with a polymer dielectric using a spin-coating technique. The polymer layer is opened on top of the Si-center of the (polymer) donut. This allows for the selective (wet or dry) etching of the central Si pillar and the back-etching of the oxide at the bottom of the hole, exposing the metal contact pad. The final steps are the PVD deposition of a barrier and Cu seed layer, followed by the electroplating of the Cu via. An important advantage over the sloped via process is that no lithography at the bottom of the via is required

Conclusion

3D integration technologies, in particular wafer-to-wafer bonding using metallic seals and through-Si wafer via technology offer a cost-effective solution to MEMS-packaging by addressing the packaging issues at the wafer level and minimizing the area overhead for packaging.

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