13.2 A 3.7mW-RX 4.4mW-TX Fully Integrated Bluetooth Low-Energy/IEEE802.15.4/Proprietary SoC with an ADPLL-Based Fast Frequency Offset Compensation in 40nm CMOS

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This paper presents an ultra-low-power (ULP) fully-integrated Bluetooth Low-Energy(BLE)/IEEE802.15.4/proprietary RF SoC for Internet-of-Things applications. Ubiquitous wireless sensors connected through cellular devices are becoming widely used in everyday life. A ULP RF transceiver [1-3] is one of the most critical components that enables these emerging applications, as it can consume up to 90% of total battery energy. Furthermore, a low-cost radio design with an area-efficient fully integrated RF SoC is an important catalyst for developing such applications. By employing a low-voltage digital-intensive architecture, the presented SoC is fully compliant with BLE and IEEE802.15.4 PHY/Data-link requirements and achieves state-of-the-art power consumption of 3.7mW for RX and 4.4mW for TX.

Figure 13.2.1 shows the architecture of the RF SoC. An all-digital TX consists of a sub-mW snapshot-TDC all-digital PLL (ADPLL) [4] and an energy-efficient Class-D PA. A sliding-IF RX is adopted because it does not require a power-hungry LO generation. The PA with partial on-chip impedance matching and the LNA are both single-ended, which reduce external components and simplify the antenna interface design. A multistandard DBB [5] includes all PHY processing and data link for BLE and IEEE802.15.4. In this work the DBB further includes optimized HW/SW register interfaces and HW accelerators for protocol support, and implements an AHB/APB interface to facilitate integration with an ARM Cortex™-M0 MCU and 128kB SRAM.

One of the most challenging parts of the BLE RX mode is to receive the packets with an extremely short 8b preamble, which requires fast automatic gain control (AGC) and carrier-frequency offset (CFO) compensation method. A two-step AGC algorithm performs only coarse gain tuning in the RF parts (i.e., LNA and mixers) during the preamble with 12dB/step, allowing the RX output amplitude to quickly settle within the ADC dynamic range in just a few symbol periods. The fine amplitude tuning is performed in the LPF/PGA during the access code period with 3dB/step. Furthermore, BLE also specifies that the RX should accommodate a "dirty TX" with a large CFO up to ±100kHz (±41ppm). The CFO could be post-compensated in the DBB with a phase rotator, but then the LPF BW needs to be at least 100kHz wider, which compromises the adjacent channel rejection. In this work, a mixed-mode CFO compensation through an ADPLL allows direct compensation in the analog domain without increasing LPF BW. The CFO is first estimated by the DBB based solely on a part of the packet's preamble. The CFO estimation unit employs a 17-tap FIR filter with low latency. The CFO is detected by converting the IQ data to phase difference, and averaging it across preamble symbols. The CFO is then compensated by directly adjusting the fractional-N ADPLL with a frequency resolution of 1kHz. However, PLLs typically have a slow settling in the order of 20µs, which is not fast enough to compensate the CFO within the preamble. Therefore, the 2-point injection technique employed in the TX mode for wideband modulation is reused in the RX mode as the fast CFO compensation path without increasing power consumption. The slow frequency response of the ADPLL is equalized by feed-forwarding the 10b compensation data, Δf, to the DCO (Fig. 13.2.2).

In comparison to a conventional analog PLL [1-3], ADPLLs are preferred in low-cost low-power radio as they offer benefits of smaller area, programmability, capability of extensive self-calibrations. This reduces the PLL chip area more than 50%, i.e., from 0.5mm^2 to 0.2mm^2, and eliminates the leakage issue of the analog loop filter in 40nm CMOS. The internal signals of the ADPLL can be directly read out, allowing extensive calibrations to be deployed to improve the stability over PVT, e.g., the 2nd-point gain can be calibrated by directly reading the DCO tuning word. Moreover, the ADPLL parameters can be widely programmed to support different phase noise or settling-speed requirements. The initial TX frequency perturbation, due to the PA start-up, disturbs the RX packet reception especially with short preamble. BLE specifies that the average frequency drift of the preamble should be lower than 20kHz. Hence, when the ADPLL is operating in TX mode, a higher loop BW is used to quickly recover from the PA pulling, whereas a lower loop BW is set in RX mode to fulfill the phase noise requirement for interference rejection.

To maximize the power efficiency of RF transceivers in ULP applications, they are designed to directly attach to a small battery, e.g., 1.3V Zinc-air, without using power converters. The transceivers thus must sustain supply voltages below 1V and have low leakage current to maximize the life time. On the other hand, the threshold voltage of the 40nm MOS devices increases to as high as 500mV, making the conventional current-biased circuits difficult to operate at such low supply voltage. Therefore, as shown in Fig. 13.2.3, digital-style inverter-based circuits are widely used in the analog baseband and LO chain. In addition, the DCO replaces a current tail with a resistor bias and an amplitude calibration loop for low-voltage operation. A start-up circuit is added in OP-Amps to guarantee that the common-mode feedback still functions below 1V. A clock booster is adopted in the ADC sample-and-hold to raise the clock voltage, so the linearity of the sampling switch can achieve the targeted 9b dynamic range. The RF front-end still maintains key functionalities and performance at 0.9V. The leakage current is minimized by implementing extensive power gating (measured 1.5µW).

The digital-intensive RF design reduces the analog core area to 1.3mm^2. Figure 13.2.4 shows the RX measurement results with the proposed fast AGC and CFO compensation. The RX sensitivity of [1] was measured with previous BLE definition (continuous BER of 0.1%) which doesn't take into account the short preamble effect. In this work, the RX measurement follows the latest BLE definition, i.e., packet error rate (PER) of 30.8%, and it achieves a sensitivity of -94dBm. The RX with fast AGC has a dynamic range from the sensitivity level up to -5dBm, and fulfills BLE interference and block rejection requirement with sufficient margin. The proposed fast CFO compensation extends the CFO tolerance from ±50kHz in the previous work [1] to ±150kHz (BLE spec.: ±100kHz). The RX also fulfills all IEEE802.15.4 requirements and has a sensitivity of -97dBm. Figure 13.2.5 shows the measured transient of the demodulated TX frequency and the BLE burst modulation quality. With a higher PLL BW in TX mode, the frequency perturbation due to the PA pulling can be settled to 20kHz in 12µs. The TX has a modulation quality of 5% (BLE) and 2% (802.15.4). The PA delivers -2dBm power, and the 2nd and 3rd harmonics are -49dBm and -53dBm, respectively, which are both below FCC emission regulation. Figure 13.2.6 benchmarks with state-of-the-art BLE transceivers [1-3] and off-the-shelf SoCs. Figure 13.2.7 shows the die micrograph. By employing a digital-intensive RF architecture and fully utilizing the calculation power of the tightly integrated DBB and MCU, the presented SoC in 40nm is fully compliant with BLE/IEEE802.15.4 and further reduces the supply voltage (20%), power consumption (25%), and chip area (35%) compared to the previous 90nm RF front-end design [1].

Acknowledgement:
The authors would like to thank E. Wouters from IMEC Services for the back-end support.

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 978-1-4799-6224-2/15/$31.00

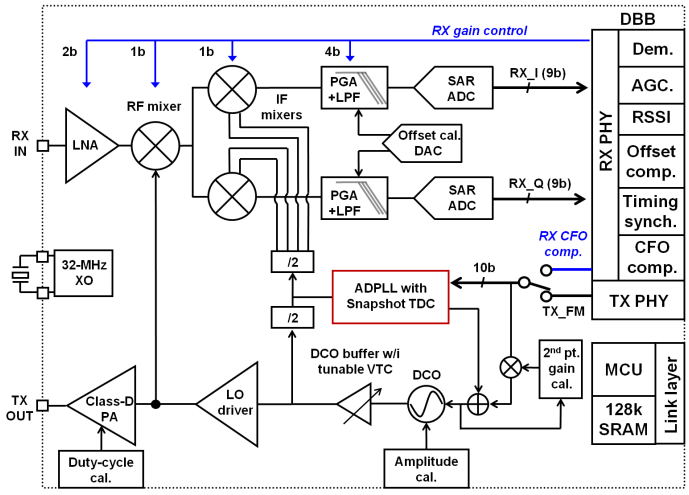

Figure 13.2.1: Simplified block diagram of the BLE RF SoC.

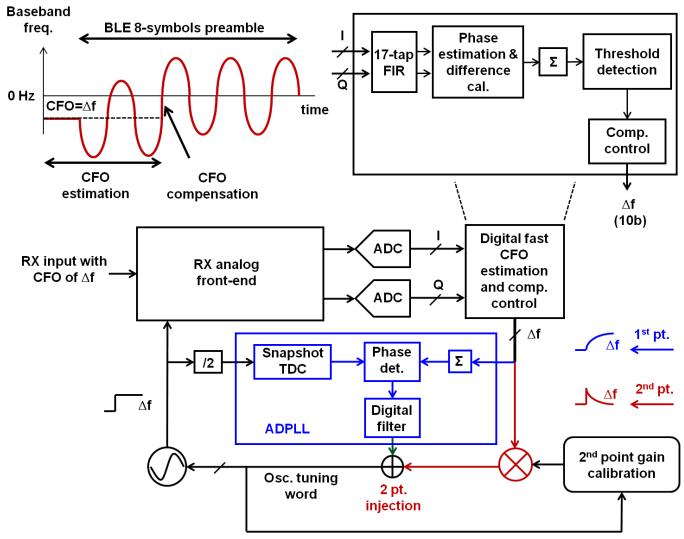

Figure 13.2.2: The block diagram and the conceptual illustration of the proposed fast CFO compensation through a 2-point injection ADPLL.

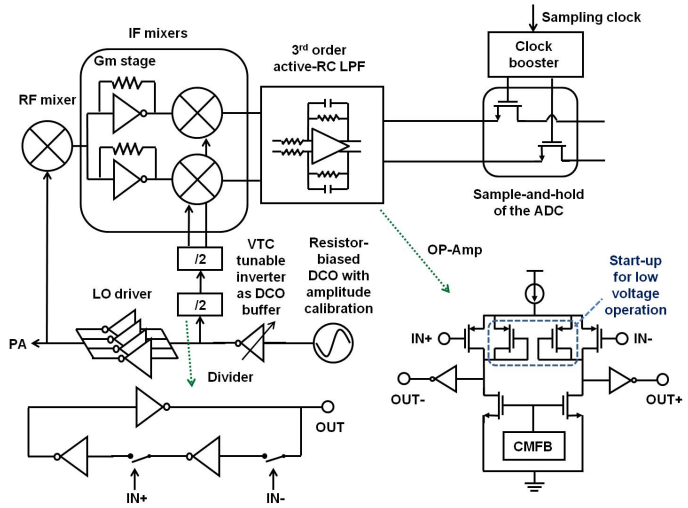

Figure 13.2.3: Simplified block diagram and schematic of the sub-1V RX ABB and LO generation.

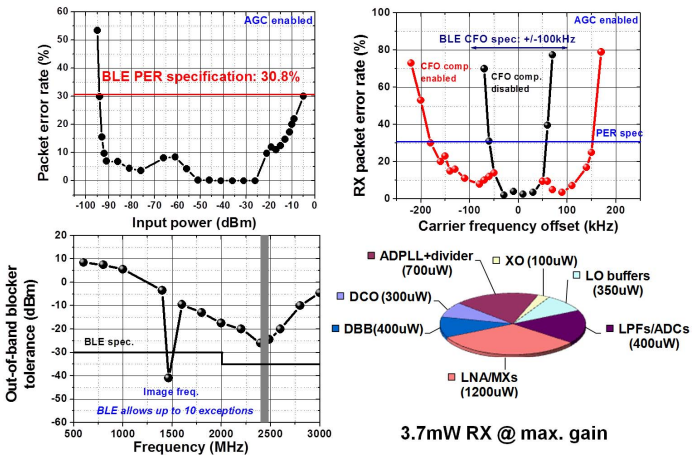

Figure 13.2.4: Measured RX dynamic range, CFO and blocker tolerance, and power breakdown at 1V in BLE mode.

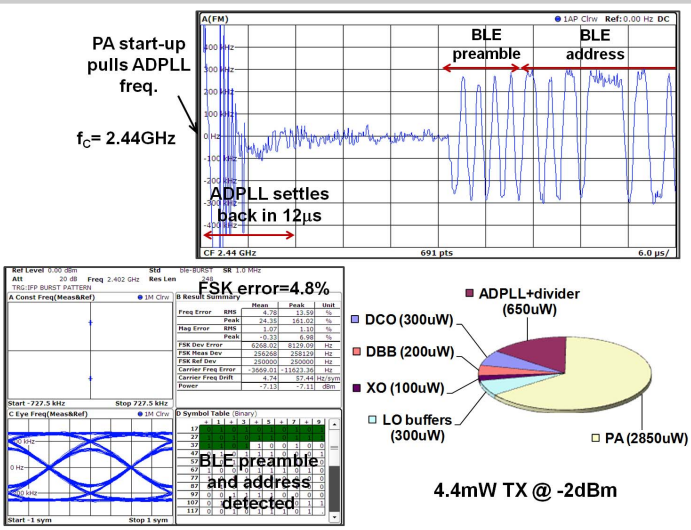

Figure 13.2.5: Measured TX frequency after demodulation, burst-mode modulation quality and power breakdown at 1V in BLE mode.

	This work	[1] ISSCC'13	[2] ISSCC'12	[3] RFIC'13	Nordic nRF51822	Dialog DA14580
Standards	BLE 4.1 802.15.4 2M propriet.	BLE4.0 802.15.4 802.15.6 2M popriet.	BLE4.0 802.15.6	BLE4.0 802.15.4 4M Propriet.	BLE4.1 Propriet.	BLE4.1
Technology	40nm	90nm	65nm	90nm	N.A.	N.A.
Integration level	RF/DBB/ MCU SoC	RF only	RF only	RF+DBB	RF/DBB/ MCU SoC	RF/DBB/ MCU SoC
RX BLE sensitivity	-94dBm*	-98dBm	-94dBm	-94.5dB	-93dBm*	-93dBm*
RX BLE ACR(1/2/3MHz)	-4/-25/-35dB	-4/-26/36dB	N.A.	N.A.	1/-25/-50dB	-3/-20/-30dB
RX BLE CFO tolerance	±**150kHz**	±50kHz	N.A.	N.A.	N.A.	N.A.
TX max. P_{OUT}	-2dBm/1dBm**	0dBm	5dBm	4dBm	4dBm	0dBm
PLL settling time	15µs	40µs	N.A.	5µs~15µs	N.A.	N.A.
Supply voltage (Typ.)	1V	1.2V	1V/1.5V PA	1.2V	3V	3V
Analog chip area	1.3mm^2	2mm^2	N.A.	N.A.	N.A.	N.A.
Power dissipation ***						
DBB (TX/RX)	0.2/0.4mW	No DBB	No DBB	N.A.	N.A.	N.A.
TX	**4.2mW**	5.4mW	9mW	10.5mW	31mW	10mW
RX	**3.3mW**	3.8mW	6.5mW	8.2mW	39mW	11mW

*Measured according to the latest BLE test specification (RF-PHY.TS/4.0.1) with 30.8% PER.
The RXs in [1-3] were measured with the previous V4.0 definition of 0.1% bit error rate (BER).
** -2dBm is with partial on-chip matching; 1dBm is with off-chip matching.
*** DBB is included, but MCU/SRAM is not included as it is application dependent.

Figure 13.2.6: Performance summaries and comparison with the state-of-the-art low-power BLE transceivers and SoCs.

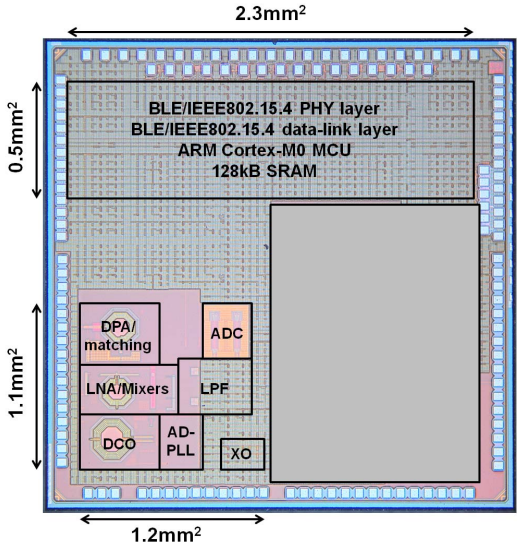

Figure 13.2.7: Die Micrograph.

978-1-4799-6224-2/15/$31.00