A 0.12mm^2 7.4μW Micropower Temperature Sensor with an Inaccuracy of ±0.2°C (3σ) from -30°C to 125°C

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***Abstract*— A temperature sensor intended for RFID applications has been realized in a 0.16μm standard CMOS process. After a single digital trim at 30°C, it achieves an inaccuracy of ±0.2°C (3σ) over the temperature range: –30°C to 125°C. At a conversion rate of 10Hz, it achieves a resolution of 15mK. The sensor is compact, occupying only 0.12mm^2, and power efficient, drawing 4.6μA from a 1.6V to 2V supply, which corresponds to a minimum power dissipation of 7.4μW, the lowest ever reported for a precision temperature sensor.**

I. Introduction

Energy efficiency and low-power operation are key requirements of battery powered systems such as wireless sensor nodes and radio frequency identification (RFID) tags. Adding temperature sensors to such systems will open up new applications in the medical, industrial, automotive and consumer fields. Such sensors, however, must be both accurate (with errors below ±1°C) and energy efficient (operating at nano-Joule levels). They should also be low cost, which implies small chip area and, at most, a single-temperature trim. In recent work, smart temperature sensors intended for such applications have been reported [1], [2]. The sensor in [1] uses a single room-temperature trim and a zoom ADC, to achieve an inaccuracy of ±0.25°C (3σ) while drawing 10.8μW from a 1.8V supply. Although the sensor in [2] draws lower power (2.4μW), its inaccuracy, after a one-temperature trim, is only +0.4/-1.1°C from -20°C to 30°C.

In this work, a temperature sensor is presented whose power consumption has been reduced by 24% compared to the sensor in [1]. Moreover, it occupies 54% less area. In the following section, the operating principle of the sensor is described. Section III is devoted to the sensor's front-end, while section IV describes the zoom ADC and its implementation. The measurement results are presented in section V, and the paper ends with conclusions.

II. Operating Principle

In order to perform an accurate temperature to digital conversion, two well-defined signals are required, a temperature-dependent signal and a temperature-independent reference signal. The former is traditionally a proportional-to-absolute-temperature (PTAT) voltage, while the latter is derived from a band-gap voltage reference. Substrate PNP bipolar transistors have been extensively used to generate such PTAT and reference signals [1-5].

The base-emitter voltage V_{BE} of bipolar transistors exhibits a complementary-to-absolute-temperature (CTAT) behavior (see Fig. 1) with a nominal temperature coefficient (TC) of -2mV/K: $V_{BE} \approx (kT/q)\cdot\ln(I_C/I_S)$ where k is the Boltzmann constant, q is the electron charge, T is the temperature in Kelvin, I_C is the collector current and I_S is the PNP's saturation current. As shown in Fig. 1, the base-emitter voltage *difference* of two identical substrate PNPs biased at a 1:p collector current ratio is a PTAT voltage: $\Delta V_{BE} = V_{BE2} - V_{BE1} = (kT/q)\cdot\ln(p)$, which depends only on the thermal voltage kT/q and on p. A linear combination of V_{BE} (CTAT) and ΔV_{BE} (PTAT) results in a band-gap reference voltage $V_{REF} = V_{BE} + \alpha\cdot\Delta V_{BE}$, where α is a fixed gain factor.

An analog-to-digital converter (ADC) can then be used to determine the ratio between $\alpha\cdot\Delta V_{BE}$ (PTAT) and the reference voltage V_{REF}. The digital result is a linear function of temperature [3]: $\mu = \alpha\cdot\Delta V_{BE} / (V_{BE} + \alpha\cdot\Delta V_{BE})$. Alternatively, the ratio of V_{BE} and ΔV_{BE} can also be used as a measure of temperature [1], [5]. As shown in Fig. 2, for p=5, the ratio $X = V_{BE} / \Delta V_{BE}$ is a non-linear function of temperature. Once X is known, the PTAT function μ (see Fig. 2) can again be calculated as follows: $\mu = \alpha\cdot\Delta V_{BE}/(V_{BE}+\alpha\cdot\Delta V_{BE}) = \alpha/(\alpha+X)$.

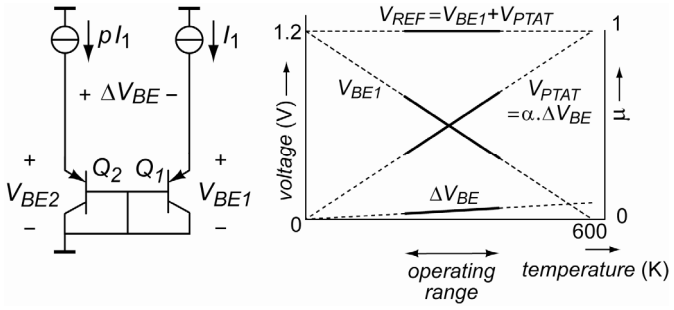

Figure 1. Two substrate PNPs generate the required voltages (V_{PTAT} and V_{REF}) for a ratiometric temperature measurement.

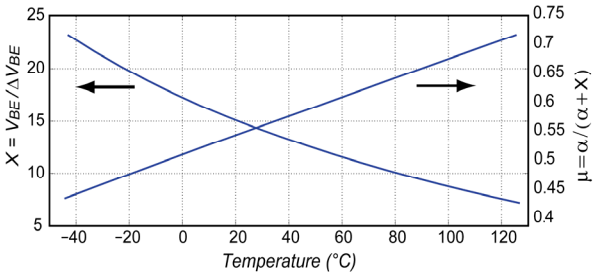

Figure 2. Non-linear $X = V_{BE} / \Delta V_{BE}$ (p=5) and linearized $\mu = \alpha/(\alpha+X)$ as a function of temperature.

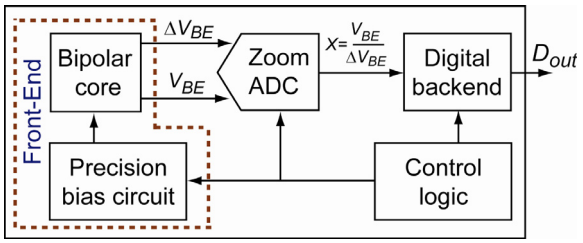

Figure 3. Block diagram of the smart temperature sensor.

The block diagram of the resulting smart temperature sensor is shown in Fig. 3. It consists of a zoom ADC and an analog front-end: a precision bias circuit whose PTAT output current biases the substrate PNP transistors of a bipolar core. The V_{BE} and ΔV_{BE} voltages extracted from the bipolar core are digitized by the zoom ADC, which outputs X to a digital backend, which then determines the PTAT function μ and D_{out}, the temperature in degrees centigrade.

III. Analog Front-End

Fig. 4 shows the circuit diagram of the analog front-end. A bias circuit uses two PNP transistors, again biased at a 5:1 current ratio, to generate an accurate PTAT current I, which is then used to bias the PNPs of the bipolar core. Since a substrate PNP transistor must be biased via its emitter, the collector current and, thus, the resulting V_{BE} will depend on the transistor's current gain β_F. The spread (up to 50%) and temperature dependence of β_F will then impact the accuracy of V_{BE}. This effect becomes more significant as the current gain β_F decreases [3], as is the case in modern CMOS processes.

In a technique known as β_F–compensation, this problem is mitigated by modifying the PTAT bias circuit so as to generate a β_F-dependent current [3]. This is done by adding a resistor $R_b/5$ in series with the base of Q_{BL}. The opamp in the feedback loop then ensures that $I = (\ln(5)\cdot(kT/q)/R_b)(\beta_F+1)/\beta_F$. When biased with this emitter current, the collector current of the PNPs in the bipolar core (Q_L, Q_R) will be equal to $(\ln(5)\cdot(kT/q)/R_b)$, and hence their base-emitter voltages will be insensitive to variations in β_F . However, the accuracy of this technique is limited by current-mirror and β_F mismatch. Careful layout of the PNPs and the current sources is, therefore, essential.

A further source of V_{BE} error is the current dependency of β_F. In this design, the value of I (=90nA) was optimized to ensure that both I and $5I$ are in the PNP's flat-β_F region. To

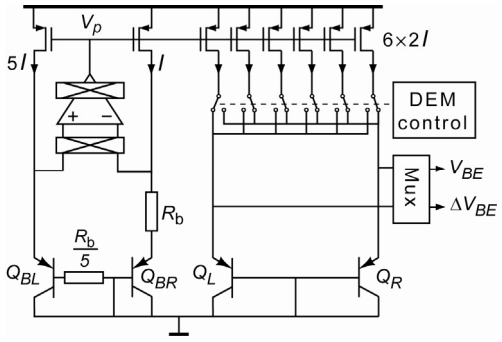

Figure 4. Circuit diagram of the analog front-end.

generate the accurate 1:5 current ratio required for an accurate ΔV_{BE}, the six current sources and the two bipolar transistors in the bipolar-core are dynamically matched, so that their mismatch is averaged out [3].

Besides the spread in R_b, the opamp's offset V_{OS} is a major source of bias current inaccuracy. For a TS inaccuracy of less than ±0.2°C, this offset needs to be less than 100μV [3]. But in CMOS, this cannot be practically achieved by transistor sizing and careful layout. By chopping the opamp, however, the resulting bias current will be switched between $I+I_{off}$ and $I-I_{off}$ where $I_{off} = V_{OS} / R_b$. Thus, the average of the resulting V_{BE} in Q_L, Q_R will be, to first order, independent of V_{OS}. However, the use of chopping means that there will be square-wave ripple at the opamp's output V_P. While the ripple amplitude is not important, complete settling of V_P at the end of each chopping phase is critical, since this is when the zoom ADC samples the resulting V_{BE}. Due to the large input capacitance of the current-mirror, however, the opamp typically requires a relatively large bias current. For example, the folded cascode opamp used in [1] drew a large portion of the sensor's supply current (1.7μA out of a total of 6μA, or 28%).

As shown in Fig. 5, an adaptive self-biasing opamp [6] is used in this work. It consists of a PMOS input pair ($M_{5,6}$) with diode-connected NMOS loads ($M_{1,2}$). Since the opamp's input voltage is chopped, switch S_1 is used to maintain the correct feedback polarity. The voltage output of the input stage ($V_{gs,M1}$ or $V_{gs,M2}$) is converted into a current via M_3 and fed back to the differential pair through the M_{10}:M_{11} current mirror. As a result, the tail current of the input stage is derived from its output voltage. The aspect ratio of the

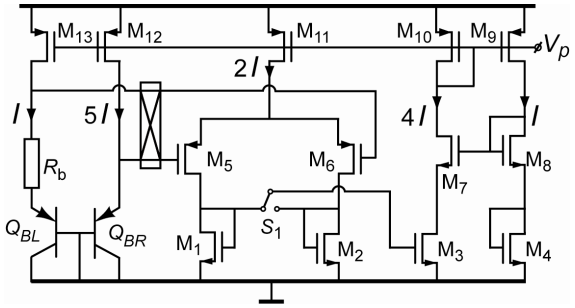

Figure 5. Simplified circuit diagram of the bias current circuit (left hand side) and positive feedback opamp.

transistors has been chosen such that: $(W/L)_3=4\cdot(W/L)_{1,2}$ and $(W/L)_{10}=2\cdot(W/L)_{11}$. This ensures that the current gain of the loop formed by $M_{1,2}$:M_3, M_{10}:M_{11} is equal to 1 for zero input. When operated in an open-loop configuration, the positive feedback in this current loop would result in ever-increasing/decreasing output currents for negative/positive differential input voltages, corresponding to a very high DC gain. In the bias circuit, however, the amplifier is operated in a negative feedback loop which stabilizes the circuit and enforces a PTAT current I. The key feature of this opamp is its high DC gain at very low tail currents ($I_{tail}=2I$=180nA at 25°C). Furthermore, since M_{10} is diode-connected, V_p is a low impedance node, which reduces the time constant associated with the settling of V_P. The current flowing in M_{10}, therefore, can be reduced to match the relaxed load requirements.

As any current mirror mismatch results in an input referred offset, a high overdrive voltage as well as careful layout are essential. To minimize the effect of channel length modulation on the current gain of the positive feedback loop, a replica circuit drives M_8 and ensures that the V_{ds} of M_3 is equal to that of $M_{1,2}$. At 25°C, the opamp draws only 630nA; a significant improvement (a 63% reduction) compared to previous work [1]. The entire front-end draws only 2.1μA from a 1.8V supply.

IV. ZOOM ADC

To minimize the sensor's energy consumption, a fast, low-power ADC is required, since the bias circuit and bipolar core draw current throughout a conversion. Moreover, accurate temperature sensors require precise calibration, and hence a high resolution ADC. ΔΣ ADCs have been widely used in temperature sensors [3–5], with 1st-order ADCs offering low complexity, while 2nd-order ADCs achieve faster speed. In this work, a zoom ADC which combines these features is used [1].

As shown in Fig. 6, the ratio $X=V_{BE}/\Delta V_{BE}$ ranges from 7 to 24 from –40°C to 125°C. X can thus be expressed as $X=n+\mu'$, where n and μ' are its integer and fractional parts, respectively, and can be determined separately (Fig. 7). In a coarse conversion, n is determined by a SAR algorithm, which compares V_{BE} to integer multiples of ΔV_{BE}. In a fine conversion, the fraction μ' is then determined by a 1st-order ΔΣ ADC, whose references are chosen so as to *zoom* into the region determined by the SAR algorithm, i.e. from $n\cdot\Delta V_{BE}$ to $(n+1)\cdot\Delta V_{BE}$. Since the region of interest is quite small (less

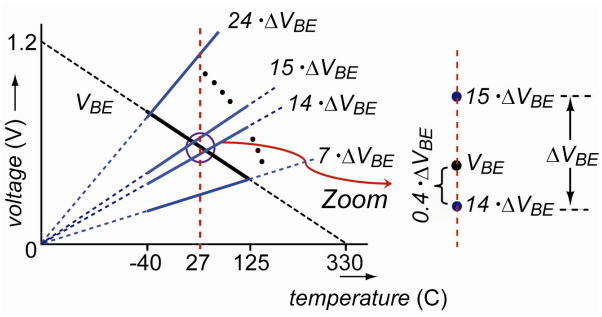

Figure 6. Temperature dependence of $k\cdot\Delta V_{BE}$ and V_{BE} from -40°C to 125°C, e.g. at room temperature: $14\cdot\Delta V_{BE} < V_{BE} < 15\cdot\Delta V_{BE}$.

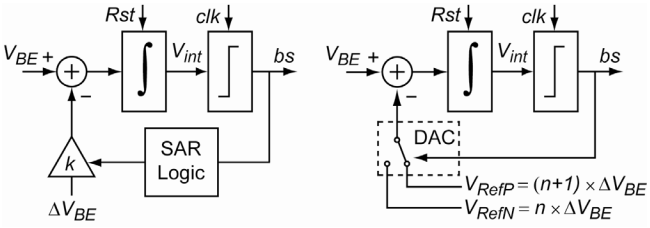

Figure 7. Block diagram of the zoom ADC during the coarse (left) and fine (right) conversions.

than 18°C), the resolution requirements on the ΔΣ ADC are greatly relaxed, thus leading to simple circuitry and short conversions. Moreover, since the accuracy-determining fine conversion still involves a ΔΣ ADC, high accuracy can be obtained with the help of the usual dynamic error cancellation techniques [3], [4].

As shown in Fig. 8, the zoom ADC is basically a modified 1st-order SC ΔΣ ADC with 24 unit sampling capacitors. At the start of each comparison step of the coarse conversion, the integrator is reset. V_{BE} is then sampled on a unit capacitor and integrated. In the next cycle, $-\Delta V_{BE}$ is sampled on k unit capacitors and also integrated. The comparator's output bs then indicates the result of the comparison $V_{BE} > k\cdot\Delta V_{BE}$. The control logic implements the SAR algorithm, with which n can be determined within five comparison steps, since $n \le 24$. Once n is known, the fine conversion step is determined with a ΔΣ charge-balancing scheme (Fig. 7). After an initial reset, the modulator operates as follows: when bs=0, $(V_{BE}-n\cdot\Delta V_{BE})$ is integrated, and when bs=1, $(V_{BE}-(n+1)\cdot\Delta V_{BE})$ is integrated. Since the net integrated charge is zero, the bitstream average is the desired $\mu'=(V_{BE}-n\cdot\Delta V_{BE})/\Delta V_{BE}$. As illustrated in Fig. 8, the main element of the zoom ADC is a SC integrator built around a folded-cascoded opamp with a gain of 86dB. Due to the relaxed requirements on the ADC's resolution, no gain boosting is required, unlike [3–5], thus reducing area and power. The sampling capacitors are also quite small: C_S = 120fF. The opamp's offset and 1/f noise are reduced by correlated double-sampling (CDS) during the coarse and fine conversions, moreover, the entire ADC is chopped twice per fine conversion [3]. Each comparison step requires two clock cycles, starting with a V_{BE} integration and

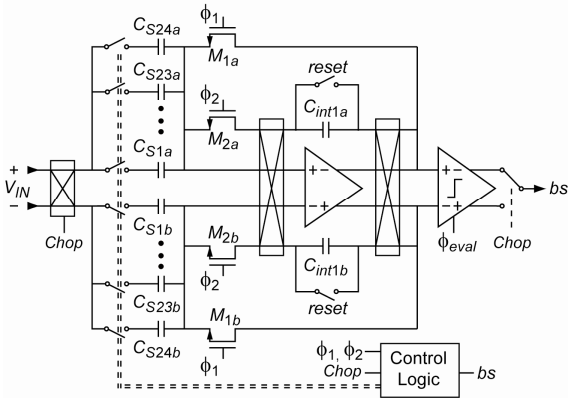

Figure 8. Circuit diagram of the zoom ADC.

followed by a $-k{\cdot}\Delta V_{BE}$ integration. As in [3], a charge proportional to V_{BE} is integrated during one clock cycle, while a charge proportional to $k{\cdot}\Delta V_{BE}$ is integrated during the other. In the coarse conversion, k is determined by the state of the SAR algorithm, while in the fine step, k is either equal to n (bs=0) or n+1 (bs=1).

To ensure that quantization errors during the coarse conversion do not lead to out-of-range errors during the fine conversion, the range of the fine conversion was increased from ΔV_{BE} to $3{\cdot}\Delta V_{BE}$. This is done in such a way that the unknown V_{BE} is always roughly in the middle of this range, thus relaxing the requirements on the coarse conversion.

V. Measurement Results

The 0.12 mm^2 (active area) sensor was realized in a standard 0.16µm CMOS process (Fig. 9). The digital back-end, the control logic and the fine conversion's sinc^2 decimation filter were implemented off-chip for flexibility. 19 devices in ceramic DIL package were measured over the temperature range from –30°C to 125°C. The resulting batch-calibrated inaccuracy was ±0.5°C (3σ), after digital compensation for residual curvature. A single digital trim at 30°C was used to compensate for V_{BE}'s PTAT spread, hence reducing the inaccuracy to ±0.2°C (3σ), as shown in Fig. 10. At 10 conversions/sec (1024 ΔΣ cycles), the sensor achieves a kT/C limited resolution of 15mK (rms), while consuming only 830nJ from a 1.8V supply. The sensor operates from a 1.6V to 2V supply with a supply sensitivity of 0.1°C/V. The sensor's performance is summarized in Table. I and compared to other low-power designs.

VI. Conclusions

A CMOS smart temperature sensor for RFID applications has been implemented. To minimize the sensor's energy consumption, a fast, low power zoom ADC has been used. By using a positive feedback amplifier in the bias circuitry, the sensor's power consumption has been reduced by 24% compared to recent work [1], while maintaining the same accuracy. Moreover, all capacitors were realized with fringe capacitors rather than metal-metal capacitors, thus reducing the chip area by about 54%. The resulting sensor occupies only 0.12mm^2 and draws only 7.4µW, the lowest ever reported for a precision temperature sensor.

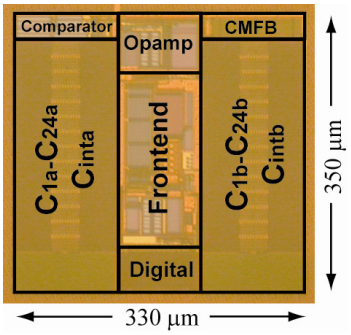

Figure 9. Chip micrograph of the sensor.

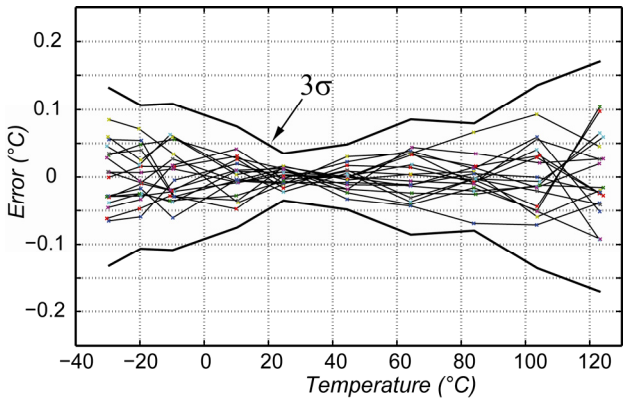

Figure 10. Temperature error of 19 measured devices after digital trimming at 30°C in the digital back-end.

TABLE I. Performance Summary and Comparison To Previous Work.

Parameter	This work	[1]	[2]	[7]
Technology	0.16µm	0.16µm	0.18µm	0.18µm
Chip area	0.12mm^2	0.26mm^2	1.1mm^2	0.05mm^2
Supply current (RT)	4.6µA	6µA	1.33µA	220nA
Supply sensitivity	0.1°C/V	0.2°C/V	-	Supply referenced
Temperature range	–30°C to 125°C	–40°C to 125°C	–20°C to 30°C	0°C to 100°C
Inaccuracy (Trim)	±0.2°C [1] (1-point)	±0.25°C [1] (1-point)	+0.4/-1.1°C [2] (1-point)	-1.6°C/+3°C [2] (2-point)
Resolution (T_{conv})	0.015°C (100msec)	0.018°C (100msec)	0.35°C (40msec)	0.1°C (100msec)

1: 3σ, 2: Maximum

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